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2D Silicon/Ferroelectric Liquid Crystal Spatial Light Modulators

We have developed a spatial light modulator technology based on foundry silicon fabrication processes. This technology employs a thin, ferroelectric liquid crystal light-modulating layer at the substrate's surface, producing electrically addressed display devices with resolutions up to 256×256 and frame rates up to 10 kHz. We have also fabricated optically addressed smart-pixel arrays for low-level image processing. Performance has advanced rapidly due to design innovations and effective use of modern process features.

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Spatial light modulator (SLM) technologies have received fresh interest with the widening of applications for optical signal processing and the rising demand for small-format displays. Wide recognition of the versatility of silicon as an electronic material and the wealth of knowledge available on it has motivated researchers to devise SLM technologies that combine silicon with various light-modulating materials and devices.[1]

Investment in time and money for silicon fabrication is enormous, making commodity silicon a bargain that is hard to beat. Using standard processes is so inexpensive compared to the alternative that it is worth adapting a design approach to the nature of this resource. Our challenge is to accommodate those characteristics of foundry VLSI that are at odds with the requirements of good SLMs.

We use standard or nearly standard commodity CMOS fabrication services provided by silicon foundries to produce chips that realize all but the light-modulating function of electrically or optically addressed SLMs. Post-processing steps can then incorporate a light-modulating layer onto the chips to turn them into complete SLMs.

The properties of the light-modulating material incorporated with the VLSI determine the usefulness and practicability of the resulting SLM technology. Ferroelectric liquid crystals (FLCs) with switching speeds at or below 100 μs operate 100 times faster than the twisted-nematic materials used in early liquid crystal light valves. Further, their mechanical properties are convenient. Being isotropic liquids at convenient temperatures (around 100°C), FLCs are compatible with straightforward procedures for creating and filling thin cells.

Ferroelectric liquid crystals and SLMs

Figure 1 (next page) shows how we incorporate a light-modulating layer on the surface of a chip. Cells are specified at chip design time by laying out cuts in the passivation glass above metal pads. The pads serve both as mirrors and switching electrodes. A window carrying a transparent conductive layer, usually indium-tin oxide (ITO), and a rubbed polymer molecular alignment layer, is contacted directly to the chip surface. The window forms the top bounding surface of the cells and provides a common reference electrode. Attaching the window and filling the chips with FLC material are the only steps performed to turn them into SLMs.

The thinness of the cells (1 to 2 μm) causes the FLC molecules to align in the surface-stabilized configuration.[2] In this mode, the FLC layer

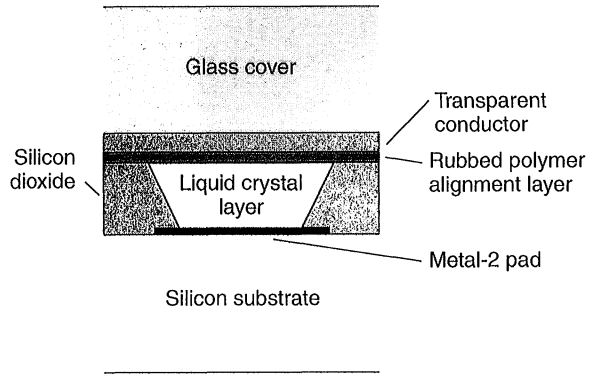

Figure 1. Typical silicon/FLC light modulator cell cross section.

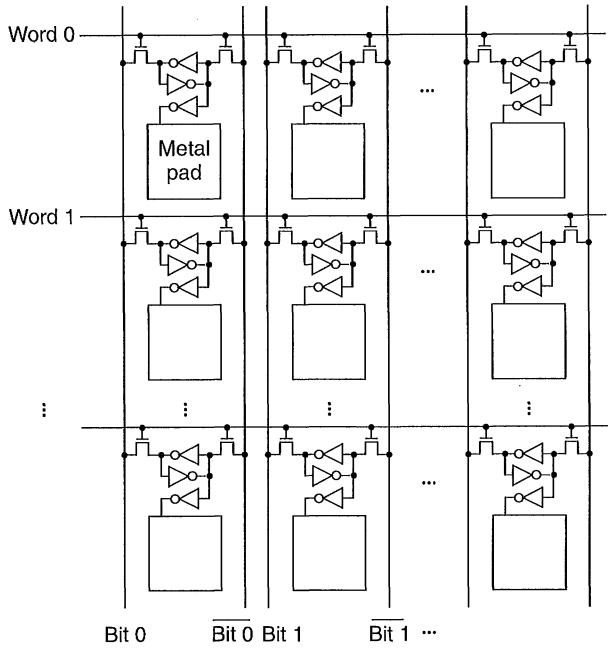

Figure 2. Pixel array circuitry of SRAM-based 64×64 SLM.

behaves optically as a uniaxially anisotropic slab with its slow axis in the plane of the bounding surfaces. When the electric field reverses, the slow axis rotates through 45 degrees. Suitable configuration of the input polarization yields a 90 degree modulation of polarization rotation, which gives rise to amplitude modulation between crossed polarizers. Electric fields of 2.5V/μm effect switching of the newer materials in 50 to 100 μs. Such fields are easily generated on a CMOS VLSI chip, and the circuit loading of a 50-μm×50-μm

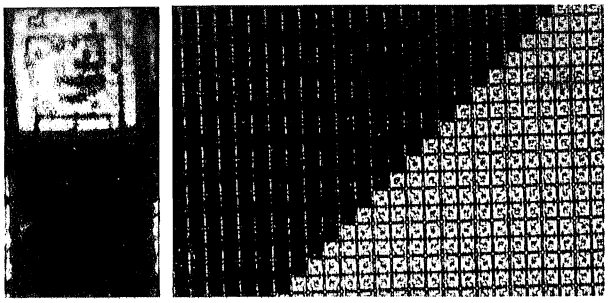

Figure 3. Photographs of a few cells of the 64×64 SRAM SLM (a), and most of the array (b), with an image displayed.

FLC cell is comparable to that of a few minimum-geometry logic gate inputs. This match in drive requirements makes silicon and FLCs a natural technology combination.

Three generations of electrically addressed SLMs

We have constructed electrically addressed SLMs by augmenting conventional static or dynamic random-access memory (SRAM or DRAM) designs with FLC light modulators. Our devices associate one modulator with each RAM cell; the binary-valued cell state drives the modulator. Interfacing to these devices is straightforward because, electrically, they resemble standard RAM parts. The designs we describe next appeared at approximately equal intervals over a five-year period. Their descriptions should convey a sense of the evolutionary pace of this SLM technology, how its progress has been tied to advances in silicon technology, and future improvements to anticipate.

64×64 SRAM-based SLM with 60-μm cell pitch. Our first device was fabricated in a 3-μm, double-metal process, based on SRAM cells of the form shown in Figure 2. The cross-coupled static inverters, coupled by nMOS pass transistors to a pair of Bit lines, constitute a standard, six-transistor, static design. An additional inverter buffers the stored state and drives a second-metal pad that completely covers the cell. This switching electrode is driven to 0V or 5V. With the common window electrode held at 2.5V, the two possible cell states result from generating equal but opposite electric fields across the FLC. We chose an 8-bit-wide data input for easy interfacing to a PC provided with a plug-in interface card. Thus, each row of the 64×64 array fills in eight write cycles.

Choosing a static cell design eliminated the need for complex drive circuitry with critical timing specifications, and thus eased the verification and demonstration of this first device. Also, the additional buffer in each cell assures that the electrical state of the memory cell is isolated from that of the

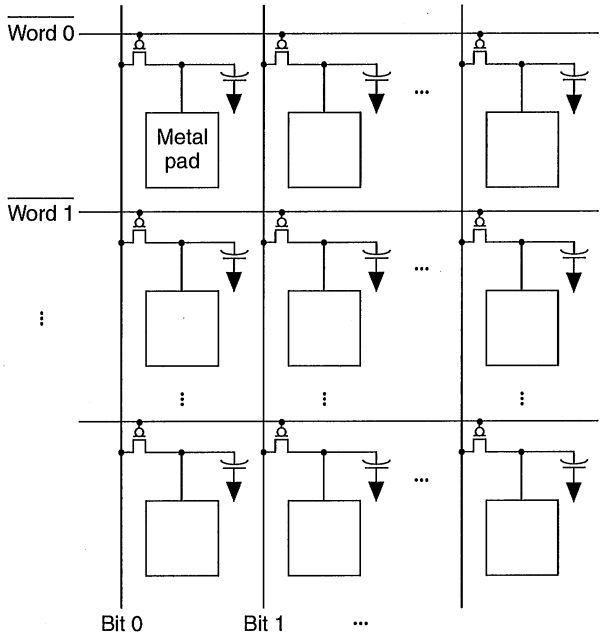

Figure 4. Pixel array circuitry of DRAM-based 256×256 SLMs. Each cell comprises a single-pass transistor controlled by a Word line, which gates the cell's internal capacitance onto a Bit line.

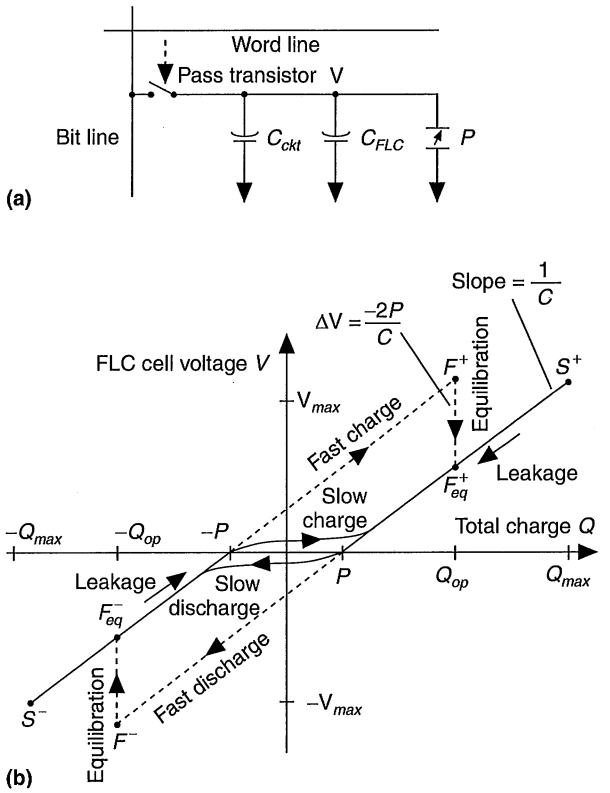

Figure 5. DRAM-style SLM pixel design: equivalent circuit (a) and voltage-charge characteristics (b).

FLC. This means that a group of eight cells can be selected, written, and deselected in just nanoseconds, and writing a new group can begin while the first group is still switching. In fact, the entire array can be written in much less than the approximately 100-µs FLC cell switching time.

Photographs of a few cells and of the whole array with a displayed image appear in Figure 3. Cells are on a 60-µm pitch. The texture visible within the bright cells results from thickness variations in the FLC film. Variations occur because of the undulating topography of the circuitry beneath the second-metal layer. The fabrication process' 5-µm second-metal spacing rule and the provision for individual passivation cuts for each cell determined the 67-percent area fill factor. We measured intensity contrast ratios of 12:1 using 633-nm HeNe laser light. The SLM operated at a 4.5-kHz frame rate without attenuation of the peak-to-peak optical response.[3]

256×256 DRAM-based SLM with 20-µm cell pitch. The static cell design has advantages, such as easily met drive requirements and drive pipelining, but requires too much area for use in high-resolution displays. We implemented our next design in a 2-µm process and also moved to a dynamic cell configuration, shown in Figure 4.

Since all the FLC switching charge must now come through the Bit line, charge dynamics within the cell become important, as does maximizing the time the cells connect with their Bit lines. To accomplish the latter, we incorporated a 256-bit-wide pipeline register into the data path. To write a row, 32-bit words are read sequentially into eight registers. These word registers then dump in parallel into the full-row pipeline register. The register's contents are gated onto the Bit lines, while the word registers are loaded with the next row's data. Thus, each cell is driven by its Bit line during the active phase of a Word line cycle that lasts practically 1/256th of the frame time. At television frame rates, the resulting 65-µs Word cycle is commensurate with the FLC switching time. However, framing at 4 kHz reduces this time to less than 1 µs. How does this affect the writing process?

Charge dynamics of the FLC now come into play. Physically, we can model the modulator cell as a suspension of electric dipoles in a viscous dielectric fluid, bounded by parallel-plate electrodes. Figure 5a shows the pass transistor as a switch, and C_{ckt} represents the combination of an explicit MOS capacitor with other parasitic circuit capacitances. We represent the FLC cell as the parallel combination of linear

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