Ferroelectric-liquid-crystal/silicon-integrated-circuit spatial light modulator

L. K. Cotter

Displaytech, Inc., 2200 Central Avenue, Boulder, Colorado 80301

T. J. Drabik

School of Electrical Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332

R. J. Dillon and M. A. Handschy

Displaytech, Inc., 2200 Central Avenue, Boulder, Colorado 80301

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We present the design and characterization of a spatial light modulator (SLM) comprising a ferroelectric-liquid-crystal light-modulating layer on top of a silicon integrated circuit. Our SLM consists of two electrically addressed arrays on the same integrated-circuit die. The first, a 1×128 linear array with a 20-μm center-to-center element spacing, used shift register addressing, while the second, a 64×64 square array with 60-μm pitch, used static random access memory addressing. The resulting SLM could be addressed at frame rates of up to 4.5 kHz and gave single-element intensity contrast ratios of 12:1.

A high-performance spatial light modulator (SLM) is the key component for many proposed optical computers. The SLM, a typically two-dimensional array of light modulators, spatially encodes data bits onto a light beam as an image. It is by processing these entire image frames in rapid succession that the computers achieve high speed. Consequently, the frame rate of the SLM limits overall computing speed. We present here a SLM that exploits the low-voltage, low-power, fast electro-optic properties of ferroelectric liquid crystals (FLC's) to attain a high frame rate. We put a FLC light-modulating layer directly atop a silicon integrated circuit (IC), using functional elements of the IC to apply the required driving voltages to the FLC layer.

Lee *et al.*[1] use a similar approach with $(Pb_{1-x}La_x)(Zr_yTi_{1-y})_{1-x/4}O_3$ (PLZT) light modulators, but the problems of integrating the light modulator with the silicon circuitry are much more difficult for the ceramic PLZT than for the organic liquid FLC. FLC's are directly compatible with standard IC processing, as has been demonstrated by Drabik and Gaylord, who fabricated FLC light modulators on a silicon die processed according to standard complementary metal oxide semiconductor (CMOS) steps but containing no functional circuitry.[2] Picart *et al.*[3] have applied both nematics and FLC's to circuits with very-large-scale integration (VLSI) to obtain average and real-time visualization of circuit voltages. McKnight *et al.*[4] have demonstrated small SLM's using the slower nematic liquid crystals on a static random access memory (SRAM) IC. Nematics on silicon IC's were first used to make miniature displays.[5,6] Our FLC/IC hybrid approach, which was independently proposed by Collings *et al.*,[7] who called it the "active-backplane" SLM, permits frame times equal to the FLC switching time independent of the number of elements in the SLM, in contrast to commonly used passive matrix addressing techniques[7] whose line-at-a-time character will likely limit frame rates to the order of 100 Hz.[8]

To exploit the electro-optic properties of FLCs most advantageously, we prefer the surface-stabilized FLC geometry,[9,10] where the FLC is confined between electrode plates spaced closely enough to unwind the FLC's intrinsic helical structure permanently. Figure 1(a) shows our hybrid SLM with the FLC layer between an IC (the bottom plate) and a glass coated on its inner surface with an indium tin oxide transparent electrode (the top plate). Metal electrode pads on the IC upper surface define reflective SLM elements. The FLC film is optically uniaxial with birefringence $\Delta n \approx 0.15$; voltages applied between an IC pad and the

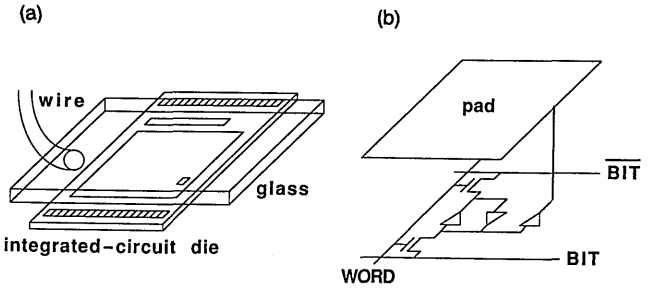

Fig. 1. (a) Construction of the FLC/silicon IC SLM. (b) Schematic diagram of the SLM square-array SRAM element. The element's state is changeable only when the WORD line is high; otherwise the static latch formed by the cross-coupled inverters holds the state last determined by the BIT and $\overline{\text{BIT}}$ lines. The latch output is buffered by the third inverter onto the FLC driving pad.

glass common electrode select according to their sign between two FLC optic-axis orientations, both lying nearly parallel to the plates but differing in direction by a characteristic angle θ that can be $\approx 45°$ by appropriate choice of FLC material and driving voltage. We performed intensity modulation with this switchable wave plate by illuminating it with polarized light whose polarization direction was parallel to the optic axis of one of the FLC's states. In this state the reflected light has the incident polarization and is rejected by a crossed analyzer following a beam splitter (the dark state). In the other FLC state the incident light is resolved into ordinary and extraordinary modes, ideally of equal amplitude ($\theta = 45°$). The FLC film introduces a phase shift between these modes; by a choice of the FLC film thickness d such that the phase shift is π, i.e., $\Delta nd/\lambda = 1/4$, the reflected light will be linearly polarized at an angle 2θ to the incident polarization and hence passed by the analyzer (the bright state).

We put two electrically addressed arrays on the same IC die. The first, a 1×128 one-dimensional array with a 20-μm center-to-center element spacing, used shift register addressing, while the second, a 64×64 two-dimensional array with a 60-μm pitch, used SRAM addressing. The addressing circuitry was optimized for a high frame rate. A single cell of the SRAM array, illustrated schematically in Fig. 1(b), comprises a six-transistor static RAM cell[11] augmented with an inverter to isolate the load of the switching electrode from the cell's state. This permits latching of a state into a cell in a few nanoseconds without waiting a number of microseconds for the liquid crystal driven by the cell to complete switching. Additional provisions for speed in the two-dimensional device design are a byte-wide write operation to reduce the number of write cycles required per frame and a row–page writing mode. In the row–page mode, the WORD line selecting a row is held high while all eight bytes in that row are written; therefore the WORD line need be toggled high and low only once per written row. Inclusion of these design features has led to the capability of writing a complete frame into the two-dimensional device in less than the switching time of the FLC material used; thus the cell outputs can be made to change nearly in unison. In the one-dimensional device the shift register cells were also buffered from the FLC material with extra inverters. This permits clocking of the shift register a high speeds ($\approx$10 MHz) and therefore the loading of a new 128-long frame in less than the switching time of the FLC cells.

The IC was designed by us and fabricated at MOSIS,[12] the Defense Advanced Research Projects Agency/National Science Foundation silicon brokerage service. The chip was fabricated in a 3-μm CMOS double-metal p-well process and could provide 0- or 5-V drive to the reflective pads. By connecting the glass common electrode to 2.5 V, either plus or minus 2.5 V could be applied to the FLC. The functional cell circuitry in the lower levels of the IC was made from field-effect transistors of doped silicon and oxide layers, interconnected by conductors in added polysilicon and first metal layers. Each cell drives a reflective pad in a second-level metal layer. In the final layer of sputtered passivation glass we specified an opening over each reflective pad, which provided both electrical contact between each element's electrode and the FLC and part of the spacer layer separating the pad from the top electrode plate of the completed device. The elements were on 60-μm centers, with square second-metal pads 55 μm on a side centered under openings 45 μm on a side in the passivation glass.

After testing the electrical function of the IC's, we assembled the chips into complete FLC cells. We applied a rubbed nylon alignment layer to a clean indium tin oxide-coated glass plate and soldered on a fine wire to permit connection to the indium tin oxide. After dusting off the IC with a gentle, filtered static-free air stream, we laid the glass plate directly on the die, with the glass narrow enough to fit between the rows of wire bonds on the two opposing edges of the die and long enough to permit the soldered wire to hang over the edge of the die. The assembly was clamped together and filled under vacuum with liquid crystal ZLI-4003.[13] Our first SLM's were held together only by the liquid crystal's surface tension. This technique proved successful, although to preserve the cell parallelism for long periods we found it necessary to glue the glass plate to the IC at the expense of small portions of the arrays' being lost owing to glue flow between the glass plate and the IC. A number of permanent bonding techniques have been used to join substrates in situations with requirements and conditions similar to ours[14]; we anticipate little difficulty in adapting a bonding technique to the production of silicon/FLC devices.

Figure 2 shows a microphotograph of the square array. The surface of the square array is much like that of a waffle, with the passivation glass overlayer forming the ridges and the metal reflectors sitting at the bottom of the FLC-filled wells. The highest points on the ridges, over the addressing lines, contact and support the glass plate. Judged by comparing their largely yellow color between crossed polarizers

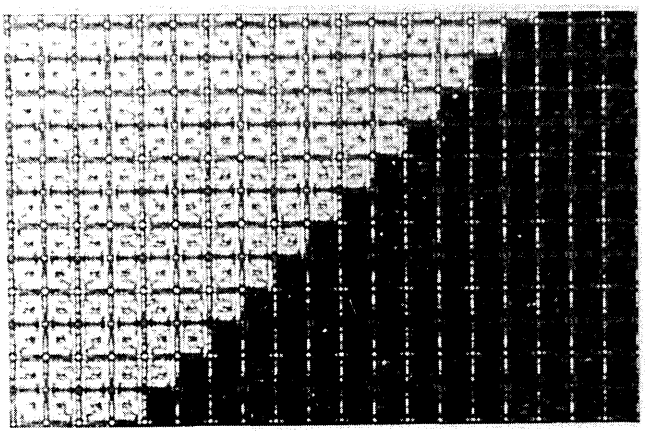

Fig. 2. Reflected light microphotograph of a portion of the 64×64 square array between crossed polarizers. The array has been oriented so that the FLC state in half the elements has its optic axis parallel to the polarizer. These elements appear dark, while the other elements appear bright, their FLC axis making an angle $\approx 25°$ to the polarizer. The elements are on 60-μm centers.

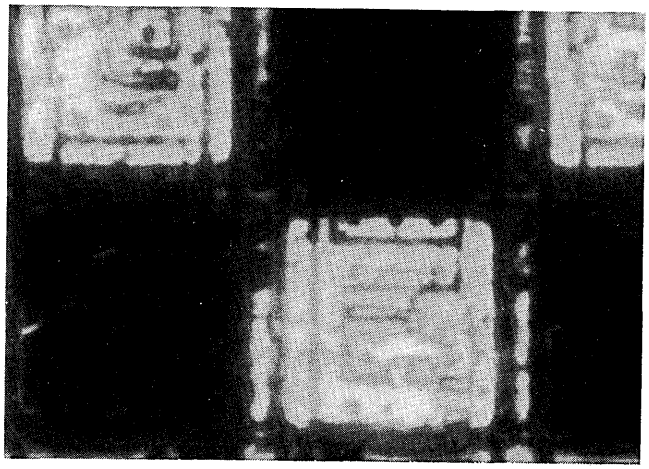

Fig. 3. Higher-magnification microphotograph of the square array showing structure within the elements due to the underlying circuitry topography.

with FLC cells of known thickness, the elements in the two-dimensional array have a FLC film thickness of approximately 1 μm. Structure visible within the bright elements in the square array (Fig. 3) is due to the underlying circuitry, which makes the metal reflector bumpy; these bumps cause variations in the thickness of the FLC layer that result in the observed variations of appearance within each element. In the linear array (not shown) all circuitry is off to the side and the reflectors themselves are flat with no underlying structure.

We measured intensity contrast ratios of 12:1 on single elements within the square array using He–Ne laser light whose 633-nm wavelength should have been close to the transmittance peak indicated by the cells' yellow color. To measure the SLM's frame rate we drove the square array alternately all bright and all dark; the highest frequency attained without attenuation of the peak-to-peak optical response was 2.25 kHz, for a frame rate of 4.5 kHz. The optical rise and fall times were FLC limited at 120 μsec. At this frame rate the 64 × 64 SLM has a data throughput of 18 Mbit/sec.

In conclusion, we have demonstrated how two relatively mature technologies, silicon VLSI and FLC's, can be simply combined to make a hybrid SLM. The FLC light modulator's low drive voltage requirements makes it a good match to the characteristics of the standard CMOS IC. Its low power dissipation, unlike that of most light-modulation technologies, prevents thermal dissipation from limiting the frame speed. For example, even allowing for 10-W/cm^2 dissipation, an efficient PLZT/IC SLM is estimated to be thermally limited to a 50-kHz frame rate[1]; a FLC SLM could be framed 10 times more frequently.[15] At a thermal dissipation level that could be achieved without special measures, say 100 mW/cm^2, the PLZT frame rate would drop to 500 Hz, while if FLC dissipation were the only limit, 70 kHz would be allowable. However, power dissipation by the silicon active backplane is likely to be more limiting than dissipation from the FLC.[7] FLC/IC SLM's of a quality satisfactory for optical processors will also require further research to produce flat arrays with optically uniform elements, which can be based in part on IC planarization processes.[16]

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