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Paper 7
Entered: January 21, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ATOPTECH, INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

Case IPR2014-01145
Patent 6,237,127 B1

Before TRENTON A. WARD, PETER P. CHEN, and FRANCES L. IPPOLITO, *Administrative Patent Judges.*

IPPOLITO, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner ATopTech, Inc. filed a Petition on July 11, 2014, requesting an *inter partes* review of claims 1–13 of U.S. Patent No. 6,237,127 B1 (Ex. 1001, "the '127 patent"). Paper 1 ("Pet."). Patent Owner Synopsys, Inc. timely filed a Preliminary Response to the Petition. Paper 6 ("Prelim. Resp.").

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least one of the claims challenged in the petition." 35 U.S.C. § 314(a).

Pursuant to 35 U.S.C. § 314, we conclude there is a reasonable likelihood that Petitioner would prevail with respect to claims 1–4 and 7–11 of the '127 patent. We deny the Petition as to claims 5, 6, 12, and 13.

A. Related Proceedings

The '127 patent is involved in a district court proceeding in the U.S. District Court of the Northern District of California captioned *Synopsys, Inc. v. ATopTech, Inc.*, Case No. 3:13-cv-02965-MMC (N.D. Cal. 2013). Pet. 1. Additionally, Petitioner has filed Petitions challenging the patentability of certain claims of Patent Owner's US Patent Nos. 6,567,967 (IPR2014-01150 and IPR2014-01159), 6,507,941 (IPR2014-01153), and 6,405,348 (IPR2014-01160).

B. The '127 Patent

The '127 patent relates generally to the static timing analysis of digital electronic circuits, and in particular applies static timing analysis to

synthesis of circuits by analyzing certain paths of a circuit using "non-default timing constraints known as 'exceptions.'" Ex. 1001, Title, 1:8–11. Exceptions allow a circuit designer, working with a circuit synthesis system, to specify certain paths through the circuit to be synthesized as being subject to non-default timing constraints. *Id.*, Abstract. The '127 patent discloses that static timing analysis had been used to verify that the design of a digital electronic circuit would perform correctly at the target clock speeds, and "[f]or similar reasons, it would be useful to apply, as efficiently as possible, static timing analysis to the synthesis process." *Id.* at 1:40–42. Specifically, the '127 patent discloses performing static timing analysis on units of a circuit, referred to as "sections," which comprise a set of "launch" flip flops, non-cyclic combinational circuitry, and a set of "capture" flip flops. *Id.* at 2:1–4.

The static timing analysis described in the '127 patent is accomplished in two main phases: (1) propagation of tagged rise-fall (RF) timing tables and (2) relative constraint analysis. Ex. 1001, 8:37–41. In the first phase of the timing analysis, delays between inputs and outputs of circuit devices are represented by "timing arcs." Ex. 1001, 8:44–45. Using the timing arcs for the circuit devices, maximum and minimum delay values for the rise time and the fall time are determined and stored in RF timing tables. *Id.* at 9:54–67. The timing tables are propagated through the circuit and the delays at each circuit node are added to the minimum and maximum values of the timing table from the previous node. *Id.* at 9:58–13:2, Fig. 5. Additionally, each timing table is associated with a "tag" that may include clock identifier and a variety of "labels." Ex. 1001, 3:11–15, 10:21–25. The labels of a

"tag" also may identify points in the circuit referenced by an exception. Ex. 1001, 3:29–32.

After the propagation of the timing tables through the circuit, the second phase of the timing analysis, relative constraint analysis, is performed. Ex. 1001, 13:3–4. Relative constraint analysis involves the comparison of the delay values included in the timing tables with the timing constraints of the circuit. *Id.* at 13:66–14:27. The '127 patent describes maximum allowable path delays (MAPDs) and shortest allowable path delays (SAPDs), which are default timing constraints alterable by exceptions. *Id.* at 13:34–63, 14:30–38. The delay values stored in the timing tables are compared to the MAPD and SAPD values, and if the MAPD and SAPD timing constraints are satisfied, the circuit has passed the static timing analysis. *Id.* at 13:56–14:26.

Additionally, with respect to exceptions, the '127 patent instructs "[e]xceptions are specified by the circuit designer as individual syntactic units called 'exception statements' which are comprised of a 'timing alteration' and a 'path specification.'" Ex. 1001, 1:58–61. The timing alteration instructs the timing analyzer how to alter the default timing constraints for paths through the circuit to be analyzed which satisfy the path specification. *Id.* at 1:61–63. For example, a "set_false_path" exception indicates that for paths satisfying the path specification, the relevant MAPD value is set to infinity and the relevant SAPD value is set to zero for the relative constraint analysis. *Id.* at 14:47–54.

C. Illustrative Claim

Of the challenged claims, claim 1 is independent. Claim 1 reproduced below is illustrative of the subject matter of the '127 patent:

> 1. A method performed in a circuit analysis process, comprising the steps performed by a data processing system of:
>
> marking certain points in a circuit description according to their being referenced by at least a first exception;
>
> propagating a plurality of timing tables through the circuit description; and
>
> wherein at least a first timing table, of the plurality of timing tables, refers to a tag comprising at least a first label indicating a marked point in the circuit description, through which the table has been propagated.

D. The Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable over the following grounds:

Reference(s)	Basis	Claims Challenged
Belkhale[1]	§ 102	1–11 and 13
Belkhale	§ 103	1–13
Belkhale and Tom[2]	§ 103	1–13

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *see also* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Under the broadest reasonable construction standard, claim terms are given

[1] Krishna Belkhale, *Timing Analysis with Known False Sub Graphs*, in IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN, DIGEST OF TECHNICAL PAPERS 736–740 (Nov. 5–9, 1995) (Ex. 1005, "Belkhale").

[2] U.S. Patent No. 5,210,700, issued May 11, 1993 (Ex. 1006, "Tom").

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