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Paper 24
Entered: January 19, 2016

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ATOPTECH, INC.,
Petitioner,

v.

SYNOPSYS, INC.,
Patent Owner.

Case IPR2014-01145
Patent 6,237,127 B1

Before TRENTON A. WARD, MATTHEW R. CLEMENTS, and PETER P. CHEN, Administrative Patent Judges.

WARD, *Administrative Patent Judge*.

DECISION
FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

We have statutory authority under 35 U.S.C. § 6(c). This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

With respect to the grounds instituted in this trial, we have considered the papers submitted by the parties and the evidence cited therein. For the reasons discussed below, we determine Petitioner has shown by a preponderance of the evidence that claims 1–4 and 7–11 of U.S. Patent No. 6,237,127 B1 (Ex. 1001, "the '127 patent") are unpatentable.

A. BACKGROUND

ATopTech, Inc. ("Petitioner") filed a Petition requesting an *inter partes* review of claims 1–13 of the '127 patent. Paper 2 ("Pet."). Synopsys, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). On January 21, 2015, we instituted an *inter partes* review for claims 1–4 and 7–11 on certain grounds of unpatentability alleged in the Petition. Paper 7 ("Dec. on Inst.").

After institution of trial, Patent Owner filed a Patent Owner Response (Paper 15, "PO Resp."), to which Petitioner filed a Reply (Paper 18, "Pet. Reply"). An oral hearing was held on November 13, 2015, consolidated with the hearings in IPR2014-01150 and IPR2014-01159. The transcript of the consolidated hearing has been entered into the record. Paper 23 ("Tr.").

B. RELATED PROCEEDINGS

The '127 patent is involved in a district court proceeding in the U.S. District Court of the Northern District of California, captioned *Synopsys, Inc. v. ATopTech, Inc.*, Case No. 3:13-cv-02965-MMC (N.D. Cal. 2013). Pet. 1. In a related proceeding before the Board, we instituted an *inter*

partes review of claims 1, 4, 8, 9, 12, 16, 19–22, and 32–36 of U.S. Patent No. 6,567,967 B2, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01150, slip. op. 22–23 (PTAB January 21, 2015) (Paper 11). Additionally, we instituted an *inter partes* review of claims 5, 23, 24, 26, 27, and 31 of U.S. Patent No. 6,567,967 B2, in *ATopTech, Inc. v Synopsys, Inc.*, Case IPR2014-01159, slip. op. 25–26 (PTAB January 21, 2015) (Paper 11).

C. THE '127 PATENT

The '127 patent relates generally to the static timing analysis of digital electronic circuits, and in particular applies static timing analysis to synthesis of circuits by analyzing certain paths of a circuit using "non-default timing constraints known as exceptions." Ex. 1001, Title, 1:8–11. Exceptions allow a circuit designer, working with a circuit synthesis system, to specify certain paths through the circuit to be synthesized as being subject to non-default timing constraints. *Id.*, Abstract. The '127 patent discloses that static timing analysis had been used to verify that the design of a digital electronic circuit would perform correctly at the target clock speeds, and "[f]or similar reasons, it would be useful to apply, as efficiently as possible, static timing analysis to the synthesis process." *Id.* at 1:40–42. Specifically, the '127 patent discloses performing static timing analysis on units of a circuit, referred to as "sections," which comprise a set of "launch" flip flops, non-cyclic combinational circuitry, and a set of "capture" flip flops. *Id.* at 2:1–4.

The static timing analysis described in the '127 patent is accomplished in two main phases: (1) propagation of tagged rise-fall (RF) timing tables and (2) relative constraint analysis. Ex. 1001, 8:37–41. In the first phase of the timing analysis, delays between inputs and outputs of circuit devices are

represented by "timing arcs." Ex. 1001, 8:44–45. Using the timing arcs for the circuit devices, maximum and minimum delay values for the rise time and the fall time are determined and stored in RF timing tables. *Id*. at 9:54–67. The timing tables are propagated through the circuit and the delays at each circuit node are added to the minimum and maximum values of the timing table from the previous node. *Id*. at 9:58–13:2, Fig. 5. Additionally, each timing table is associated with a "tag" that may include a clock identifier and a variety of "labels." Ex. 1001, 3:11–15, 10:21–25. The labels of a "tag" also may identify points in the circuit referenced by an exception. Ex. 1001, 3:29–32.

After the propagation of the timing tables through the circuit, the second phase of the timing analysis, relative constraint analysis, is performed. Ex. 1001, 13:3–4. Relative constraint analysis involves the comparison of the delay values included in the timing tables with the timing constraints of the circuit. *Id*. at 13:66–14:27. The '127 patent describes maximum allowable path delays ("MAPD"s) and shortest allowable path delays ("SAPD"s), which are default timing constraints alterable by exceptions. *Id*. at 13:34–63, 14:30–38. The delay values stored in the timing tables are compared to the MAPD and SAPD values, and if the MAPD and SAPD timing constraints are satisfied, the circuit has passed the static timing analysis. *Id*. at 13:56–14:26.

Additionally, with respect to exceptions, the '127 patent instructs "[e]xceptions are specified by the circuit designer as individual syntactic units called 'exception statements' which are comprised of a 'timing alteration' and a 'path specification.'" Ex. 1001, 1:58–61. The timing alteration instructs the timing analyzer how to alter the default timing

constraints for paths through the circuit to be analyzed which satisfy the path specification. *Id*. at 1:61–63. For example, a "set_false_path" exception indicates that for paths satisfying the path specification, the relevant MAPD value is set to infinity and the relevant SAPD value is set to zero for the relative constraint analysis. *Id*. at 14:47–54.

Claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. A method performed in a circuit analysis process, comprising the steps performed by a data processing system of:
>
> marking certain points in a circuit description according to their being referenced by at least a first exception;
>
> propagating a plurality of timing tables through the circuit description; and
>
> wherein at least a first timing table, of the plurality of timing tables, refers to a tag comprising at least a first label indicating a marked point in the circuit description, through which the table has been propagated.

Id. at 31:47–32:5.

D. LEVEL OF ORDINARY SKILL IN THE ART

Patent Owner's declarant, Dr. Martin G. Walker, states that in view of the '127 patent, a person of ordinary skill in the art would have a minimum of a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or a closely related field and would have a minimum of one to two years of professional experience in the development and analysis of digital electronic circuits.

Ex. 2004, Declaration of Dr. Martin G. Walker ¶ 22. Petitioner does not disagree with Dr. Walker's opinion as to the proper level of ordinary skill in the art. Pet. Reply 17.

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