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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SYNOPSYS, INC.
Petitioner

v.

MENTOR GRAPHICS CORPORATION
Patent Owner

Case IPR2012-00042
Patent 6,240,376 B1

Before SALLY C. MEDLEY, HOWARD B. BLANKENSHIP, and JENNIFER S. BISK, *Administrative Patent Judges.*

BISK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Synopsys, Inc. filed a petition to institute an *inter partes* review of U.S. Patent 6,240,376 B1 (Ex. 1001) (the "'376 patent"). 35 U.S.C. § 311. For the reasons that follow, the Board, acting on behalf of the Director, has determined to institute an *inter partes* review. 35 U.S.C. § 314.

OPINION

I. INTRODUCTION

A. Background

Synopsis requests *inter partes* review of claims 1-15 and 20-33 of the '376 patent alleging that each of the claims is unpatentable under 35 U.S.C. §§102 and/or 103 based on the following prior art references: Koch, et. al, "Breakpoints and Breakpoint Detection in Source Level Emulation," ISSS Proceedings of the 9th Int'l Symposium on System Synthesis 26-31 (1996) (Ex. 1004) ("Koch"); Koch, et. al, "Debugging of Behavioral VHDL Specifications by Source Level Emulation," Proceedings of the European Design Automation Conference 256-261 (Sept. 1995) (Ex. 1006) ("1995 Koch"); U.S. 6,132,109 (Ex. 1007) ("Gregory"); HDL-ICE™ ASIC Emulation System, Quickturn Design Systems, Inc. (Ex. 1008) ("HDL-ICE"); and U.S. 5,960,191 (Ex. 1009) ("Sample"). The specific grounds are detailed below.

Reference[s]	**Basis**	**Claims challenged**
Koch	§§ 102 and 103	1-5, 8-10, 20-24, 28, 32, and 33
Koch and 1995 Koch	§ 103	11 and 25-27
Gregory	§§ 102 and 103	1-9, 11-14, 24, 25, and 28-33
Gregory and 1995 Koch	§ 103	10, 15, 20-23, 26, and 27
HDL-ICE	§§ 102 and 103	1, 2, 5, 10, 11, and 28

Sample	§§ 102 and 103	1, 2, 5, 10, and 28
Sample and 1995 Koch	§ 103	11

The ’376 patent has been and is currently involved in district court litigation. On March 13, 2006, Mentor Graphics filed a complaint against EVE-USA, Inc. and Emulation and Verification Engineering, S.A. alleging infringement of the ’376 patent. *Mentor Graphics Corp. v. EVE-USA, Inc.*, 06-cv-341-AA (D. Or.). Pet. 1. The case was dismissed with prejudice on November 30, 2006. *Id.* On September 27, 2012, the day after the Petition in this case was filed, Petitioner filed a complaint for declaratory judgment for invalidity of all claims of the ’376 patent in the Northern District of California. *Synopsys, Inc. v. Mentor Graphics Corp.*, 12-cv-05025-LB (N.D. Cal.). That case is ongoing. Ex. 2004.

B. The ’376 patent

The ’376 patent generally relates to the fields of simulation and prototyping of integrated circuits. ’376 patent col. 1, ll. 10-11. In particular, the patent describes “debugging synthesizable code at the register transfer level during gate-level simulation.” *Id.* col. 1, ll. 11-13.

As described in the Background of the Invention, integrated circuit design begins with a description of the behavior desired in a high level description language (“HDL”) such as Very High Speed Integrated Circuit Description Language (“VHDL”). *Id.* col. 1, ll. 14-25. A subset of HDL source code is referred to as Register Transfer Level (“RTL”) source code. *Id.* col. 1, ll. 28-30. The RTL description of a circuit can be used by synthesis tools to generate a “gate-level

netlist," which in turn can be converted to a format suitable for programming a hardware emulator. *Id.* col. 1, ll. 35-42.

Gate-level simulation is useful for validation of a circuit design. *Id.* col. 1, ll. 55-67. However, much of the high-level information is lost during synthesis, resulting in the unavailability of many traditional debugging tools, such as setting breakpoints and visually tracing source code execution. *Id.* col. 2, ll. 1-23. The '376 patent describes a method of synthesizing RTL source code such that the resulting gate-level simulation can support these traditional debugging tools. *Id.* col. 2, ll. 26-30.

Claim 1, reproduced below, illustrates the claimed subject matter:

A method comprising the steps of:

a) identifying at least one statement within a register transfer level (RTL) synthesizable source code; and

b) synthesizing the source code into a gate-level netlist including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement.

C. Claim Construction

As a step in our analysis for determining whether to institute a trial, we determine the meaning of the claims. Consistent with the statute and the legislative history of the AIA, the Board will interpret claims using the broadest reasonable construction. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012); 37 CFR § 100(b). There is a "heavy presumption" that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). By "plain meaning" we refer to the

ordinary and customary meaning the term would have to a person of ordinary skill in the art. Such terms have been held to require no construction. *See, e.g.*, *Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1349 (Fed. Cir. 2001) (finding no error in non-construction of "melting"); *Mentor H/S, Inc. v. Med. Device Alliance, Inc.*, 244 F.3d 1365, 1380 (Fed. Cir. 2001) (finding no error in court's refusal to construe "irrigating" and "frictional heat").

Petitioner submits that for purposes of this review, the claim terms take on the ordinary and customary meaning that the terms would have to one of ordinary skill in the art. Pet. 4. Petitioner does not address what this meaning would be for any specific claim term. In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (en banc). In this case, Petitioner does not argue that any term has a different meaning to a lay person than to a person of ordinary skill in the art. Except for the following terms, Petitioner's proposal of plain and ordinary meaning, with no elaboration, does not appear unreasonable at this stage of the proceeding. Because this position is not challenged by Patent Owner, we adopt it. However, resolving the issues set forth in the Petition requires a more detailed definition for at least the terms "instrumentation signal," "gate-level netlist," "gate-level design," and "sensitivity list."

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