# United States Patent [19]

### Darbee et al.

[56]

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4,959,810

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[54]	UNIVERSA	AL REMOTE CONTROL DEVICE	4,769,643	9/1988	Sogame 340/825.69
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[75]	Inventors:	Paul V. Darbee, Santa Ana; Richard	4,774,511	9/1988	Rumbott et al 340/825.69
		E. Ellis, Garden Grove; Louis S.	, , , , , , , ,		Yamamoto 340/825.69
		Jansky, Long Beach; Avram S.	4,807,052	2/1989	Amano 455/355
		Grossman, Santa Ana, all of Calif.	4,825,200	4/1989	Evans et al 341/23
		•	4,841,368	6/1989	Rumbolt et al 455/352
[73]	Assignee:	Universal Electronics, Inc., Tustin,	4,855,746	8/1989	Stacy 358/194.1
		Calif.	4,856,081	8/1989	Smith 455/151
f0.13	A 1 NT-	107.000	4,860,380	8/1989	Mengel 455/185
[21]	Appl. No.:	127,399	4,866,434	9/1989	Keenan 340/825.69
[22]	Filed: Dec. 2, 1987		Primary Examiner-Andrew J. James		
	Rela	Assistant Examiner—Viet Q. Nguyen Attorney, Agent, or Firm—Thomas R. Vigil			
[63]	[63] Continuation-in-part of Ser. No. 109 336 Oct. 14, 1987				

[63]	Continuation-in-part of Ser. No. 109,336, Oct. 14, 1987,
	abandoned.

[51]	Int. Cl. <sup>5</sup> H04	В 9/00; (	
[52]	U.S. Cl	364/900;	H04Q 1/00 340/825.69
	340/825.57; 340/825.3	72; 455/1	51; 455/603
			455/352

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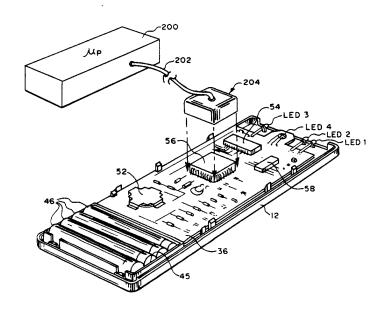
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## [57] ABSTRACT

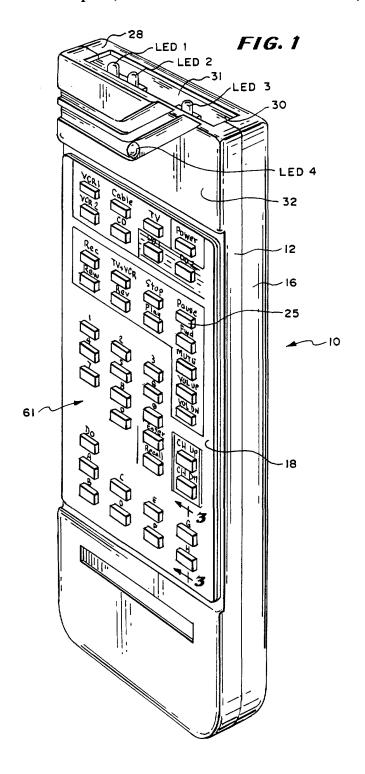
The universal remote control system comprises data processor, input device including a keyboard and a keyboard circuit connected to the data processor, signal output device including circuitry for generating infrared light codes connected to the data processor means, a memory including a battery backed, non-volatile RAM only and no ROM for storing (a) a set of instructions and (b) a library of code data for enabling the infrared light generating circuitry to generate specific infrared codes, the RAM being coupled to the data processor, and a data coupling device including terminals coupled to the CPU for enabling new code data to be supplied from outside the system to, or retrieved from, the RAM through the terminals and the CPU.

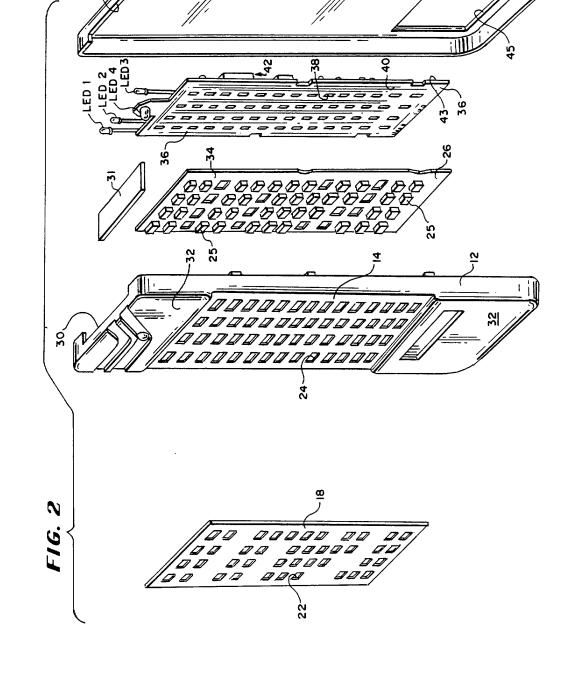
The RAM in the ROM-less data processing means is loaded by carrying out the following steps: (a) disabling the central processing unit; (b) connecting a separate microprocessor system to said RAM; (c) transferring instructions and/or data to said RAM; and (d) re-enabling the central processing unit to enable the central processing unit to execute the instructions so transferred.

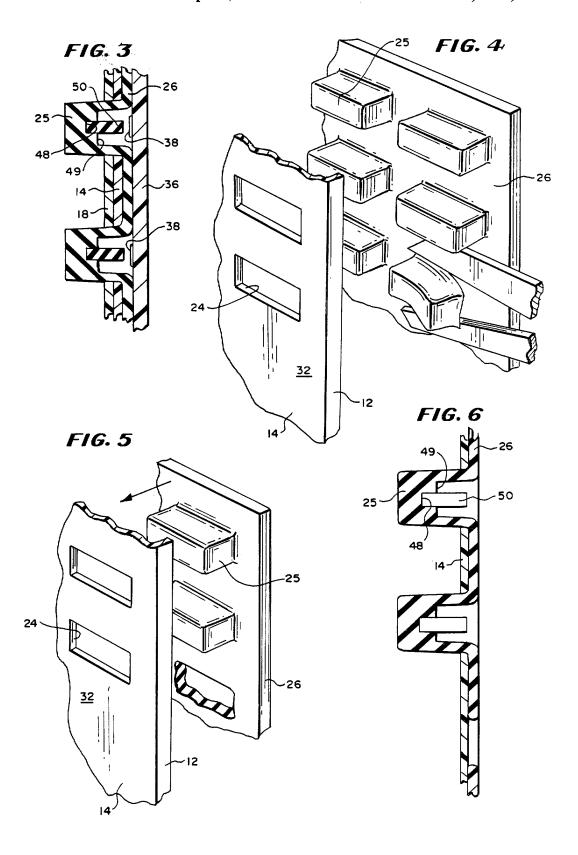
38 Claims, 17 Drawing Sheets

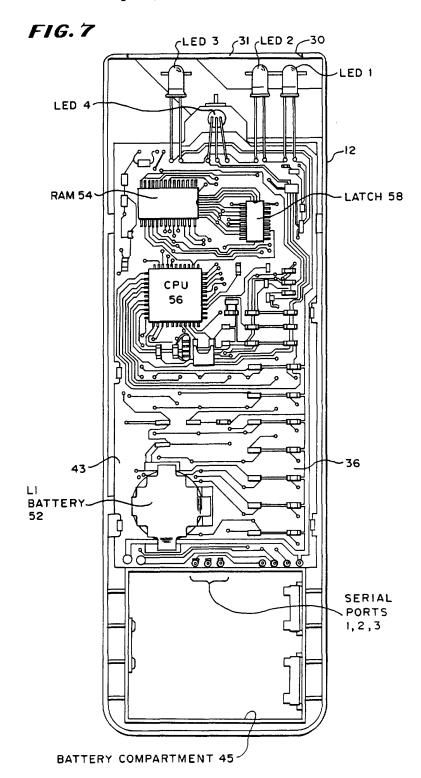












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