256 QAM Modem for Multicarrier 400 Mbit/s Digital Radio

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Abstract—**This paper describes the performance of a 256 QAM modem with 400 Mbit/s transmission capacity. A variety of novel techniques are introduced as ways to achieve good performance. Key techniques include 1) an accurate 256 QAM modulator employing a new monolithic multiplier IC, 2) a carrier recovery circuit which satisfies such requirements: good phase jitter performance and no false lock phenomenon, 3) a highly stable high-level decision circuit, and 4) a forward error correcting code. As an overall modem performance, BER characteristics and signatures are presented. The equivalent CNR degradations of 1 dB (at BER of 10^{-4}) and 2 dB (at BER of 10^{-9}) are obtained using a single Lee-error correcting code and a seven-tap baseband transversal equalizer. The residual bit errors are decreased below the order of 10^{-10}. The performance of a 256 QAM multicarrier modem has given prospect for the development of 400 Mbit/s digital microwave radio system.**

I. Introduction

ONE of the most important criteria in the design of digital radio systems is the transmission capacity per RF bandwidth, i.e., bits/second/Hertz. High-level modulation schemes for increasing spectrum utilization efficiency are now a major subject in the development of digital microwave radio. In recent years, several digital radio systems with 16 QAM, and even with as high as 64 QAM modulation have been developed and are in operation in the microwave frequency band [1]–[4]. The trend to increase spectrum utilization efficiency may continue [5].

As the modulation level increases, the system becomes more sensitive to multipath induced waveform distortion and interference noise. It was already demonstrated [8] that the multicarrier transmission method is effective for high-level modulation schemes in a multipath environment. On the basis of the above considerations, this paper describes a 256 QAM multicarrier modem for the 400 Mbit/s digital microwave radio (DM-400M) system [6], [7].

First, the performance of a newly developed monolithic multiplier IC for 256 QAM modulation and demodulation is described. Next, two principal techniques employed in a demodulator are stated. One is "a carrier recovery PLL with control mode selection function" which satisfies such requirements as good phase jitter performance and no false lock phenomenon. Another is "automatic gain and decision threshold control (AGTC) circuits." Due to these circuits, an excellent 256 QAM BER performance can be obtained. Forward error correction (FEC) is one of the key techniques for high-level modulation systems, because it eliminates residual bit errors. A single Lee-error correcting code with low redundancy is employed.

Finally, the 256 QAM BER performance, and signature with and without adjacent channel interference are presented. The equivalent CNR degradations of 1 dB at BER of 10^{-4} and of 2 dB at BER of 10^{-9} are obtained. The residual bit errors are decreased below the order of 10^{-10}.

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II. General Description

A. Outline of 256 QAM Four-Carrier Modem

For the realization of a digital radio system having a transmission capacity of 400 Mbits/s within 80 MHz bandwidth, a 256 QAM modulation using the Nyquist spectral shaping ($\alpha = 0.5$) is required. This enables the frequency utilization efficiency of 10 bits/s/Hz when the orthogonal dual polarization is employed.

In a high-level modulation system such as 64 QAM or 256 QAM, the multipath fading causes large degradation of BER performance. A multicarrier system is considered to be a promising method for high-level signal transmission in a fading channel. From the 256 QAM transmission characteristics estimation, a four-carrier system with 12.5 MBaud data rate and rolloff factor of 0.5 was found necessary to achieve 400 Mbits/s [8]. In this situation, the frequency spacing between adjacent carriers is 20 MHz and the radio channel is composed of four modems. The modem block-diagram and major system parameters are shown in Fig. 1 and Table I.

The transmitting terminal equipment converts 400 Mbit/s data into 32 rails of 12.5 MBaud binary signals. These 32 binary bit streams are fed to the four modulator circuitry. In each modulator, eight binary streams are differentially encoded (quadrant symmetry encoding) and redundant bits for error correcting are added by an FEC coder circuit. These streams are converted by D/A converters to form in-phase and quadrature 16 level signals. Each 16 level signal modulates a local oscillator. The 256 QAM signals with cosine rolloff spectrum shaping ($\alpha = 0.5$) are then combined by a hybrid circuit and supplied to the transmitter. The 256 QAM four-carrier spectrum is shown in Fig. 2.

At a demodulator, the 256 QAM four-carrier signals are

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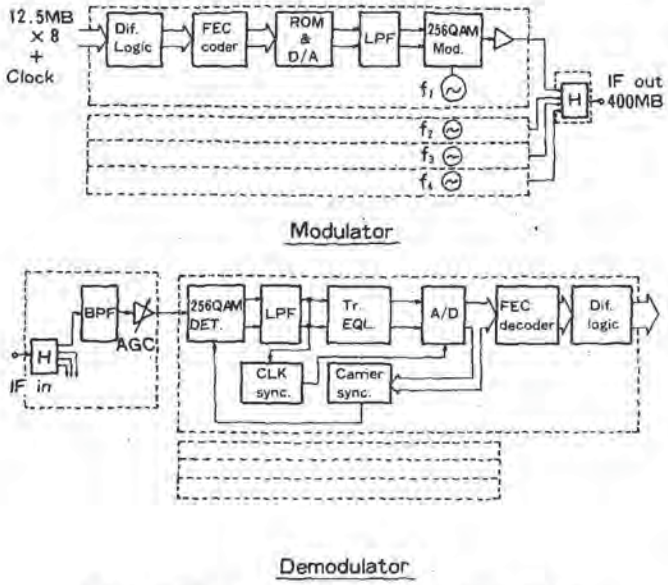

Fig. 1. Block diagram of 256 QAM four-carrier modem.

TABLE I
MAIN PARAMETERS OF 256 QAM 400 Mbit/s MULTICARRIER MODEM

Modulation /demodulation	256QAM-coherent detection
Transmission capacity	400Mb/s (4 carrier)
Symbol rate	12.5MB
Spectrum shaping	0.5 cosine roll-off
Spectrum utilization efficiency	10bits/s/Hz(※)

(※)with orthogonal dual polarization

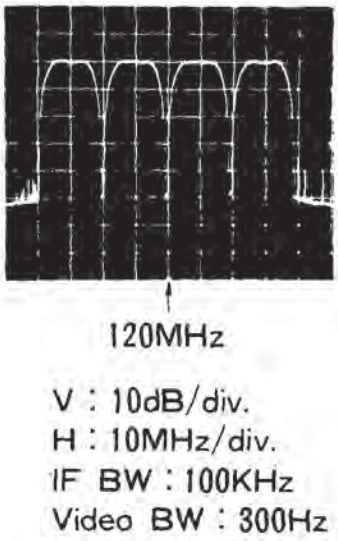

Fig. 2. Four-carrier spectrum.

distributed by a hybrid circuit and coherently detected to produce two orthogonal 16 level baseband signals. The seven-tap baseband transversal equalizers are employed to equalize both in-phase and quadrature waveform distortions. In order to improve pull-in performance, ZF (zero forcing) with MLE (maximum level error) algorithm is employed [6]. Demodulated 16 level signals are regenerated by A/D converters to produce eight rails of 12.5 MBaud binary signals. Error correction is then carried out in the FEC decoder circuit.

B. Key Techniques for an Accurate 256 QAM Modem

In order to realize an accurate 256 QAM modem, the following novel techniques are applied.

1) monolithic multiplier IC for the modulator and the phase detector,

2) high-level decision circuit with automatic gain and decision threshold control (AGTC circuit),

3) carrier recovery with control mode selection function,

4) forward error correction (FEC) technique.

III. CIRCUIT DESCRIPTION

A. Modulation Section

The degradation factors arising at various parts in a modem, such as waveform distortion, phase error, carrier jitter, etc., were categorized and the effects of these factors on 256 QAM equivalent CNR degradation were presented in [5]. Concerning the modulation section, it was revealed that the allowable maximum modulation phase error is $\pm 0.5°$ to satisfy the requirement for an equivalent CNR degradation of 0.6 dB at a BER of 10^{-6} for 256 QAM.

Therefore, a new monolithic multiplier IC capable of reducing the modulation phase and amplitude errors has been developed for the 256 QAM [9]. The main performance of the multiplier itself is presented in Table II. The new IC has a baseband input voltage linearity of more than 1.5 V and modulation phase error is less than 0.2°, which are extremely superior to the conventional ring modulators and to multiplier IC developed for a 16 QAM system. Third-order intermodulation products (IM3) of more than 55 dB at the average output power level is obtained. These performances are achieved with the aid of the latest device technology: SST (super self-aligned process technology) [10]. The modulation phase error ob-

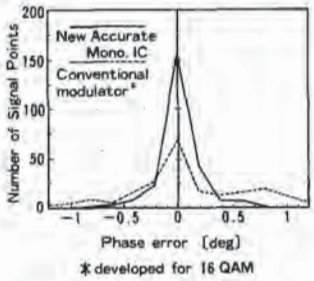

Fig. 3. Modulation phase error distributions comparing new monolithic IC and conventional modulator.

Fig. 4. 256 QAM signal constellation.

TABLE II
MONOLITHIC MULTIPLIER IC PERFORMANCE

modulation phase error	less than 0.2 degree
modulation amplitude error	less than 0.2dB
frequency characteristics	amplitude deviation between 100MHz and 180MHz is 0.4dB
baseband input linearity voltage	more than 1.5V
IM3 (third-order intermodulation products)	more than 55dB where the output back-off is 7dB
fabrication process	SST (Super Self-aligned process technology)

tained from the new monolithic multiplier IC and conventional one developed for a 16 QAM system are measured. Fig. 3 shows the number of signal points versus modulation phase error comparing the two multiplier IC's. The number of signal points of the quadrature multiplier with phase error of less than $\pm 0.5°$ are 238 by using the new monolithic IC's. The measured maximum phase error of less than $\pm 1°$ has been obtained.

It is concluded from experimental results that the newly developed monolithic multiplier IC almost satisfies the requirements for 256 QAM modulator. Fig. 4 shows the measured 256 QAM signal space diagram.

B. Demodulation Section

1) Carrier Recovery with Control Mode Selection Function: A variety of carrier tracking loops for the QAM signal have been proposed [11], [12]. One of the most effective methods for 16 QAM carrier recovery was a selective gated phase locked loop (PLL), which uses only the error signal derived from the same phases of a 4-PSK signal. The recovered carrier jitter of more than 35 dB for a 16 QAM signal was obtained by this method [11]. How-

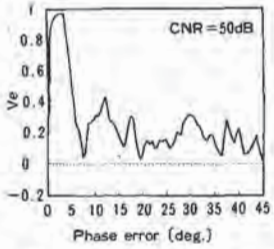

Fig. 5. Phase comparator characteristic.

ever, the required carrier jitter for 256 QAM is more than 45 dB when the equivalent CNR degradation of 0.3 dB is permitted. Therefore, it is necessary to design a carrier recovery circuit which satisfies such requirements: a) good phase jitter performance and b) no false lock phenomenon.

The received 256 QAM signal is demodulated into 16-level baseband signals at in-phase and quadrature channels. The regenerated first-bit signal sets (a_1, b_1), which are the most significant bit (MSB) of A/D converters, and the fifth-bit signal sets (a_5, b_5), which are error polarity signals, are multiplied and is used as the VCO control signal. The phase control voltage $V(\theta)$ is obtained as follows.

$$V(\theta) = \hat{a}_1 \hat{b}_5 - \hat{b}_1 \hat{a}_5. \tag{1}$$

The reduction of a PLL noise bandwidth and the improvement of VCO phase jitter are necessary to obtain a recovered carrier jitter of more than 45 dB. The carrier jitter of more than 45 dB has been achieved by designing RF local oscillator frequency stability of the order of 10^{-8} and employing a voltage controlled crystal oscillator (VCXO) in the demodulator. In spite of a good carrier jitter performance, it has been clarified from the phase comparator characteristic that the carrier recovery circuit has a false-lock point in the same frequency when input CNR is sufficiently high [5].

The selective gating of VCXO control signal during the course of an acquisition is effective in order to prevent the false-lock phenomenon.

After locking into a normal phase, the operation of selecting the control signal is inhibited. The switching is performed by monitoring the intersymbol interference which is easily estimated from the multiplication of the fifth and the sixth bits of A/D converter. This technique simultaneously enables the improvement of pull-in and carrier jitter performance.

The phase comparator characteristic in a selective gating mode is obtained as follows.

Let *Dsi* be the probability that the signal point i is involved in a selective area. *Dsi* is shown as

$$Dsi = \iint_{Rs \cup Es} Pi(x, y)\, dx\, dy \tag{2}$$

where, $Pi(x, y)$ is a Gaussian pdf $(i = 1 \sim 256)$.

$$Pi(x, y) = Pi(x) \cdot Pi(y)$$
$$= \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left\{-\frac{(x - Six)^2}{2\sigma^2}\right\} \cdot \exp\left\{-\frac{(y - Siy)^2}{2\sigma^2}\right\} \quad (3)$$

Six = in-phase component of signal point i
Siy = quadrature component of signal point i
σ^2 = white Gaussian noise power
2δ = minimum distance between signal points.

The average CNR (carrier to noise ratio) of 256 QAM can be obtained as

$$\text{CNR} = 85\,\delta^2/\sigma^2 = k_0^2. \quad (4)$$

In (2), Rs means the positive area producing correct control voltage "+1" and Es means the negative area producing error control voltage "−1." When the signal point i is involved in a selective area, the phase control voltage $Vi(\theta)$ is shown as

$$V_i(\theta) = \iint_{Rs} Pi(x, y)\,dx\,dy - \iint_{Es} Pi(x, y)\,dx\,dy. \quad (5)$$

When the signal point i is involved in a nonselective area, the phase control voltage $Vi(\theta)$ is put into "hold" condition by a sample and hold circuit. Then, the following equations are introduced.

$$Pe(\theta) = \sum_{i=1}^{256} \{V(\theta)\,Dsi + Pe(\theta)\,(1 - Dsi)\}/256$$

$Pe(\theta)$ = phase comparator characteristic. (6)

From (6), $Pe(\theta)$ can be written as

$$Pe(\theta) = \sum_{i=1}^{256} V(\theta) Dsi \Big/ \sum_{i=1}^{256} Dsi. \quad (7)$$

The phase comparator characteristic in a selective gating mode is shown in Fig. 5. The number of error signals used in the selective gating in Fig. 5 is 96 out of 256. Note that the loop exhibits no false lock point. The recovered carrier spectrum is shown in Fig. 6. The measured carrier jitter was 45.5 dB and the pull-in frequency range of more than 8 kHz was obtained.

2) High-Level Decision Circuit with Automatic Gain and Decision Threshold Control (AGTC): In order to achieve a good BER performance, an automatic gain and decision threshold control (AGTC) circuit is employed [14]. It uses the first and fifth bits of A/D converter as the feedback signals for the amplitude variation and dc drift of demodulated signals. These degradations are mainly caused by a local leak of the modulator, AGC level variation and temperature characteristic of amplifiers. The feedback signals are fed to the dc amplifier which is located before the A/D converter. Fig. 7 shows the circuit configuration.

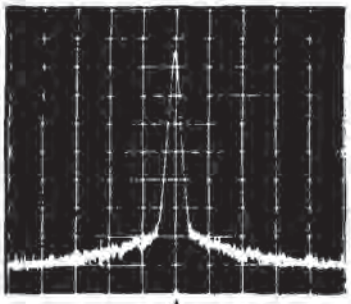

Fig. 6. Recovered carrier spectrum.

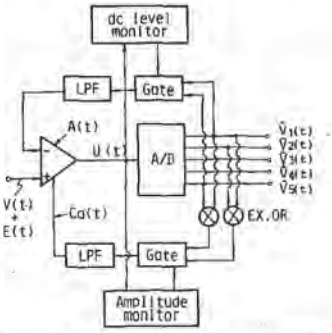

Fig. 7. Feedback circuit configuration.

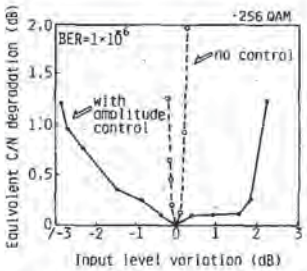

Fig. 8. Equivalent C/N degradation due to input level variation.

Let the input signal to the A/D converter be $u(t)$ and applying Laplacian "s" to $u(t)$, in dc drift compensation feedback loop [5]:

$$U(s) = V(s) + E(s)/(1 + Kd\,F(s)). \quad (8)$$

When $F(s)$ is supposed to be a perfect integrator,

$$F(s) = Ka/s, \quad (9)$$

then,

$$U(s) = V(s) + \frac{s}{s + Ka \cdot Kd} E(s). \quad (10)$$

In amplitude variation compensation feedback loop (see Appendix)

$$U(s) = V(s) + A(s)/mKg\,F(s) \qquad (11)$$

therefore, (11) becomes

$$U(s) = V(s) + \frac{s}{mKa \cdot Kg} A(s). \qquad (12)$$

where

$V(s)$ = 256 QAM demodulated signal
$E(s)$ = dc drift
$A(s)$ = amplitude variation
$F(s)$ = low-pass filter transmitting function
Kd, Kg = the linearized gain constants of the loop
m = gain constant of a dc amplifier.

The mathematical model of the feedback system indicated in (9), (10) has shown that it has a high-pass frequency characteristic for both amplitude variation and dc drift. The high-pass frequency characteristic of the feedback loops enables suppression of low frequency components of these degradations. Fig. 8 shows one experiment example of the input level variation compensation. This figure gives equivalent CNR degradation versus input level variation at BER of 10^{-6} for 256 QAM. Even a small level variation causes a large degradation in case of no control, while the CNR degradation is suppressed within 0.3 dB for the input level variation of ± 1 dB by employing the amplitude control.

A fifth bit of the A/D converter is used as the feedback signal for the dc drift compensation, and an exclusive-or output of a first and fifth bits is used for amplitude variation compensation. However it is revealed that, in both cases, if the dc drift or amplitude variation exceeds a half of the minimum distance between signal points, the compensated signal is locked to the incorrect voltage. Once the situations occur, burst bit errors are continually produced. This phenomenon is called "false-lock" and the calculation of the control voltage characteristics also prove its existences [5]. The dc level/amplitude monitor circuits and gate circuits shown in Fig. 7 are used to slip out from this "false-lock" situation. It is effective to change the feedback signals. For example, the first and fifth bits of the A/D converter are exchanged for the dc drift compensation and the exclusive-or output of the first and second bits is selected for the amplitude variation compensation once the "false-lock" occurs.

C. Forward Error Correction (FEC)

An application of FEC codes to high-level modulation systems greatly improves BER performance, particularly useful for the elimination of residual bit errors. Generally, in high-level modulation schemes, the symbol error probability between the adjacent symbols is much larger than that between the separate symbols. Therefore, it is effective to select an FEC code which can mainly correct the error propagations to adjacent symbols. The representative one is Lee-error correcting code [15]. The theoretical symbol error rate (SER) improvement due to the single Lee-error correcting code (72, 70) is shown as

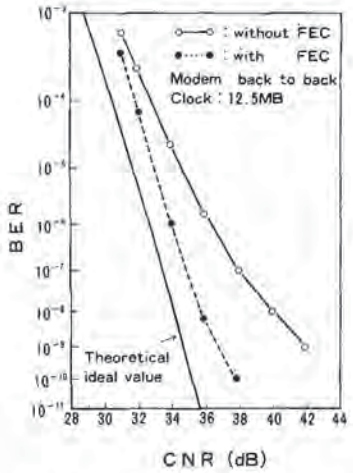

Fig. 9. 256 QAM BER performance.

$$Pe = 107 \cdot P^2 \qquad (13)$$

Pe = SER after FEC

P = SER before FEC.

The rate overhead of this code is only about 3 percent. The differential decoding is performed after error correction.

IV. Overall Performance

The 256 QAM signal has 16 baseband levels. The baseband signal is obtained by D/A converters as

$$S_1 = 2^3 \cdot a_1 + 2^2 \cdot a_2 + 2 \cdot a_3 + a_4$$

$$S_2 = 2^3 \cdot b_1 + 2^2 \cdot b_2 + 2 \cdot b_3 + b_4.$$

Signal sets $(a_1, b_1), \cdots (a_4, b_4)$ are binary codes and categorized as "Path 1" to "Path 4" indicating the first to fourth bit. The BER of 256 QAM is obtained as the average of the BER's of each path. Considering a quadrant symmetry differential encoding, the average BER of 256 QAM becomes

$$Pe = 19/64\ \mathrm{erfc}(\delta/\sqrt{2}\,\sigma)$$
$$= 19/64\ \mathrm{erfc}(k_0/\sqrt{170}) \qquad (14)$$

2δ = minimum distance between signal points,
σ^2 = white Gaussian noise power.

The 256 QAM BER's for Path 4 (modem back to back) are shown in Fig. 9. The single Lee-error correcting code and a seven-tap baseband transversal equalizer are implemented in this system. The equivalent CNR degradation of 1 dB (at a BER of 10^{-4}) and 2 dB (at a BER of 10^{-9}) are obtained. The measured coding gain by the FEC at a BER of 10^{-4} is about 2.5 dB. The residual bit errors have been reduced below the order of 1×10^{-10}. The demodulated eye pattern is presented in Fig. 10.

The overall filter system should be designed to minimize intersymbol and interchannel (adjacent carrier) in-

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