UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD. (TSMC),
Petitioner

v.

DSS TECHNOLOGY MANAGEMENT, INC.
Patent Owner

Patent 5,652,084

Title: METHOD FOR REDUCED PITCH LITHOGRAPHY

DECLARATION OF RICHARD A. BLANCHARD, PH.D.
UNDER 37 C.F.R. § 1.68

I, Richard Blanchard, do hereby declare:

1. I am making this declaration at the request of Taiwan Semiconductor Manufacturing Company, Ltd. ("TSMC") in the matter of the *Inter Partes* Review of U.S. Patent No 5,652,084 ("the '084 Patent") to James M. Cleeves.

2. In the preparation of this declaration, I have studied:

(1) The '084 Patent, TSMC-1001;

(2) The prosecution history of the '084 Patent, TSMC-1002;

(3) U.S. Patent No. 5,710,061 ("Cleeves II"), TSMC-1003;

(4) Japanese Patent App. No. 04-71222 ("Jinbo"), TSMC-1004;

(5) U.S. Patent No. 4,591,547 ("Brownell"), TSMC-1005;

(6) U.S. Patent No. 4,931,351 ("McColgin"), TSMC-1006;

(7) U.S. Patent No. 4,548,688 ("Matthews"), TSMC-1007; and

(8) U.S. Patent No. 5,158,910 ("Cooper"), TSMC-1008.

3. In forming the opinions expressed below, I have considered:

(1) The documents listed above, and

(2) My knowledge and experience based upon my work in this area as described below.

4. I am familiar with and am a practitioner of the technology at issue and am aware of the state of the art at the time the application resulting in the '084 Patent was filed. The earliest priority date is December 22, 1994. Based on the technologies disclosed in the '084 Patent, I believe that one of ordinary skill in the art would include someone who has a B.S. degree in Electrical Engineering, Material Science, or Physics, or equivalent training, as well as 3-5 years of experience in the field of integrated circuit (IC) design, IC fabrication, and lithographic fabrication techniques. Unless otherwise stated, when I give my understanding and analysis below, it is consistent with the level of one of ordinary skill in these technologies at and around the filing date of the '084

patent.

I. QUALIFICATIONS

5. I am a consultant for Thomson Reuters Expert Witness Services (formerly known as Silicon Valley Expert Witness Group), a consulting company specializing in expert witness litigation support and technology consulting. I also provide technical consulting services to the semiconductor and electronics industry through Blanchard Associates.

6. My academic credentials include both a Bachelor of Science Degree in Electrical Engineering (BSEE) and a Master of Science Degree in Electrical Engineering (MSEE) from the Massachusetts Institute of Technology in 1968 and 1970, respectively. I subsequently obtained a Ph.D. in Electrical Engineering in 1982 from Stanford University.

7. My professional background and technical qualifications are stated above and are also reflected in my *Curriculum Vitae,* which is attached as TSMC-1010. I am being compensated at a rate of $275.00 per hour, with reimbursement for actual expenses, for my work related to this Petition for *Inter Partes* Review. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration.

8. I have worked or consulted for more than 40 years as an Electrical Engineer. My primary focus has been on the development,

manufacture, operation, and use of devices and integrated circuits, the assembly of these devices and integrated circuits, products that use them, and their failures. My employment history following my graduation from MIT began at Fairchild Semiconductor in 1970. At Fairchild, my responsibilities included circuit and device design, process development, and product engineering in the Linear Integrated Circuits Department.

9. In 1974, I joined Foothill College as an Associate Professor in the Engineering & Technology Division. My responsibilities included developing a program in Semiconductor Technology as well as teaching other courses in the division. While at Foothill College, I co-founded two companies, Cognition and Supertex, and later joined Supertex as a Vice President in 1978. At Supertex, I designed and developed discrete DMOS (double-diffused metal oxide semiconductor) transistors, as well as integrated circuits that contained DMOS transistors. At Supertex, I also supervised the in-house assembly area, which included responsibility for the associated manufacturing processes.

10. I left Suptertex to join Siliconix in 1982, where I soon became Vice President of Engineering, with the responsibility for directing all of the company's product design and development. At Siliconix, I directed and contributed to the development of both discrete transistors and integrated

circuits, including aspects of their assembly.

11. In 1987, I joined IXYS Corporation as a Senior Vice President with the responsibility for organizing an integrated circuit department. At IXYS, I developed integrated circuits that contained DMOS devices or that interfaced to DMOS devices. My responsibilities included the design, assembly, and testing of these integrated circuits.

12. These duties continued until 1991, when I left IXYS to set up Blanchard Associates, a consulting firm specializing in semiconductor technology, including intellectual property. Soon thereafter, I was invited to join Failure Analysis Associates, which I did in late 1991. At Failure Analysis Associates, I investigated failures in electrical and electronic systems in addition to performing design and development consulting.

13. I left Failure Analysis in 1998 to join IP Managers, which later merged with Silicon Valley Expert Witness Group, now known as Thomson Reuters Expert Witness Services ("Thomson Reuters"). At Thomson Reuters, I work with companies on patent and trade secret matters. I also consult for a number of semiconductor companies, working with them to develop products and intellectual property, or assisting them in other technical areas through Blanchard Associates. Design and Development projects that I have worked on range from the design and evaluation of

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