UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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EMC CORPORATION AND VMWARE, INC.
Petitioner

v.

PERSONALWEB TECHNOLOGIES LLC
Patent Owner

_____

Case IPR2013-00083 (JYC)
U.S. Patent No. 6,415,280

_____

Before KEVIN F. TURNER, JONI Y. CHANG, and
MICHAEL R. ZECHER, *Administrative Patent Judges*.

ZECHER, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

EMC Corporation and VMware, Inc. ("EMC") filed a petition ("Pet.") requesting *inter partes* review of claims 36 and 38 of U.S. Patent No. 6,415,280 ("the '280 patent"). Paper No. 6. Patent owner, PersonalWeb Technologies LLC ("PersonalWeb"), filed a preliminary response ("Prelim. Resp."). Paper No. 14. We have jurisdiction under 35 U.S.C. § 314.

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides:

> THRESHOLD --The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Taking into account PersonalWeb's Preliminary Response, we conclude that the information presented in the Petition demonstrates that there is a reasonable likelihood that EMC will prevail in challenging claims 36 and 38 as unpatentable under 35 U.S.C. §§ 102 and 103. Pursuant to 35 U.S.C. § 314, we hereby authorize an *inter partes* review to be instituted as to claims 36 and 38 of the '280 patent.

A. Related Matters

EMC indicates that the '280 patent was asserted against it in *PersonalWeb Technologies LLC v. EMC Corporation and VMware, Inc.*, Case No. 6:11-cv-00660-LED, pending in the U.S. District Court for the Eastern District of Texas. Pet. 1. EMC also filed five other Petitions

seeking *inter partes* review of the following patents: U.S. Patent No. 5,978,791 (IPR2013-00082), U.S. Patent No. 7,945,544 (IPR2013-00084), U.S. Patent No. 7,945,539 (IPR2013-00085), U.S. Patent No. 7,949,662 (IPR2013-00086), and U.S. Patent No. 8,001,096 (IPR2013-00087). *Id*. According to EMC, those patents and the '280 patent share a common disclosure. *Id*. (citing to Ex. 1008).

B. The Invention of the '280 Patent (Ex. 1001)

The invention of the '280 patent relates to a data processing system that identifies data items using substantially unique identifiers, otherwise referred to as True Names, which depend on all the data in the data item and only on the data in the data item. Ex. 1001, Spec. 1:12-16, 3:28-31, and 6:7-9. According to the '280 patent, the identity of a data item depends only on the data and is independent of the data item's name, origin, location, address, or other information not directly derivable from the data associated therewith. Ex. 1001, Spec. 3:32-34. The invention of the '280 patent also examines the identities of a plurality of data items in order to determine whether a particular data item is present in the data processing system. Ex. 1001, Spec. 3:35-38.

Figures 1(a) and 1(b) illustrate the data processing system that implements the invention of the '280 patent. Ex. 1001, Spec. 4:45-47. Figure 1(a) is reproduced below.
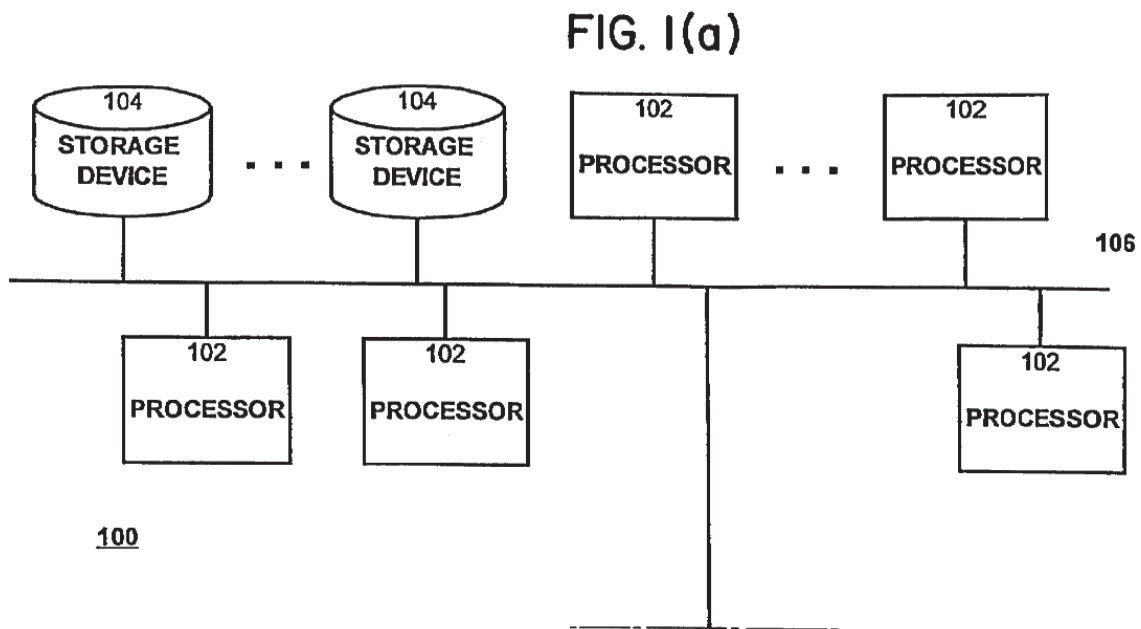
FIG. I(a)

Figure 1(a) illustrates the data processing system 100.

The Specification of the '280 patent discloses that the data processing system 100 includes one or more processors 102 and various storage devices 104 connected via bus 106. Ex. 1001, Spec 4:59-64.
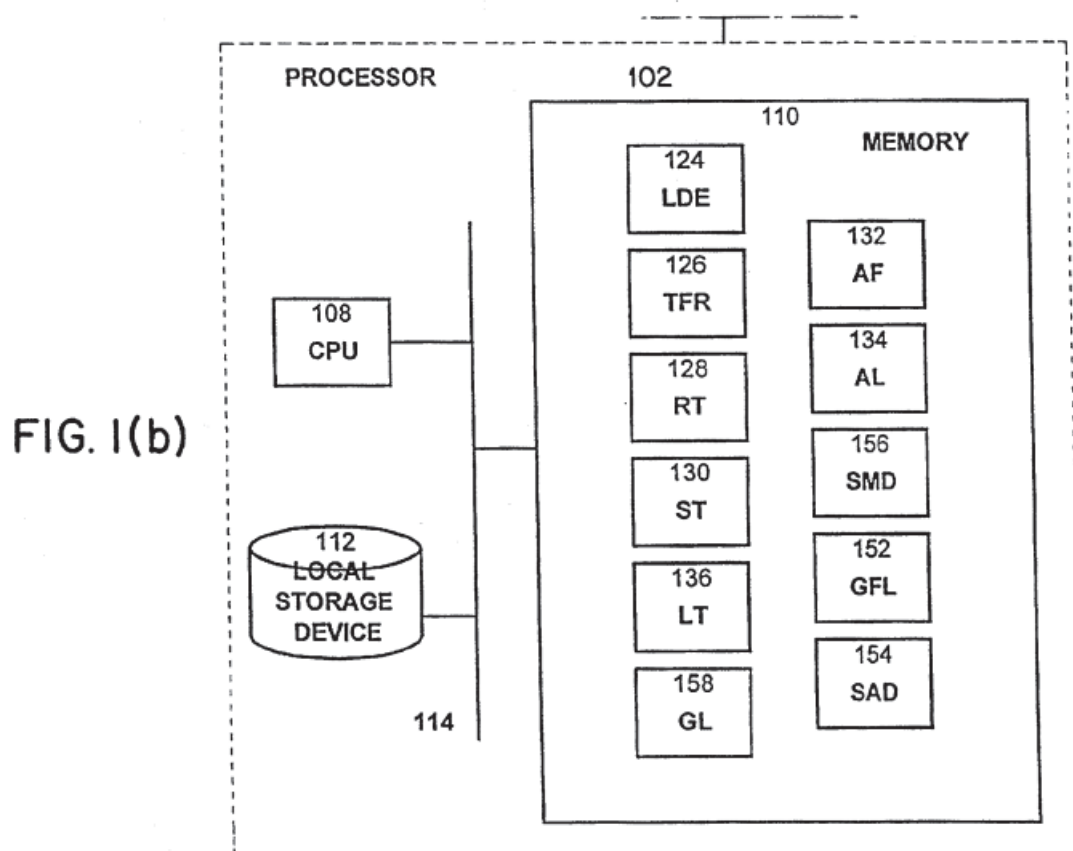
Figure 1(b) is reproduced below.

FIG. I(b)

**Figure 1(b) illustrates a typical data processor 102
in the data processing system 100.**

The Specification of the '280 patent discloses that each processor 102 includes a central processing unit 108, memory 110, and one or more local storage devices 112 connected via an internal bus 114. Ex. 1001, Spec. 4:65-5:1. The memory 110 in each processor 102 stores data structures that are either local to the processor itself or shared amongst multiple processors in the data processing system. Ex. 1001, Spec. 7:65-8:13.

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