# Robert W. Horst, Ph.D.

## Expertise

- Computer design and architecture
- Fault tolerant computing
- CPU, cache and memory design
- I/O and storage subsystems
- High speed networks
- Performance evaluation
- Hardware testing
- Patents and intellectual property

## Professional Summary

From: 2001 HT Consulting
To: Present San Jose, CA
Position: Independent consultant

- Work with startups, VC firms, established companies and law firms on architectural definition of new products, design reviews, technical due diligence on potential investments, identification and protection of intellectual property and litigation support.
- Expert witness in patent and technology litigation

From: 2013 AlterG
To: Present Fremont, CA
Position: Chief Technology Officer, Robotics

- Tibion was acquired by AlterG in April, 2013.
- Leading development of AlterG Bionic Leg and future products

From: 2001 Tibion Corporation
To: 2013 Sunnyvale, CA
Position: Founder / VP of R&D / CTO

- Inventor of the Tibion Bionic Leg, the first wearable robotic device for assistance and rehabilitation of those with impaired mobility.
- Investigate product and technology options
- Develop electronics, software and mechanics for several generations of prototypes and products
- Design and test production electronics and control algorithms
- Formulate and execute IP strategy

From: 2002 Network Appliance, Inc.
To: 2003 Sunnyvale, CA
Position: Technical Director

- Investigate processor and interconnect options for future generations of network-attached storage subsystems.
- Represent Network Appliance in the PCI Express Advanced Switching working group.

From: 1999 3ware, Inc.
To: 2001 Mountain View, CA
Position: Vice President, Research & Technology

- Initiate and lead project that resulting in industry's first Ethernet Storage Area Network storage subsystem. Enhance the company's patent position with 10 new patent applications.
- Develop novel disk mirroring architecture and help the company to grow from 15 to over 100 people. Participate in fund raising activities and prototype development.

From: 1980 Tandem Computers / Compaq Computers
To: 1999 Cupertino, CA
Position: Technical Director

- Designer and architect of several generations of fault-tolerant mainframes used in banking, stock exchanges, and commerce.
- Co-founder of Tandem Labs. Initiated internal projects and started several joint research projects with universities,
- Lead architect of the ServerNet System Area Network. Internal and external champion of ServerNet. Wrote technical papers and made numerous presentations to technical audiences and customers
- Principal architect of the NonStop Cyclone superscalar processor. Listed inventor on the industry's first superscalar patents.
- Project leader of NonStop TXP fault-tolerant CPU.

From: 1976 Hewlett-Packard Co.
To: 1980 Cupertino, CA
Position: Development Engineer

- Designed the micro-sequencer and cache of the HP3000 Series 64 processor.
- Designed a test system for the processor cards using pseudo-random scan and signature analysis.

## Litigation Support Experience

Served as a testifying and consulting expert witness on patent cases related to systems, processors and storage. Served as a consulting expert on class-action and defective product cases. Further details furnished on request.

## Patents

| # | PAT. NO. | TITLE |
|---|---|---|
| 77 | 8,639,455 | Foot pad device and method of obtaining weight data |
| 76 | 8,353,854 | Methods and devices for moving a body joint |
| 75 | 8,274,244 | Actuator system and method for extending a joint |
| 74 | 8,058,823 | Actuator system with a multi-motor assembly for extending and flexing a joint |
| 73 | 7,811,189 | Deflector Assembly |
| 72 | 7,648,436 | Rotary Actuator |
| 71 | 7,537,573 | Active muscle assistance device and method |
| 70 | 7,521,836 | Electrostatic actuator with fault tolerant electrode structure |
| 69 | 7,484,038 | Method and apparatus to manage storage devices |
| 68 | 7,468,982 | Method and apparatus for cluster interconnection using multi-port nodes and multiple routing fabrics |
| 67 | 7,365,463 | High torque motor |
| 66 | 7,239,065 | Electrostatic actuator with fault tolerant electrode structure |
| 65 | 6,966,882 | Active muscle assistance device and method |
| 64 | 6,950,428 | System and method for configuring adaptive sets of links between routers in a system area network (SAN) |
| 63 | 6,924,780 | Spatial display of disk drive activity data |
| 62 | 6,775,794 | Use of activity bins to increase the performance of disk arrays |
| 61 | 6,753,878 | Parallel pipelined merge engines |
| 60 | 6,751,757 | Disk drive data protection using clusters containing error detection sectors |
| 59 | 6,650,533 | Pluggable drive carrier assembly |
| 58 | 6,646,984 | Network topology with asymmetric fabrics |
| 57 | 6,631,131 | Transpose table biased arbitration scheme |
| 56 | 6,591,339 | Methods and systems for selecting block sizes for use with disk arrays |
| 55 | 6,591,338 | Methods and systems for mirrored disk arrays |
| 54 | 6,567,892 | Use of activity bins to increase the performance of disk arrays |
| 53 | 6,549,977 | Use of deferred write completion interrupts to increase the performance of disk operations |
| 52 | 6,516,032 | First-order difference compression for interleaved image data in a high-speed image compositor |
| 51 | 6,496,940 | Multiple processor system with standby sparing |
| 50 | 6,487,633 | Methods and systems for accessing disks using forward and reverse seeks |

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|---|---|---|
| 49 | 6,484,235 | Methods and systems for dynamically distributing disk array data accesses |
| 48 | 6,424,655 | Transpose table-biased arbitration |
| 47 | 6,424,523 | Pluggable drive carrier assembly |
| 46 | 6,266,765 | Computer architecture capable of execution of general purpose multiple instructions |
| 45 | 6,233,702 | Self-checked, lock step processor pairs |
| 44 | 6,157,967 | Method of data communication flow control in a data processing system using busy/ready commands |
| 43 | 6,092,177 | Computer architecture capable of execution of general purpose multiple instructions |
| 42 | 6,009,506 | Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions |
| 41 | 5,964,835 | Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source |
| 40 | 5,930,275 | Clock error detection circuit |
| 39 | 5,918,032 | Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions |
| 38 | 5,914,953 | Network message routing using routing table information and supplemental enable information for deadlock prevention |
| 37 | 5,890,003 | Interrupts between asynchronously operating CPUs in fault tolerant computer system |
| 36 | 5,867,501 | Encoding for communicating data and commands |
| 35 | 5,838,894 | Logical, fail-functional, dual central processor units formed from three processor units |
| 34 | 5,765,007 | Microinstruction sequencer having multiple control stores for loading different rank registers in parallel |
| 33 | 5,758,113 | Refresh control for dynamic memory in multiple processor system |
| 32 | 5,752,064 | Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions |
| 31 | 5,751,932 | Fail-fast, fail-functional, fault-tolerant multiprocessor system |
| 30 | 5,742,135 | System for maintaining polarity synchronization during AMI data transfer |
| 29 | 5,710,549 | Routing arbitration for shared resources |
| 28 | 5,694,121 | Latency reduction and routing arbitration for network message routers |
| 27 | 5,675,579 | Method for verifying responses to messages using a barrier message |
| 26 | 5,628,024 | Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions |
| 25 | 5,574,941 | Computer architecture capable of concurrent issuance and execution of general purpose multiple instruction |
| 24 | 5,574,933 | Task flow computer architecture |
| 23 | 5,404,550 | Method and apparatus for executing tasks by following a linked list of memory packets |

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|---|---|---|
| 22 | 5,390,355 | Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions |
| 21 | 5,384,906 | Method and apparatus for synchronizing a plurality of processors |
| 20 | 5,353,436 | Method and apparatus for synchronizing a plurality of processors |
| 19 | 5,329,629 | Apparatus and method for reading, writing, and refreshing memory with direct virtual or physical access |
| 18 | 5,317,726 | Multiple-processor computer system with asynchronous execution of identical code streams |
| 17 | 5,287,472 | Memory system using linear array wafer scale integration architecture |
| 16 | 5,239,641 | Method and apparatus for synchronizing a plurality of processors |
| 15 | 5,203,005 | Cell structure for linear array wafer scale integration architecture with capability to open boundary I/O bus without neighbor acknowledgement |
| 14 | 5,193,175 | Fault-tolerant computer with three independently clocked processors asynchronously executing identical code that are synchronized upon each voted access to two memory modules |
| 13 | 5,146,589 | Refresh control for dynamic memory in multiple processor system |
| 12 | 5,075,844 | Paired instruction processor precise exception handling mechanism |
| 11 | 5,072,364 | Method and apparatus for recovering from an incorrect branch prediction in a processor that executes a family of instructions in parallel |
| 10 | 5,034,964 | N:1 time-voltage matrix encoded I/O transmission system |
| 9 | 5,016,208 | Deferred comparison multiplier checker |
| 8 | 4,872,109 | Enhanced CPU return address stack |
| 7 | 4,823,252 | Overlapped control store |
| 6 | 4,800,486 | Multiple data patch CPU architecture |
| 5 | 4,754,396 | Overlapped control store |
| 4 | 4,636,943 | Enhanced CPU microbranching architecture |
| 3 | 4,618,956 | Method of operating enhanced alu test hardware |
| 2 | 4,574,344 | Entry control store for enhanced CPU pipeline performance |
| 1 | 4,571,673 | Enhanced CPU microbranching architecture |

## Education

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|---|---|---|
| 1991 | University of Illinois | Ph.D., Computer Science. Design and simulation of a massively parallel, multi-threaded *task flow* computer. |
| 1978 | University of Illinois | M.S., Electrical Engineering. Design, construction and debugging of a shared memory parallel microprocessor system. |
| 1975 | Bradley University | B.S., Electrical Engineering. Summa Cum Laude. |

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