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Paper 60
Entered: February 19, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SYNOPSYS, INC.
Petitioner

v.

MENTOR GRAPHICS CORPORATION
Patent Owner

Case IPR2012-00042
Patent 6,240,376 B1

Before HOWARD B. BLANKENSHIP, SALLY C. MEDLEY, and JENNIFER S. BISK, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION

35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background

Petitioner, Synopsys, Inc. ("Synopsys"), filed a petition on September 26, 2012, for *inter partes* review of claims 1-15 and 20-33 of U.S. Patent No. 6,240,376 B1 ("the '376 Patent") pursuant to 35 U.S.C. §§ 311-319. Paper 1 ("Pet."). Patent Owner, Mentor Graphics Corporation ("Mentor Graphics"), filed a preliminary response on December 28, 2012. Paper 15 ("Prelim. Resp."). On February 22, 2013, the Board denied the petition as to claims 10, 12-15, 20-27, and 30-33, and instituted trial for claims 1-9, 11, 28, and 29, on one ground of unpatentability, anticipation by U.S. Patent No. 6,132,109 ("Gregory") (Ex. 1007). Paper 16 ("Decision to Institute").

After institution of trial, Mentor Graphics filed a patent owner response. Paper 28 ("PO Resp."). Mentor Graphics also filed a substitute motion to amend claims by submitting proposed new claims 34-43 for claims 1, 5, 28, 2, 3, 6, 8, 9, 11, and 29, respectively. Paper 31 ("Mot. to Amend"). Synopsys filed a reply to the patent owner response (Paper 36; "Reply"), and also an opposition to Mentor Graphics's motion to amend (Paper 35; "Opp."). Mentor Graphics then filed a reply in support of its motion to amend. Paper 39 ("Reply Mot. to Amend").

In preparation for oral hearing, both parties filed and fully briefed motions to exclude. Paper 42 ("Mentor Graphics's Motion to Exclude"); Paper 44 ("Synopsys's Motion to Exclude"). Oral hearing was held November 14, 2013. Paper 59 ("Transcript").

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written decision is issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73.

Synopsys has shown that claims 5, 8, and 9 are unpatentable. Synopsys, however, has not met its burden to show by a preponderance of the evidence that claims 1-4, 6, 7, 11, 28, and 29 are unpatentable.

Mentor Graphics's motion to amend claims is *denied.*

B. The '376 Patent

The '376 patent generally relates to the fields of simulation and prototyping of integrated circuits. Ex. 1001, col. 1, ll. 10-11. In particular, the patent describes "debugging synthesizable code at the register transfer level during gate-level simulation." *Id.* at ll. 11-13.

As described in the Background of the Invention, integrated circuit design begins with a description of the behavior desired in a hardware description language ("HDL") such as Very High Speed Integrated Circuit Description Language ("VHDL"). *Id.* at ll. 14-25. A subset of HDL source code is referred to as Register Transfer Level ("RTL") source code. *Id.* at ll. 28-30. This RTL source code can be simulated using software, which typically offers robust debugging functionality for analyzing and verifying the design, including navigating the design hierarchy, viewing the RTL source code, setting breakpoints on a statement of RTL source code to stop the simulation, and viewing and tracing variables and signal values. *Id.* at ll. 44-54. However, although flexible, software RTL simulators are slow compared with hardware emulation. *Id.* at ll. 55-63. Thus, it often is desirable to use gate-level simulation to verify complex designs. *Id.*

The RTL description of a circuit can be used by synthesis tools to generate a "gate-level netlist," which, in turn, can be converted to a format suitable for programming a hardware emulator. *Id.* at ll. 35-42. A gate-level netlist represents the circuit to be simulated and ultimately is comprised of

combinatorial or sequential logic gates (e.g. AND, NAND, and NOR gates, or flip-flops and latches) and a description of their interconnections using signals (signals are also referred to as nets). *Id.* at col. 4, ll. 5-17. As discussed, gate-level simulation is useful for validation of a circuit design. *Id.* at col. 1, ll. 55-67. However, one disadvantage of gate-level simulation is that much of the high-level information from the RTL source code is lost during synthesis, resulting in debugging functionality that is limited severely in comparison with that available in software RTL simulation. *Id.* at col. 2, ll. 1-23.

The '376 patent describes a method of synthesizing RTL source code such that the resulting gate-level simulation can support the traditional debugging tools of setting breakpoints, mapping signal values to particular source code lines, and stepping through the source code to trace variable values. *Id.* at ll. 1-30. The Summary of the Invention describes facilitating debugging during gate-level simulation by: (1) generating "instrumentation logic indicative of the execution status of at least one synthesizable statement within the RTL source code"; (2) generating a gate-level netlist from the RTL source code; and (3) during simulation, evaluating the instrumentation logic of the gate-level netlist to enable RTL debugging. *Id.* at ll. 26-39.

The '376 patent describes two main embodiments for implementing this method. The first embodiment modifies the gate-level netlist to provide instrumentation signals "implementing the instrumentation logic and corresponding to synthesizable statements within the RTL source code." *Id.* at ll. 40-43. This modification of the gate-level netlist can be done either by modifying the RTL source code directly or by generating the modified gate-

level netlist during synthesis. *Id.* at ll. 43-46. The second embodiment ("the cross-reference embodiment") describes storing the instrumentation signals in a cross-reference database instead of modifying the gate-level netlist. *Id.* at ll. 47-52.

Figure 2 of the '376 patent, reproduced below, illustrates "one embodiment of the instrumentation process in which instrumentation is integrated with the synthesis process." *Id.* at col. 5, ll. 9-11.

FIG. 2

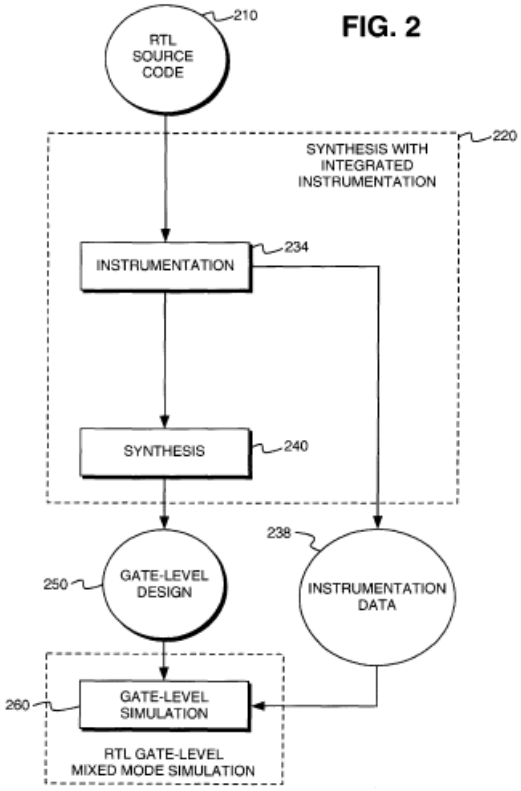

Figure 2, above, shows that RTL source code 210 is provided to synthesis process 220, which includes instrumentation step 234 followed by synthesis step 240. *Id.* at ll. 11-16. In the first embodiment, in which the gate level netlist is modified to include instrumentation signals, the resulting gate-level design 250 "contains additional logic to create the additional instrumentation output signals referenced in instrumentation data 238." *Id.* at ll. 17-30.

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