THOMAS MARTIN CONTE

CURRICULUM VITAE

POSITIONS HELD

Professor, School of Electrical and Computer Engineering, College of Engineering, and Professor, School of Computer Science, College of Computing (*joint appointment*) Georgia Institute of Technology	7/08 – *present*
Professor, Department of Electrical and Computer Engineering North Carolina State University	8/02 – 7/08
Director, Center for Efficient, Scalable and Reliable Computing North Carolina State University	1/07 – 7/08
Director, Center for Embedded Systems Research North Carolina State University	1/01 – 12/06
Chief Microarchitect and Manager, Back End Compiler Development BOPS, Inc. (VLIW DSP startup, while on leave from NCSU for AY00-01)	6/00 – 6/01
Voting member, EDN Embedded Benchmarking Consortium BOPS, Inc.	6/00 – 6/01
Associate Professor, Department of Electrical and Computer Engineering North Carolina State University	7/98 – 7/02
Assistant Professor, Department of Electrical and Computer Engineering North Carolina State University	8/95 – 8/98
Assistant Professor, Department of Electrical and Computer Engineering University of South Carolina	8/92 – 8/95

EDUCATION

Doctor of Philosophy, Electrical Engineering, University of Illinois, Urbana-Champaign: 1992
Master of Science, Electrical Engineering, University of Illinois, Urbana-Champaign: 1988
Bachelor of Electrical Engineering, University of Delaware: 1986

HONORS

- IEEE Fellow (citation: "*for contributions to computer architecture, compiler code generation and performance evaluation*")
- Young Alumni Achievement Award, Dept. of ECE, University of Illinois at Urbana-Champaign, 2004
- National Science Foundation Faculty Early Career Development (CAREER) Award, 1996
- IBM Partnership Award for Faculty Development, 1995, 1996
- Professional societies: *IEEE (fellow), ACM (member)*
- Honor societies: *Tau Beta Pi* (engineering), *Eta Kappa Nu* (electrical engineering)
- While a student: President of *University of Delaware IEEE Student Branch*, 1985; University of Delaware *Engineering Scholar*

PUBLICATION HISTORY

BOOKS

[1] T. M. Conte and C. E. Gimarc, eds., *Fast Simulation of Computer Architectures,* Kluwer Academic Publishers: Boston, MA 7 1995, ISBN 0-7923-9593-X.

BOOK CHAPTERS

[1] T. M. Conte and K. N. P. Menezes, "The effects of traditional compiler optimizations on superscalar architectural design," in *The Interaction of Compilation Technology and Computer Architecture* (D. J. Lilja and P. L. Bird, eds.), Kluwer Academic Publishers: Boston, MA, 1994, pp. 119-136.

[2] T. M. Conte and W. W. Hwu, "Advances in benchmarking techniques: New standards and quantitative metrics," in *Advances in Computers,* vol. 41, (M. V. Zelkowitz, ed.), Academic Press: New York, 1995.

[3] T. M. Conte, "Superscalar and VLIW Processors," *in Handbook of Parallel and Distributed Computing*, (A.-Y. Zomaya, ed.), McGraw-Hill: New York, 1995.

[4] T. M. Conte, "Superscalar and VLIW processors (instruction-level parallelism)", *Encyclopedia of Electrical and Electronics Engineering* (J. G. Webster, ed.), John Wiley & Sons: New York, NY, 1998.

[5] T. M. Conte and P. D. Bryan, "Statistical sampling for processor and cache simulation," *Performance Evaluation and Benchmarking,* (L. John and L. Eeckhout, eds.), CRC Press, 2006.

[6] T. M. Conte, "Appendix D: Embedded systems," *in Computer Architecture: A Quantitative Approach, 4th ed. (J. Hennessy and D. Patterson)*, Morgan-Kaufmann: San Francisco, 2006.

JOURNAL PAPERS

[1] T. M. Conte and W. W. Hwu, "Benchmark characterization," *IEEE Computer,* pp. 48-56, Jan. 1991.

[2] W. Y. Chen, P. P. Chang, T. M. Conte and W. W. Hwu, "The effect of code expanding optimizations on instruction cache design," *IEEE Transactions on Computers*, vol. C-42, no. 9, pp. 1045-1057, Sep. 1993.

[3] W. W. Hwu and T. M. Conte, "The susceptibility of programs to context switching," *IEEE Transactions on Computers*, vol. C-43, no. 9, pp. 993-1003, Sep. 1994.

[4] T. M. Conte, B. A. Patel, K. N. Menezes and J. S. Cox, "Hardware-based profiling: An effective technique for profile-driven optimization," *International Journal of Parallel Programming*, vol. 24, no. 2, Feb. 1996.

[5] T. M. Conte and S. W. Sathaye, "Optimization of VLIW object code compatibility systems employing dynamic rescheduling*," International Journal of Parallel Programming*, vol. 25, no. 2, Feb. 1997.

[6] T. M. Conte, P. K. Dubey, M. D. Jennings, R. B. Lee, S. Rathnam, M. Schlansker, P. Song, A. Wolfe, "Challenges to combining general-purpose and multimedia processors into one package," *IEEE Computer,* vol. 30, no. 12, Dec. 1997.

[7] M. Schlansker, T. M. Conte, J. Dehnert, K. Ebcioglu, J. Fang, C. Thompson, "Compiling for Instruction-Level Parallelism," *IEEE Computer,* vol. 30, no. 12, Dec. 1997.

[8] P. Bose and T. M. Conte, "Performance analysis and its impact on design", *IEEE Computer,* vol. 31, no. 5, May 1998.

[9] T. M. Conte, M. A. Hirsch, and W. W. Hwu, "Combining trace sampling with single pass methods for efficient cache simulation," *IEEE Transactions on Computers*, vol. C-47, no. 6, Jun. 1998.

[10] S. Banerjia, S. W. Sathaye, K. N. Menezes and T. M. Conte, "MPS: Miss path scheduling for multiple-issue processors," *IEEE Transactions on Computers*, vol. C-47, no. 12, Dec. 1998.

[11] M. D. Jennings and T. M. Conte, "Subword extensions for video processing on mobile systems," *IEEE Concurrency*, July-September, 1998, pp. 13-16.

[12] P. Bose, T. M. Conte, T. M. Austin, "Challenges in processor modeling and validation," *IEEE Micro*, May-June, 1999, pp. 2-6.

[13] T. M. Conte, S. W. Sathaye, K. N. Menezes, and M. C. Toburen "System-level power consumption modeling and tradeoff analysis techniques for superscalar processor design," *IEEE Transactions on VLSI Systems,* vol. 8, no. 2, Apr. `00, pp.129-137.

[14] T. M. Conte and S. W. Sathaye, "Properties of rescheduling size invariance for dynamic rescheduling-based VLIW cross-generation compatability", *IEEE Transactions on Computers*, vol. C-49, no. 8, Aug. `00, pp. 814-825.

[15] T. M. Conte, “Choosing the brain(s) of an embedded system,” *IEEE Computer*, vol. 35, no. 7., Jul. ’02, pp. 106-107.

[16] C. Fu, J. T. Bodine, T. M. Conte, “Modeling value speculation: An optimal edge selection problem,” *IEEE Transactions on Computers,* vol. C-52, no. 3, Mar. ’03, pp. 277-292.

[17] H. Zhou, M. C. Toburen, E. Rotenberg, and T. M. Conte. "Adaptive Mode Control: A Static-Power-Efficient Cache Design". *ACM Transactions in Embedded Computing Systems (TECS)*, vol. 2, no. 3, Aug. ’03, pp. 347-372.

[18] P. Mehrotra, V. Rao, T. M. Conte and P. D. Franzon, “Optimal Chip Package Co-design for High Performance DSP,” *IEEE Transactions on Advanced Packaging,* vol. 28, no. 2, May ‘05, pp. 288 – 297.

[19] A. Bechini, T. M. Conte, C. A. Prete, “Opportunities and challenges in embedded systems,” *IEEE Micro,* July-August, ‘04, pp. 2-3.

[20] H. Zhou and T. M. Conte, “Enhancing memory-level parallelism via recovery-free value prediction,” *IEEE Transactions on Computers,* vol. C-54, no. 7, Jul. ’05, pp. 897-912.

[21] E. Ozer and T. M. Conte, “High-performance and low-cost dual-thread VLIW processor using WELD architecture paradigm,” *IEEE Transactions on Parallel and Distributed Systems*, vol. 16, no. 12, Dec. ’05.

[22] S. Sharma, J. G. Beu and T. M. Conte, “Spectral prefetcher: An effective mechanism for L2 cache prefetching,” *ACM Transactions on Architecture and Code Optimization*, vol. 2 , no. 4, Dec. '05, pp. 423-450.

[23] J. A. Poovey, M. Levy, S. Gal-On, T. M. Conte, “A benchmark characterization of the EEMBC benchmark suite” *IEEE Micro,* Sep.-Oct. ’09.

PEER-REVIEWED CONFERENCE PUBLICATIONS

[1] W. W. Hwu and T. M. Conte, “A simulation study of simultaneous vector prefetch performance in multiprocessor memory subsystems (extended abstract),” in *Proceedings of the ACM Conference on Measurement and Modeling of Computer Systems (SIGMETRICS’89)*, (Berkeley, CA), p. 227, May 1989.

[2] W. W. Hwu, T. M. Conte, and P. P. Chang, “Comparing software and hardware schemes for reducing the cost of branches,” in *Proceedings of the 16th Annual International Symposium Computer Architecture (ISCA-16)*, (Jerusalem, Israel), pp. 224-233, June 1989.

[3] T. M. Conte and W. W. Hwu, “Benchmark characterization for experimental system evaluation,” in *Proceedings of the 23rd Hawaii International Conference on System Sciences,* Vol. 1, (Kona, HI), pp. 6-18, Jan. 1990.

[4] T. M. Conte and W. W. Hwu, “Benchmark characterization,” in *Proceedings of the 24th Hawaii International Conference on System Sciences,* vol. 1, (Kauai, HI), pp. 364-372, Jan. 1991.

[5] T. M. Conte and W. W. Hwu, “Systematic prototyping of superscalar computer architectures,” in *Proceedings of the 3rd IEEE International Workshop on Rapid System Prototyping*, (Research Triangle Park, NC), June 1992.

[6] T. M. Conte, “Tradeoffs in processor/memory interfaces for superscalar processors,” in *Proceedings of the 25th Annual International Symposium on Microarchitecture (MICRO-25),* (Portland, OR), pp. 202-205, Dec. 1992.

[7] T. M. Conte, “Architectural resource requirements of contemporary benchmarks: A wish list,” in *Proceedings of the 26th Hawaii International Conference on System Sciences,* vol. 1, (Maui, HI), pp. 517-529, Jan. 1993. (winner: *best paper)*

[8] T. M. Conte and W. Mangione-Smith, “Determining cost-effective multiple issue processor designs,” in *Proceedings of the 1993 International Conference on Computer Design (ICCD’93),* (Cambridge, MA), Oct. 1993.

[9] T. M. Conte, B. A. Patel, and J. S. Cox, "Using branch handling hardware to support profile-driven optimization," in *Proceedings of the 27th Annual International Symposium on Microarchitecture (MICRO-27),* (San Jose, CA), pp. 12-21, Dec. 1994.

[10] T. M. Conte, K. N. P. Menezes and S. A. Sathaye, "A technique to determine power efficient, high-performance superscalar processors," in *Proceedings of the 28th Hawaii International Conference on System Sciences,* vol. 1, (Maui, HI), pp. 324-333, Jan. 1995. (winner: *best paper*)

[11] J. S. Cox, D. P. Howell, and T. M. Conte, "Commercializing profile-driven optimization," in *Proceedings of the 28th Hawaii International Conference on System Sciences,* vol. 1, (Maui, HI), pp. 221-228, Jan. 1995.

[12] T. M. Conte, K. N. Menezes, P. M. Mills and B. A. Patel, "Optimization of instruction fetch mechanisms for high issue rates," in *Proceedings of the 22nd Annual International Symposium on Computer Architecture (ISCA-22)*, (Santa Margherita, Italy), Jun. 1995.

[13] A. Singla and T. M. Conte, "Bipartitioning for hybrid FPGA-software simulation," in *Proceedings of the 1996 IEEE International Conference on VLSI Design,* (Banglore, India), Jan. 1996.

[14] T. M. Conte and S. W. Sathaye, "Dynamic rescheduling: A technique for object code compatibility in VLIW architectures," in *Proceedings of the 28th Annual International Symposium on Microarchitecture (MICRO-28),* (Ann Arbor, MI), Nov. 1995. (winner: *best paper*)

[15] T. M. Conte, M. A. Hirsch, and K. N. Menezes, "Reducing state loss for effective trace sampling of superscalar processors," *in Proceedings of the 1996 International Conference, on Computer Design (ICCD'96),* (Austin, TX), Oct. 1996.

[16] T. M. Conte, S. Banerjia, S. Y. Larin, K. N. Menezes and S. W. Sathaye, "Instruction fetch mechanisms for VLIW architectures with compressed encodings," in *Proceedings of the 29th Annual International Symposium on Microarchitecture (MICRO-29),* (Paris, France), Nov. 1996.

[17] T. M. Conte, K. N. Menezes and M. A. Hirsch, "Accurate and practical profile-driven compilation using the profile buffer," *in Proceedings of the 29th Annual International Symposium on Microarchitecture (MICRO-29)*, (Paris, France), Nov. 1996.

[18] T. M. Conte, S. Banerjia and S. W. Sathaye, "A persistent rescheduled-page cache for low overhead object code compatibility in VLIW architectures," *in Proceedings of the 29th Annual International Symposium on Microarchitecture (MICRO-29),* (Paris, France), Nov. 1996.

[19] S. Banerjia, W. A. Havanki, T. M. Conte, "Treegion scheduling: A technique for extracting instruction level parallelism", *in Proceedings of the 1997 European conference in Parallel Processing,* (Passau, Germany), Aug., 1997.

[20] K. N. Menezes, S. W. Sathaye and T. M. Conte, "Path prediction for high issue-rate processors," in *Proceedings of the 1997 International Conference on Parallel Architectures and Compilation Techniques (PACT'97)*, (San Francisco, CA), Nov. 1997.

[21] W. A. Havanki, S. Banerjia and T. M. Conte, "Treegion scheduling for wide-issue processors," in *Proceedings of the 1997 4th International Symposium on High-Performance Computer Architecture (HPCA-4)*, (Las Vegas), Feb. 1998.

[22] C. Fu, M. D. Jennings, and T. M. Conte, "Value speculation scheduling for high performance processors," in *Proceedings of the 8th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VIII)*, (San Jose, CA), Oct., 1998.

[23] E. Ozer, S. W. Sathaye, K. N. Menezes, S. Banerjia, M. D. Jennings and T. M. Conte, "A fast interrupt handling scheme for VLIW processors," in *Proceedings of the 1998 International Conference on Parallel Architectures and Compilation Techniques (PACT'98)*, (Paris, France), Oct. 1998.

[24] E. Ozer, S. Banerjia, T. M. Conte, "Unified assign and schedule: A new approach to scheduling for clustered register file microarchitectures," in *Proceedings of the 31st Annual International Symposium on Microarchitecture*, (Dallas, TX), Nov. 1998.

[25] S. Y. Larin and T. M. Conte, "Compiler-driven cached code compression schemes for embedded ILP processors," in *Proceedings of the 32nd Annual International Symposium on Microarchitecture (MICRO-32)*, (Haifa, Isreal), Nov. 1999.

[26] K. M. Hazelwood and T. M. Conte, "A lightweight algorithm for dynamic if-conversion during dynamic optimization," in *Proceedings of the 2000 International Conference on Parallel Architectures and Compilation Techniques (PACT'00),* (Philadelphia, PA), Oct. 2000.

[27] H. Zhou, M. C. Toburen, E. Rotenberg and T. M. Conte, "Adaptive mode control: A static-power-efficient cache," in *Proceedings of the 2001 International Conference on Parallel Architectures and Compilation Techniques (PACT'01),* (Barcelona, Spain), Sep. 2001.

[28] E. Ozer and T. M. Conte, "Weld: A multithreading technique towards latency-tolerant VLIW processors," in *Proceedings of the 8th International Conference on High Performance Computing (HiPC-8),* (Hyderabad, India), Dec. 2001.

[29] H. Zhou, M. D. Jennings, and T. M. Conte, "Tree traversal scheduling: A global scheduling technique for VLIW/EPIC processors," in *Proceedings of the 14th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC'01)*, (Cumberland Falls, KY), August 2001.

[30] H. Zhou and T.M. Conte, "Code size efficiency in global scheduling for ILP processors," in *Proceedings of the 6th Annual Workshop on the Interaction between Compilers and Computer Architectures (INTERACT-6)* held in conjunction with the *8th International Symposium on High Performance Computer Architecture (HPCA-8)*, (Cambridge, MA), February 2002.

[31] G. G. Pechanek, S. Larin and T. Conte, "Any-size instruction abbreviation technique for embedded DSPs," in *Proceedings of the 15th Annual IEEE ASIC/SOC Conference*, (Rochester, NY), September 2002.

[32] H. Zhou, J. Flanagan, T. M. Conte, "Detecting global stride locality in value streams," *Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA-30),* (San Diego, CA), June 2003, pp. 324–335.

[33] H. Zhou and T. M. Conte, "Enhancing memory level parallelism via recovery-free value prediction," in *Proceedings of the 2003 International Conference on Supercomputing (ICS'03)* (San Francisco, CA), June 2003.

[34] M. C. Rosier and T. M. Conte, "Treegion Instruction Scheduling in GCC," in *Proceedings of the 2006 GCC Developers' Summit,* (Ottowa, Canada), June 2006.

[35] P. D. Bryan, M. C. Rosier and T. M Conte, "Reverse State Reconstruction for Sampled Microarchitectural Simulation," in *Proceedings of the 2007 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASSS'07), (San Jose, CA)*, April 2007.

[36] P. D. Bryan and T. M Conte, "Combining Cluster Sampling with Single Pass Methods for Efficient Sampling Regimen Design," in *Proceedings of the 2007 International Conference, on Computer Design (ICCD'07),* (Lake Tahoe, CA), Oct. 2007.

[37] B. V. Iyer and T. M. Conte, "A Power Model for Register-Sharing Structures," in *Proceedings of the 2008 IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES'08),* (Milano, Italy), Sep. 2008.

[38] B. V. Iyer, J. A. Poovey and T. M. Conte, "Energy-Aware Opcode Design," in *Proceedings of the 26th International Conference on Computer Design (ICCD'08)*, (Lake Tahoe, California), Oct. 12-15, 2008.

[39] B. V. Iyer, J. G. Beu, and T. M. Conte, "'Length Adaptive Processors: The solution for Energy/Performance Dilemma in Embedded Systems," *Workshop on Interaction Between Compilers and Computer Architecture (INTERACT-13), held in conjunction with HPCA-15*, (Raleigh, NC), Feb 16th, 2009.

[40] B. V. Iyer and T. M. Conte, "On power and energy trends of IEEE 802.11n PHY," *Proceedings of the 12th International ACM Symposium on Modeling Analysis and Simulation of Wireless and Mobile Systems (MSWiM 2009)*, (Tenerife, Canary Islands, Spain), Oct. 26-19, 2009.

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