(12) **United States Patent**
Hui et al.

(10) **Patent No.: US 7,265,014 B1**
(45) **Date of Patent: Sep. 4, 2007**

(54) **AVOIDING FIELD OXIDE GOUGING IN SHALLOW TRENCH ISOLATION (STI) REGIONS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 279 days.

(21) Appl. No.: **10/799,413**

(22) Filed: **Mar. 12, 2004**

(51) **Int. Cl.**
H01L 21/764 (2006.01)
H01L 29/00 (2006.01)

(52) **U.S. Cl.** **438/257**; 438/296; 257/E21.546

(58) **Field of Classification Search** 438/257, 438/266, 424, 296; 257/E21.546
See application file for complete search history.

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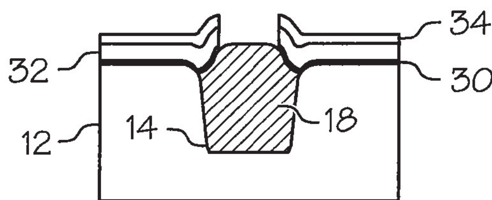
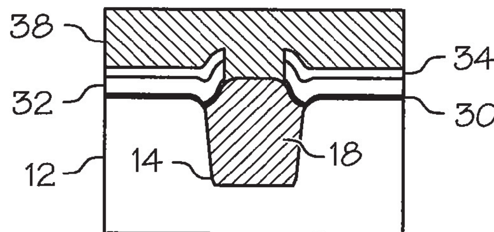
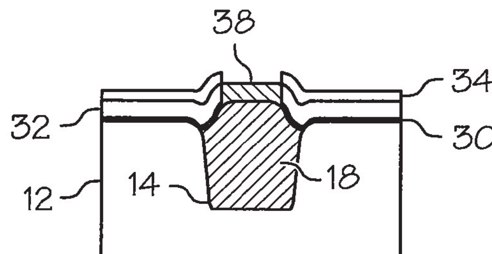
(57) **ABSTRACT**

A method and device for avoiding oxide gouging in shallow trench isolation (STI) regions of a semiconductor device. A trench may be etched in an STI region and filled with insulating material. An anti-reflective coating (ARC) layer may be deposited over the STI region and extend beyond the boundaries of the STI region. A portion of the ARC layer may be etched leaving a remaining portion of the ARC layer over the STI region and extending beyond the boundaries of the STI region. A protective cap may be deposited to cover the remaining portion of the ARC layer as well as the insulating material. The protective cap may be etched back to expose the ARC layer. However, the protective cap still covers and protects the insulating material. By providing a protective cap that covers the insulating material, gouging of the insulating material in STI regions may be avoided.

9 Claims, 3 Drawing Sheets







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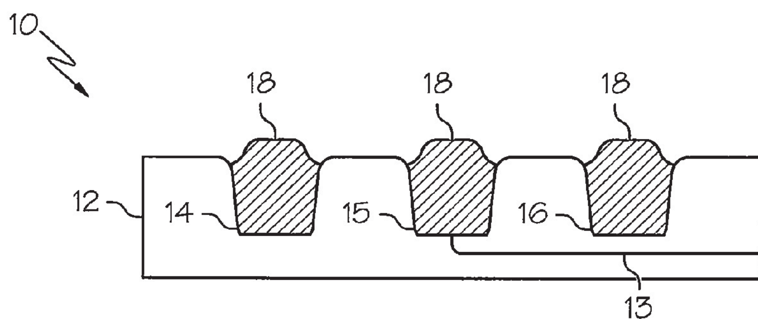

FIG. 1

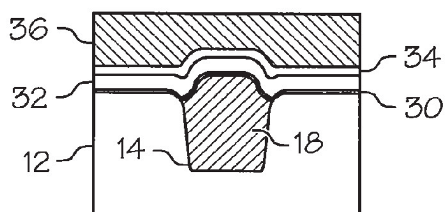

FIG. 3A

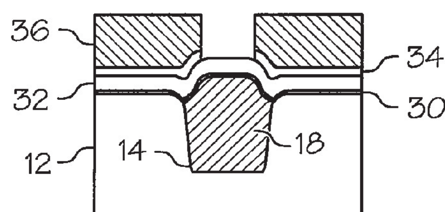

FIG. 3B

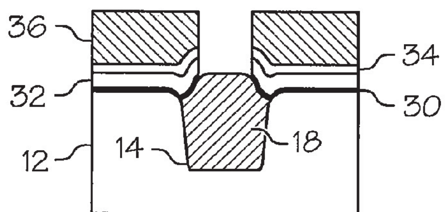

FIG. 3C

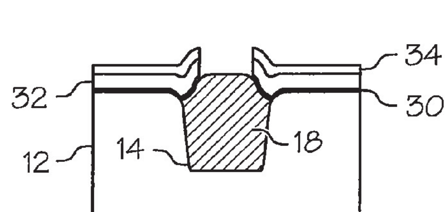

FIG. 3D

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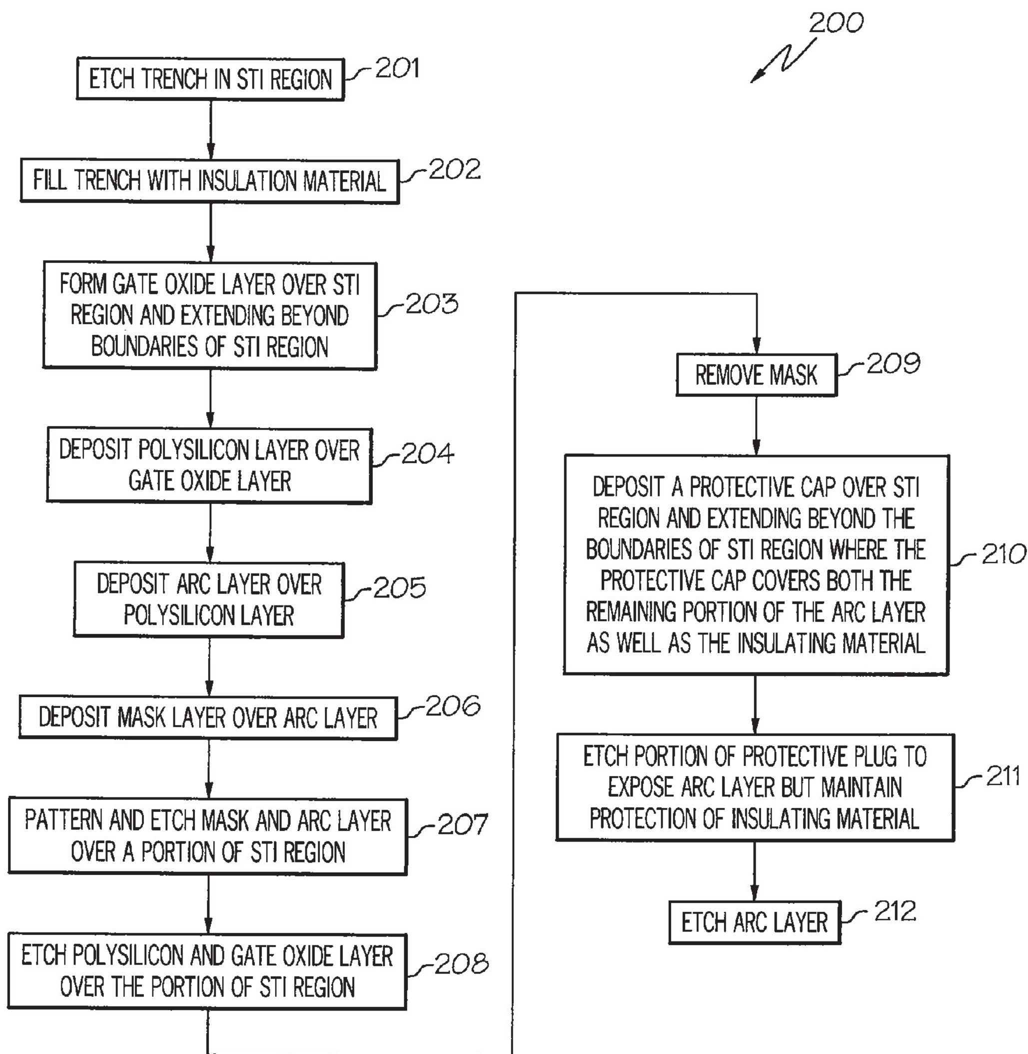

FIG. 2

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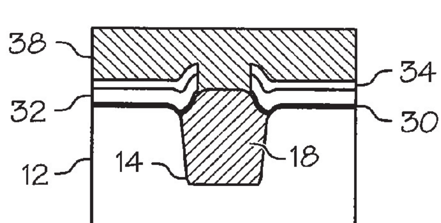

FIG. 3E

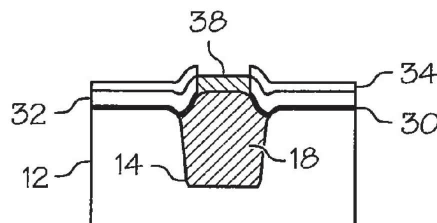

FIG. 3F

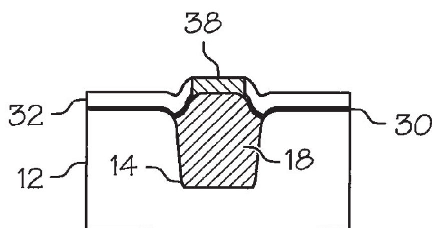

FIG. 3G

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AVOIDING FIELD OXIDE GOUGING IN SHALLOW TRENCH ISOLATION (STI) REGIONS

TECHNICAL FIELD

The present invention is related to the use of shallow trench isolation (STI) in the design and fabrication of integrated circuits, and, more specifically, avoiding damage to the field oxide in STI regions during subsequent processing steps in the fabrication of an integrated circuit device.

BACKGROUND INFORMATION

In the design and fabrication of integrated circuits, it is necessary to isolate adjacent active devices from one another so that leakage currents between devices do not cause the integrated circuits to fail or malfunction. As dimensions of semiconductor devices have shrunk, shallow trench isolation (STI) techniques have largely replaced other isolation techniques such as LOCOS. In fabricating an STI region, conventional photolithography and etching techniques may be used to create trenches in the integrated circuit substrate. The trenches may then be filled with one or more insulating materials, such as thermal silicon oxide. The wafer may then be planarized using chemical-mechanical polishing (CMP). Additional processing steps form the active devices on the substrate which are interconnected to create the circuitry in the integrated circuit.

As stated above, conventional photolithography techniques may be used to create trenches in the integrated circuit substrate. In photolithography, light may be used to expose a photolithography mask overlying the trench where the light may be reflected off of the integrated circuit layers underneath the mask. The reflections may have detrimental effects on the quality and accuracy of the resulting mask. To improve the results of photolithography at these small scales, SiN (SiON, SiRN) may be used as an anti-reflective coating or hard mask layer. The anti-reflective coating layer may reduce or substantially eliminate these reflections thereby resulting in improved masks for creating small features and structures in an integrated device.

After the formation of the gate, the hard mask/anti-reflective coating layer may need to be removed prior to subsequent device processing. The hard mask/anti-reflective coating layer may be removed using either a conventional wet strip process or a conventional plasma etching process. A conventional wet strip process may use hot phosphoric acid which may damage the polysilicon layer underlying the anti-reflective coating layer; whereas, a conventional plasma etching process may cause extensive gouging in any exposed field oxide, including in the thermal oxide in an STI region. Gouges in STI regions may alter the isolation properties of the STI region. Further, gouges in STI regions may create an uneven surface causing gap-fill problems for subsequent processing of the device wafer.

Therefore, there is a need in the art to strip a hard mask/anti-reflective coating layer that avoids damage to exposed polysilicon surfaces as well as avoids gouging exposed field oxide such as in STI regions.

SUMMARY OF INVENTION

The problems outlined above may at least in part be solved by depositing a protective cap or plug over the hard mask/anti-reflective coating layer. The protective cap may [...]

coating layer. However, the protective cap still covers and protects the thermal oxide in the trench. By providing a protective cap that covers the thermal oxide in the trench, gouging of the exposed field oxide in STI regions may be avoided.

In one embodiment of the present invention, a method for avoiding oxide gouging in shallow trench isolation (STI) regions of a semiconductor device may comprise the step of etching a trench in an STI region. The method may further comprise depositing insulating material in the formed trench. The method may further comprise depositing an anti-reflective coating layer overlying the STI region and extending beyond the boundaries of the STI region. The method may further comprise etching a portion of the anti-reflective coating layer over the STI region leaving a remaining portion of the anti-reflective coating layer over the STI region and extending beyond the boundaries of the STI region. The method may further comprise depositing a protective cap covering the STI region and extending beyond the boundaries of the STI region. The deposited protective cap covers the remaining portion of the anti-reflective coating layer as well as the insulating material in the trench.

In another embodiment of the present invention, a device may comprise a trench in a shallow trench isolation (STI) region. The device may further comprise insulating material filled in the trench. The device may further comprise a gate oxide layer covering a portion of the STI region and extending beyond the boundaries of the STI region. The device may further comprise a polysilicon layer overlying the gate oxide layer where the polysilicon layer covers the portion of the STI region and extends beyond the boundaries of the STI region. The device may further comprise an anti-reflective coating layer overlying the polysilicon layer where the anti-reflective coating layer covers the portion of the STI region and extends beyond the boundaries of the STI region. The device may further comprise a protective cap overlying the anti-reflective coating layer where the protective cap covers the entire STI region and extends beyond the boundaries of the STI region. Specifically, the protective cap covers the anti-reflective coating layer covering the portion of the STI region and covers the insulating material filled in the trench over the STI region.

The foregoing has outlined rather broadly the features and technical advantages of one or more embodiments of the present invention in order that the detailed description of the present invention that follows may be better understood. Additional features and advantages of the present invention will be described hereinafter which form the subject of the claims of the invention.

BRIEF DESCRIPTION OF DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description is considered in conjunction with the following drawings, in which:

FIG. **1** illustrates an embodiment of the present invention of a partial cross-section of a semiconductor wafer including a number of shallow trench isolation structures;

FIG. **2** illustrates a flowchart of a method for avoiding field oxide gouging in shallow trench isolation (STI) regions of a semiconductor device in accordance with the present invention; and

FIGS. **3**A through **3**G illustrate various stages in the fabrication of an integrated circuit in an STI region of a wafer in accordance with an embodiment of the present [...]

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