Trials@uspto.gov
571-272-7822

Paper 13
Entered: August 13, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MACRONIX INTERNATIONAL CO., LTD.,
MACRONIX ASIA LIMITED, MACRONIX (HONG KONG) CO., LTD.,
and MACRONIX AMERICA, INC.,
Petitioner,

v.

SPANSION LLC,
Patent Owner.

Case IPR2014-00898
Patent 7,151,027 B1

Before DEBRA K. STEPHENS, JUSTIN T. ARBES, and
RICHARD E. RICE, *Administrative Patent Judges.*

RICE, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

EXHIBIT 2000
SPANSION
9/23/14
IPR2014-00898

Macronix International Co., Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. (collectively "Petitioner") filed a Corrected Petition (Paper 6, "Pet.") to institute an *inter partes* review of claims 7 and 14 of U.S. Patent No. 7,151,027 B1 (Ex. 1001, "the '027 patent") pursuant to 35 U.S.C. §§ 311-319. Pet. 1. Patent Owner Spansion LLC ("Patent Owner") filed a Preliminary Response (Paper 12, "Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314. For the reasons that follow, the Board has determined to institute an *inter partes* review.

I. BACKGROUND

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a):

> THRESHOLD—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Petitioner challenges claims 7 and 14 as unpatentable under 35 U.S.C. § 103(a). Pet. 4. We grant the Petition, as discussed below.

A. Related Proceedings

Petitioner discloses that the '027 patent is asserted in: (1) *Spansion LLC v. Macronix International Co., Ltd.*, Civ. No. 3:13-cv-03566 (N.D. Cal.); and (2) *In re Flash Memory Chips and Products Containing Same*, Inv. No. 337-TA-893 (U.S. Int'l Trade Comm'n). *Id.* at 2.

Petitioner also discloses that the '027 patent is involved in IPR2014-00108, captioned *Macronix International Co., Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. v. Spansion LLC*, in which we instituted an *inter partes* review of claims 1-6 and 8-13, but not claims 7 and 14. *Id.*

B. The '027 Patent (Ex. 1001)

Figures 3A-3G of the '027 patent illustrate steps in a process for forming an interface structure between a memory array and a periphery of a memory device. *See* Ex. 1001, 3:18-22, 54-57. At the step illustrated in Figure 3D of the '027 patent, which is reproduced below, "second polysilicon layer (poly-2) 320" is deposited above dialectric material 315 and substrate 300. *Id.* at 4:22-24.

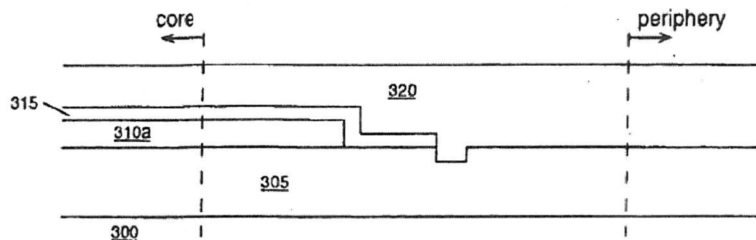

Figure 3D

A vertical dashed line on the left of Figure 3D denotes the approximate border between a memory array ("core") and an interface area, and a vertical dashed line on the right of the figure denotes the approximate border between the interface area and a periphery. *See id.* at 3:54-57 (referring to Figure 3A). As depicted in Figure 3D, first polysilicon layer 310a, referred to as "gate polysilicon ('poly-1') 310a" in the '027 patent, is disposed beneath dielectric material 315. *Id.* at 3:50-53. Figure 3D also

depicts substrate 300, isolation area 305, and second polysilicon layer 320 ("poly-2"). *See id.* at 3:51-52 (referring to Figure 3A); 4:22-25.

Figure 3E of the '027 patent, which is reproduced below, depicts the step of etching a portion of poly-1 layer 310a, dielectric material layer 315, and poly-2 layer 320, proximate to the memory array. *Id.* at 4:27-30.

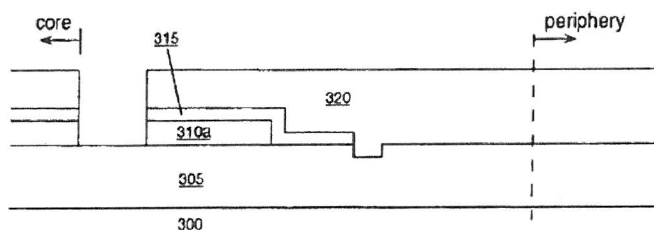

Figure 3E

The '027 patent discloses that "a known process (such as a stacked gate etch)" is used for the etching step in Figure 3E. *Id.*

Figure 3F of the '027 patent, which is reproduced below, depicts the step of etching a portion of poly-2 layer 320 proximate to the periphery. *Id.* at 4:38-40. As described in the '027 patent, "a known process (such as a second gate etch)" is used for the etching step depicted in Figure 3F. *Id.* The etching step is used to form interface structure 360, which is illustrated in Figure 3F. *Id.* at 4:41.

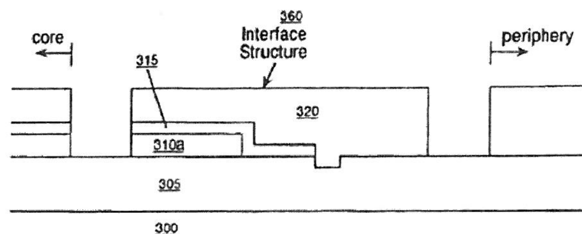

Figure 3F

As depicted in Figure 3F and described in the '027 patent, "interface structure 360 is the same height as the memory array proximate to the memory array and the same height as the periphery proximate to the periphery, such that step size is smoothed out reducing the occurrence of stringers from spacer etching." *Id.* at 4:49-54.

C. Illustrative Claim

Claims 1 and 8 are independent. Claim 7 depends directly from claim 1, and claim 14 depends directly from claim 8. Challenged claims 7 and 14 recite similar limitations. Claims 8 and 14, which are reproduced below, are illustrative:

> 8. A method for fabricating a memory device, said method comprising:
>
> forming a poly-1 layer above a substrate at an interface between a memory array and a periphery of said memory device;
>
> forming a poly-2 layer above said poly-1 layer at said interface;
>
> etching said poly-1 layer and said poly-2 layer proximate to said memory array; and
>
> etching said poly-2 layer proximate to said periphery, such that an interface structure including a portion of said poly-1 layer and a portion of said poly-2 layer remains at said interface.
>
> 14. The method as recited in claim 8 wherein said interface structure is a same height as said memory array proximate to said memory array and a same height as said periphery

> proximate to said periphery, such that step size is smoothed out reducing an occurrence of stringers from spacer etching.

Id. at 6:2-11, 7:5-8:4.

D. The Prior Art

Petitioner relies upon the following prior art references (Pet. 4):

Yuzuriha	US 6,458,655 B1	Oct. 1, 2002	Ex. 1003
Tsukamoto	US 2003/0042520 A1	Mar. 6, 2003	Ex. 1004
Lin	C.-F. Lin et al., *A ULSI shallow trench isolation process through the integration of multilayered dielectric process and chemical-mechanical planarization*, THIN SOLID FILMS 248-52 (1999)	1999	Ex. 1007

Petitioner contends that each of Yuzuriha, Tsukamoto, and Lin is prior art to the claims of the '027 patent under 35 U.S.C. § 102(b). *Id.* at 9, 18-19.

E. The Asserted Ground

Petitioner challenges claims 7 and 14 of the '027 patent on the following ground (*id.* at 9):

References	Basis	Claims Challenged
Yuzuriha, Tsukamoto, and Lin	§ 103(a)	7 and 14

F. Claim Interpretation

Consistent with the statute and legislative history of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), the Board interprets claims using the "broadest reasonable construction in light of the specification of the patent in which [they] appear[]." 37 C.F.R. § 42.100(b); *see* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). For purposes of this decision, we interpret certain claim limitations as follows:

1. "poly-2 layer" (claims 1, 7, and 8); and "poly-1 layer" (claim 8)

We interpret "poly-2 layer" and "poly-1 layer" as we did in IPR2014-00108, and incorporate our previous analysis herein. *See Macronix International Co., Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. v. Spansion LLC*, IPR2014-00108, Paper 16 (PTAB May 8, 2014) ("IPR2014-00108 Dec."), 8-9. That is, applying the broadest reasonable interpretation of the claims in light of the specification, we interpret "poly-2 layer" to mean "a polysilicon layer deposited later in time than a first polysilicon layer." Similar to "poly-2 layer," we interpret "poly-1 layer" to mean "a first polysilicon layer."

2. "etching said poly-1 layer and said poly-2 layer proximate to said memory array" (claim 8)

Patent Owner argues, as it did in IPR2014-00108, that the plain language of the claims requires that both the poly-1 layer and the poly-2 layer are etched in a single "etching" step. Prelim. Resp. 11; *see* IPR2014-00108, Paper 14, 15. In IPR2014-00108, we decided:

> The specification pertinently states "a *known process* (such as a stacked gate etch) is used to etch a portion of poly-1 310a, dialectric material 315 and poly-2 320 proximate to the memory array." Ex. 1001, 4:28-30 (emphasis added). As such, the specification describes using a "process" to etch the two recited structures. Patent Owner does not explain sufficiently why "etching" in claim 8 requires the recited structures to be etched in "one step" rather than by a process that involves multiple steps, for example, sequentially etching one structure and then the other, in separate steps.

IPR2014-00108 Dec., 9.

In this proceeding, Patent Owner compares the disputed "etching" language of claim 8 with the "etching" language of claims 1 and 2.[1] Prelim. Resp. 11. Patent Owner argues that claim 1 recites etching the poly-2 layer proximate the memory array and etching the poly-2 layer proximate the periphery as two distinct "etching" steps. *Id.* On the current record, we are not persuaded that, merely because "etching said poly-1 layer and said poly-2 layer proximate to said memory array," in claim 8, is recited differently from the etching steps in claim 1, it must require etching the poly-1 and poly-2 layers in a single step. *See id.* We also are not persuaded by Patent Owner's similar argument with respect to claim 2. *Id.*

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[1] Claim 1 recites "etching said poly-2 layer proximate to said memory array" and "etching said poly-2 layer proximate to said periphery such that a portion of said poly-2 layer remains at said interface." Claim 2, which depends from claim 1, recites "etching said poly-1 layer proximate to said memory array" and "etching said poly-1 layer proximate to said periphery such that a portion of said poly-1 layer remains at said interface." Claim 8 recites "etching said poly-1 layer and said poly-2 layer proximate to said memory array" and "etching said poly-2 layer proximate to said periphery, such that an interface structure including a portion of said poly-1 layer and a portion of said poly-2 layer remains at said interface."

Patent Owner also relies on the '027 patent specification and drawings. *Id.* at 11-13. Patent Owner argues that the words "[e]tch the poly-1 layer and poly-2 layer proximate to the memory array," in Figure 4 (flowchart), "explicitly describes the etching of the poly-1 layer and poly-2 layer proximate to the memory array as a single etching 'step' ('step 440') in its process." *Id.* at 12 (italics omitted); *see also id.* at 13 (citing Ex. 1001, 4:27-30, 5:21-24, Figs. 3D, 3E, 4).

Based on the current record, we are not persuaded by Patent Owner's arguments based on the specification and drawings. Although the specification states that "the poly-1 layer and the poly-2 layer are etched proximate to the memory array" at "step 440" (Ex. 1001, 5:21-24; *see id.*, Fig. 4), the specification also states:

> "[a]lthough specific steps are disclosed in process 400, such steps are exemplary." That is, the present invention is well suited to performing various other steps or variations of the steps recited in process 400.

Id. at 5:7-10. At this stage of the proceeding, we are not persuaded that any disclosure in the specification or drawings requires etching the poly-1 and poly-2 layers proximate to the memory array in a single etching step.

Accordingly, applying the broadest reasonable interpretation of claim 8 consistent with the specification, we determine, as we did in IPR2014-00108, that "etching said poly-1 layer and said poly-2 layer proximate to said memory array" does not require a single etching step.

3. *"such that step size is smoothed out reducing an occurrence of stringers from spacer etching" (claims 7 and 14)*

Petitioner contends that the phrase "such that step size is smoothed out reducing an occurrence of stringers from spacer etching," recited in

claims 7 and 14, is not a limitation. Pet. 6. We did not interpret expressly that phrase in IPR2014-00108. Petitioner argues that the phrase merely states an intended result of the limitation "said interface structure is a same height as said memory array proximate to said memory array and a same height as said periphery proximate to said periphery." *Id.* According to Petitioner, the specification "states that making the heights of the structures the same reduces step size, which in turn, reduces stringers from spacer etching." *Id.* (citing Ex. 1001, 2:62-66). Petitioner represents that in the co-pending ITC proceeding involving the same patent and parties, both parties have agreed that the phrase is not a limitation. *Id.* (citing Ex. 1006, 13). Patent Owner does not dispute Petitioner's proposed claim construction.

Applying the broadest reasonable interpretation of the claims in light of the specification, and for purposes of this decision, we agree that the phrase "such that step size is smoothed out reducing an occurrence of stringers from spacer etching" is an intended result and not a claim limitation.

4. Other Terms

No other terms need be construed expressly for purposes of this decision.

II. DISCUSSION

We turn now to Petitioner's asserted ground of unpatentability and Patent Owner's arguments in its Preliminary Response to determine whether Petitioner has met the threshold standard of 35 U.S.C. § 314(a). Petitioner contends that claims 7 and 14 would have been obvious over Yuzuriha, Tsukamoto, and Lin under 35 U.S.C. § 103(a). Pet. 9-24. For the reasons

explained below, we are persuaded on this record that Petitioner has established a reasonable likelihood of prevailing on that ground.

With respect to the limitations of independent method claims 1 and 8, Petitioner relies on the teachings of Yuzuriha. *Id.* at 9-16. Petitioner's analysis for these claims is similar to its analysis in IPR2014-00108. We are persuaded that Yuzuriha discloses the limitations of claims 1 and 8, for the reasons discussed in our Decision on Institution in IPR2014-00108. *See* IPR2014-00108 Dec., 14-18.

Claim 7 recites the method of claim 1, "wherein said portion of said poly-2 layer remaining at said interface is a same height as said memory array proximate to said memory array [and][2] a same height as said periphery proximate to said periphery, such that step size is smoothed out reducing an occurrence of stringers from spacer etching." Claim 14 similarly recites the method of claim 8, "wherein said interface structure is a same height as said memory array proximate to said memory array and a same height as said periphery proximate to said periphery, such that step size is smoothed out reducing an occurrence of stringers from spacer etching."

Referring to Figure 5 of Yuzuriha, Petitioner argues that "it is difficult to tell whether the height of the interface structure [dummy gate 14] taught by Yuzuriha is the same as the memory array proximate to the memory array and the periphery proximate to the periphery." Pet. 17 (citing Ex. 1003, 12:37-55, Fig. 5; Ex. 1002 (Declaration of Dhaval J. Brahmbhatt) ¶ 56). In that regard, Petitioner's Declarant, Mr. Brahmbhatt, testifies that "[a]ny differences in height in the dummy gate of [Yuzuriha's] Figure 5 result from

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[2] At this stage of the proceeding, we consider the omission of "and" after "said memory array" in claim 7 to be an obvious drafting error.

the fact that the surrounding structures are on gate oxides 9 and 12, rather than 'isolating oxide film 8.'" Ex. 1002 ¶ 57.

Figure 5 of Yuzuriha, reproduced below, is a cross-section of a semiconductor device:

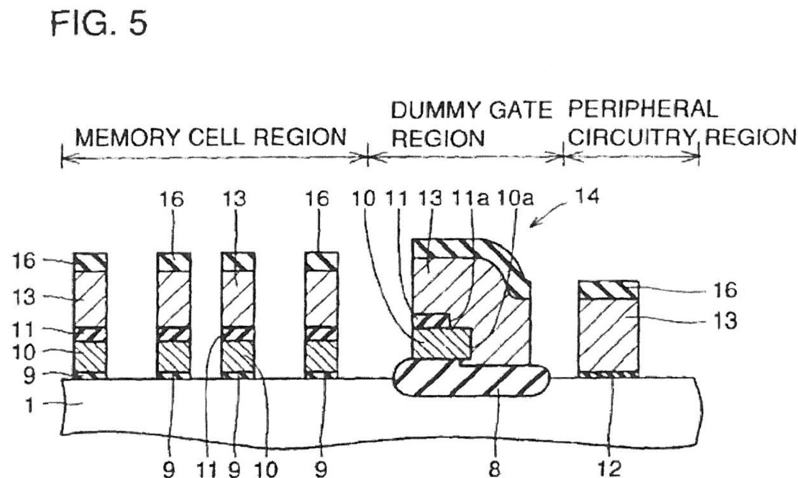


Figure 5 illustrates dummy gate 14 (on isolating oxide film 8), memory cells (on tunnel oxide film 9), and peripheral circuitry (on gate oxide film 12). *See* Ex. 1003, 11:52-54, 12:1-6, 27-28.

As depicted in Figure 5, the height of dummy gate 14 varies smoothly from one side to the other, such that the change in height is "gentle," i.e., not "abrupt." Ex. 1003, 12:37-52, Fig. 7. Yuzuriha teaches that such a "gentle step" facilitates "subsequent photolithography, processing, and the like." *Id.* at 12:52-55.

Petitioner argues that Lin teaches use of "shallow trench isolation" ("STI") to achieve improved planarization of isolation oxides, such as those formed by "local oxidation of silicon" ("LOCOS"), which "had been used '[f]or a long time,' and was 'the standard technology to provide electrical isolation between active devices for integrated circuits.'" Pet. 17–18 (quoting Ex. 1007, 248). As disclosed by Lin, STI involves etching a trench

pattern into the silicon substrate, filling the trench area, and polishing to "planarize the topography from previous deposition processes." Ex. 1007, 248. Figure 7(c) of Lin shows that the surface of the STI structure after completion of the STI process is co-planar with the surrounding substrate. *Id.* at 251; Fig. 7(c). Petitioner contends:

> Thus, a person having ordinary skill in the art would have understood that, to the extent that the Yuzuriha "oxide isolating film" was raised—and not planar, resulting in a height difference between the interface and periphery on one hand, and the interface and the memory array on the other, a person of ordinary skill in the art would have seen the obvious benefits of substituting STI in place of the oxide structure disclosed in Yuzuriha because (1) it was a known substitute for performing electrical isolation between active areas on integrated circuits . . . and (2) STI had advantages over local oxidization of silicon in that it could be planarized, thus reducing the "gentle step[.]"

Pet. 18-19 (citing Ex. 1007, 248 (left column)); Ex. 1002 ¶¶ 59–60 (supporting testimony of Dr. Brahmbhatt).

Petitioner further argues that Tsukamoto teaches using a dummy gate conductive film (DSG) structure formed on an STI area for "eliminating the difference in height between the memory cell forming region and the peripheral circuit forming region." *Id.* at 19 (quoting Ex. 1004 ¶ 58); *see* Ex. 1004 ¶¶ 2, 46. Figures 1 and 2 of Tsukamoto, as annotated in the Petition, are reproduced below:

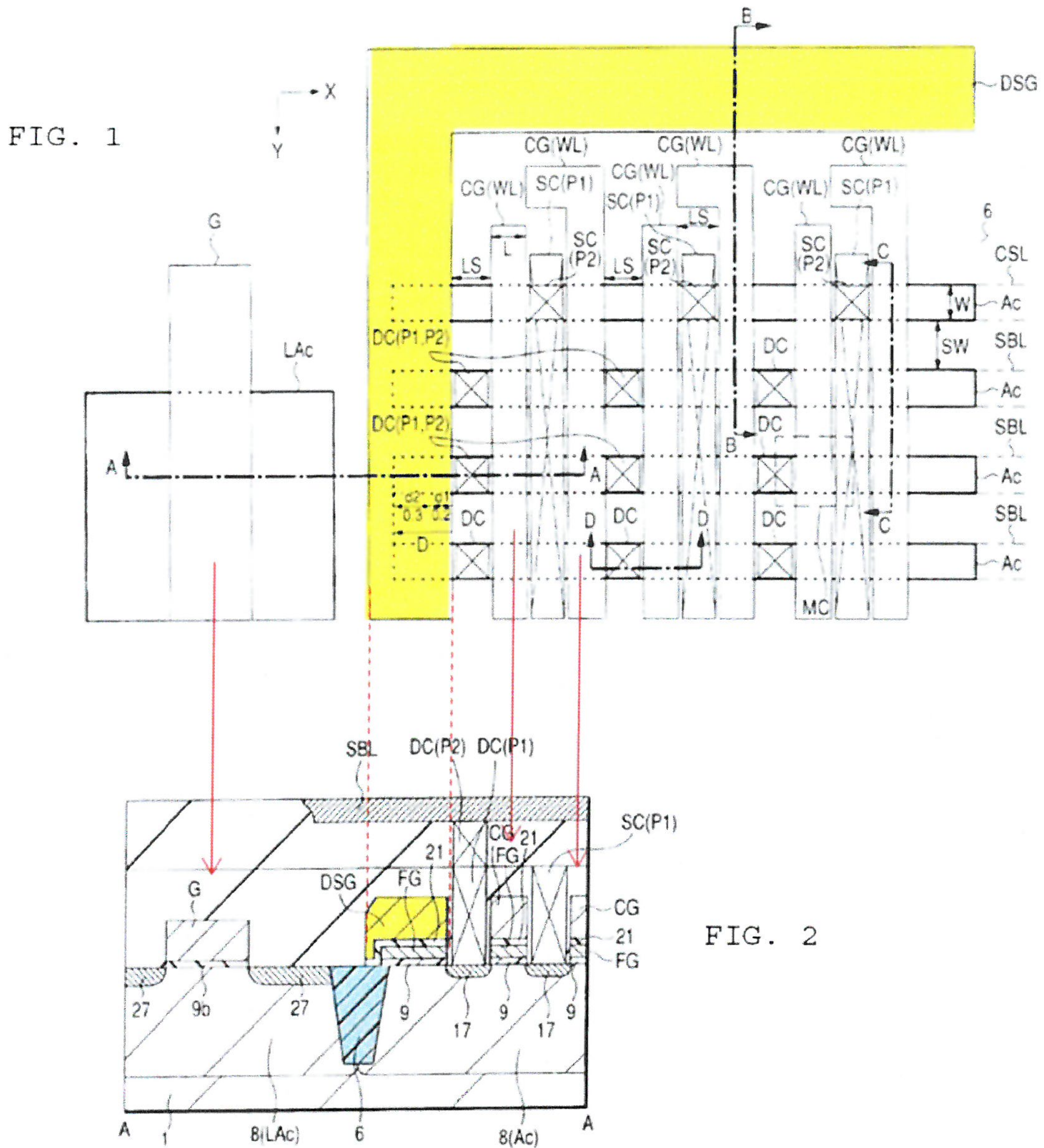


Figure 1 is a plan view of a portion of a semiconductor integrated circuit device. Figure 2 is a sectional view of the device that depicts dummy conductive film DSG, and STI insulating film 6, which is buried in a trench formed in substrate 1.

Pet. 20. Petitioner contends, based on the combination of Yuzuriha, Lin, and Tsukamoto, that:

> it would have been obvious to a person having ordinary skill in the art to modify Yuzuriha's structure to (1) use a planarized oxide isolation area such as a shallow trench isolation area to isolate the memory array and the periphery, and (2) to include a dummy gate structure that eliminates "the difference in height between the memory cell forming region and the peripheral circuit forming region," because such a configuration would have furthered Yuzuriha's goals of reducing—and in this case eliminating—a height differential between adjacent components and would have further improved "subsequent photolithography, processing and the like."

Pet. 21 (quoting Ex. 1003, 12:52-55; citing Ex. 1002 ¶¶ 56-57, 63-65). We are persuaded that Petitioner's analysis, supported by the testimony of Dr. Brahmbhatt, demonstrates a reasonable likelihood of prevailing as to claims 7 and 14.

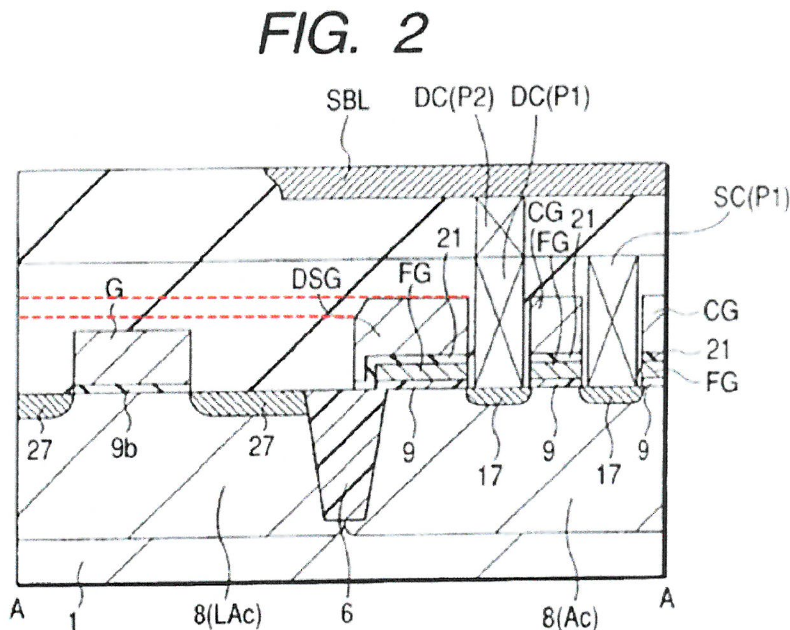
Patent Owner advances a number of arguments in opposition to the Petition. *See, e.g.,* Prelim. Resp. 3-4, 14-32. Patent Owner argues, for example, that Petitioner does not show sufficiently why a person of ordinary skill in the art would have combined Tsukamoto's teachings with those of Yuzuriha. *Id.* at 3. At this stage of the proceeding, however, we are persuaded that eliminating the difference in height between the memory cell region and the peripheral circuit region in an outer periphery portion of the memory cell array, as taught by Tsukamoto (*see* Ex. 1004 ¶ 58) according to Petitioner, would have advanced Yuzuriha's goal of eliminating abrupt height variations between a memory cell region and a peripheral circuitry region (*see* Ex. 1003, 12:37-52). *See* Pet. 19- 21; Ex. 1002 ¶¶ 62-63. We are persuaded on this record, therefore, that Petitioner has provided a sufficient reason with rational underpinning to combine the references. Patent Owner's argument that a person of ordinary skill would not have been

motivated to apply Yuzuriha to address the problems solved by the '027 Patent (*see* Prelim. Resp. 14-20) does not take into account the combined teachings of the references, and is, therefore, unpersuasive. Moreover, in an obviousness analysis, the reason to combine the prior art does not need to be the same as the reason contemplated by the inventor. *See In re Kahn*, 441 F.3d 977, 990 (Fed. Cir. 2006). Further, we note that the current record does not show that it would have been beyond the skill of a person of ordinary skill in the art to make Yuzuriha's dummy gate structure a same height as the memory cell region proximate the memory cell region and a same height as the peripheral circuit region proximate the peripheral circuit region.

Patent Owner also argues, unpersuasively, that Tsukamoto's teachings are directed to a structure (dummy conductive film DSG) that is located in the memory cell region, rather than in an interface between the memory cell region and the peripheral circuit region. Prelim. Resp. 21 & n. 5. This argument is directed to Tsukamoto's teachings in isolation, rather than the teachings of the combination of references as argued by Petitioner. *See* Pet. 10, 13-15.

Patent Owner further argues that the person of ordinary skill would not have modified the LOCOS isolation technology used in Yuzuriha with the teachings of Tsukamoto and Lin directed to STI technology, because of known problems associated with STI technology. Prelim. Resp. 30-31. Based on the current record, however, we are persuaded that the benefits of STI technology, as taught by Tsukamoto and Lin, are a sufficient reason why a person of ordinary skill would have substituted the STI technology for the LOCOS technology.

Finally, Patent Owner argues that Tsukamoto fails to disclose the required "same height" limitation of claims 7 and 14. *Id.* at 24-27. In particular, Patent Owner argues that, as depicted in Figure 2 of Tsukamoto, the DSG structure is not the same height as the periphery proximate to the periphery. Patent Owner provides an annotated version of Figure 2, which is reproduced below:



Patent Owner's annotated version of Figure 2 of Tsukamoto

Id. at 26. Patent Owner, however, does not attempt to reconcile its interpretation of Figure 2 with the express disclosure in Tsukamoto that the purpose of the DSG structure is to "eliminate[e] the difference in height between the memory cell forming region and the peripheral circuit forming region." *See* Ex. 1004 ¶ 58. Further, even if the specification were silent on the issue, Patent Owner has not shown that Figure 2 is to scale.

At this stage of the proceeding, we also are not persuaded by Patent Owner's assertion that the composite thickness of the layers comprising the

DSG structure is 336.5 nm, but the thickness of the layers comprising the structure of the peripheral circuit forming region is only 208 nm. Prelim. Resp. 26-27. Patent Owner computes the thickness of the DSG structure by adding the following individual layer thicknesses: gate insulating film 9 (10.5 nm), polycrystalline silicon film FG (100 nm), ONO film 21 (26 nm), and conductive film DSG (200 nm). *Id.* Patent Owner does not explain, however, why the computation includes the thicknesses of gate insulating film 9 and polycrystalline silicon film FG in view of Figure 2 of Tsukamoto, which shows that the portion of the DSG structure closest to the peripheral gate forming region does not include those layers. *See* Ex. 1004 ¶¶ 74-75, Fig. 2; Prelim. Resp. 26-27.[3] Further, Patent Owner does not proffer evidence in the record showing that totaling the disclosed thicknesses of the individual layers is an accurate method for ascertaining the height of the composite structure. *See, e.g.,* Ex. 1004 ¶¶ 74-78 (using the qualifier "about" when quantifying the thicknesses of the individual layers).[4]

In conclusion, based on the record before us, we are persuaded that Petitioner has established a reasonable likelihood of prevailing on its

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[3] Patent Owner also does not explain why it used 26 nm, instead of 16 nm, for the thickness of the ONO film. *See* Prelim. Resp. 26-27. Tsukamoto describes two exemplary ONO films, one that consists of three sub-layers of about 5 nm, about 7 nm, and about 4 nm, respectively, and another that consists of those three sub-layers and an additional sub-layer of about 10 nm. *See* Ex. 1004 ¶¶ 74-76.

[4] Patent Owner, in its Preliminary Response, does not appear to dispute that Tsukamoto discloses that the DSG structure is the "same height" as the memory array proximate to the memory array. In that regard, Tsukamoto discloses that the portion of the DSG structure proximate to the memory cell, which is to the right of the DSG structure as depicted in Figure 2, includes the same individual layers as the memory cell. *See* Ex. 1004 ¶ 65; Fig. 2.

assertion that claims 7 and 14 would have been obvious over the combination of Yuzuriha, Tsukamoto, and Lin.[5]

III. CONCLUSION

We conclude, on the record before us, that Petitioner has demonstrated a reasonable likelihood of prevailing on the following ground of unpatentability asserted in the Petition: claims 7 and 14 under 35 U.S.C. § 103(a) as obvious over Yuzuriha, Tsukamoto, and Lin.

The Board, however, has not made a final determination under 35 U.S.C. § 318(a) with respect to the patentability of the challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that an *inter partes* review of claims 7 and 14 of the '027 patent is granted;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '027 patent is hereby instituted commencing on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; and

FURTHER ORDERED that the trial is limited to the following grounds: claims 7 and 14 under 35 U.S.C. § 103(a) as obvious over Yuzuriha, Tsukamoto, and Lin.

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[5] We note that Petitioner cites three additional references in its Petition: (1) S. WOLF AND R.N. TAUBER, SILICON PROCESSING FOR THE VLSI ERA: VOL. 1 – PROCESS TECHNOLOGY 727-741 (2d ed. 2000) (Ex. 1008); (2) U.S. Patent No. 5,371,030 (Ex. 1010); or (3) U.S. Patent No. 4,571,819 (Ex. 1011). The references, however, are not included in Petitioner's asserted grounds of unpatentability, and we do not consider them as such.

PETITIONER:

Michael M. Murray
Andrew R. Sommer
mmurray@winston.com
asommer@winston.com

PATENT OWNER:

J. Steven Baughman
Gabrielle E. Higgins
steven.baughman@ropesgray.com
gabrielle.higgins@ropesgray.com