

UNITED STATES PATENT AND TRADEMARK OFFICE

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MACRONIX INTERNATIONAL CO., LTD., MACRONIX ASIA  
LIMITED, MACRONIX (HONG KONG) CO., LTD. and MACRONIX  
AMERICA, INC.

Petitioners

v.

SPANSION LLC

Patent Owner

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Case No. IPR2014-00898

Patent Number 7,151,027

Before the Honorable DEBRA K. STEPHENS, JUSTIN T. ARBES, and  
RICHARD E. RICE, *Administrative Patent Judges*.

DECLARATION OF BENJAMIN J. BARRETT

I, BENJAMIN J. BARRETT, hereby certify that the following is, to the  
best of my knowledge and belief, true and accurate:

1. The document attached as Appendix A, "JP2003078040(A) [Page 1]," is  
a true and accurate translation of the cover page of "JP2003078040(A)" (copy  
attached as Appendix C) from Japanese into English.

2. The document attached as Appendix B, “JP2003078040(A) [Paragraph 0035],” is a true and accurate translation of paragraph 0035 of “JP2003078040(A)” (Appendix C) from Japanese into English.
3. The Japanese term “[少なくする]” in paragraph 0035 of “JP2003078040(A),” in the context in which it appears, should be accurately translated into English as “decrease,” as shown in Appendix B
4. I have more than fifteen years of experience in translating Japanese documents into English and more than fifteen years of experience in translating Japanese patents and patent applications into English.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on October 2, 2014 in La Conner, Washington.



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(19) Japan Patent Office (JP)

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(21) Application number	Japanese Patent Application 2001-263736 (P2001- 263736)	(71) Applicant	000005108 Hitachi Co., Ltd. 6 Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo-to
(22) Filing date	August 31, 2001 (8.31.2001)	(72) Inventor	TSUKAMOTO, Keisuke c/o Hitachi Ltd. Device Development Center, 16- 3 Shin-machi 6-chome, Ome-shi, Tokyo-to
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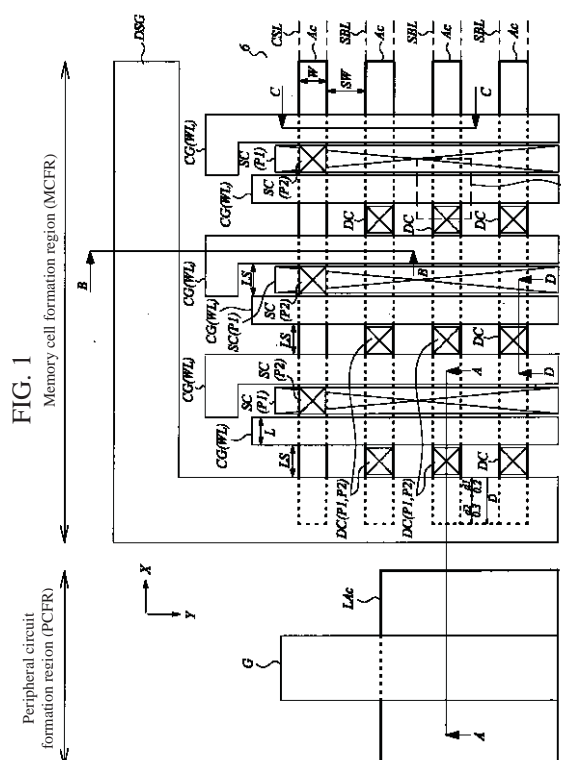
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(54) [Title of the Invention] Semiconductor integrated circuit device and fabrication method therefor

(57) [Abstract]

[Problem] To reduce defects and reduce leakage current in element formation regions in which memory cells of nonvolatile memory are formed.

[Solution] The ends of element formation region Ac in which a nonvolatile memory cell is to be formed are extended to a length D using the region below a dummy conductive film DSG, thereby concentrating the stress applied from the insulation film 6 surrounding the element formation region Ac into that extended region. As a result, defects do not extend to the region where the memory cell is to be formed, and the leakage current of the memory cell can be reduced.



[0035] Furthermore, a dummy conductive film DSG, formed in the same layer as control electrode CG, is formed in the peripheral area of the memory array. This dummy conductive film DSG is formed in order to reduce the influence of impurities generated during memory cell formation, decrease the level difference between the memory formation region and the peripheral circuit formation region, and the like.

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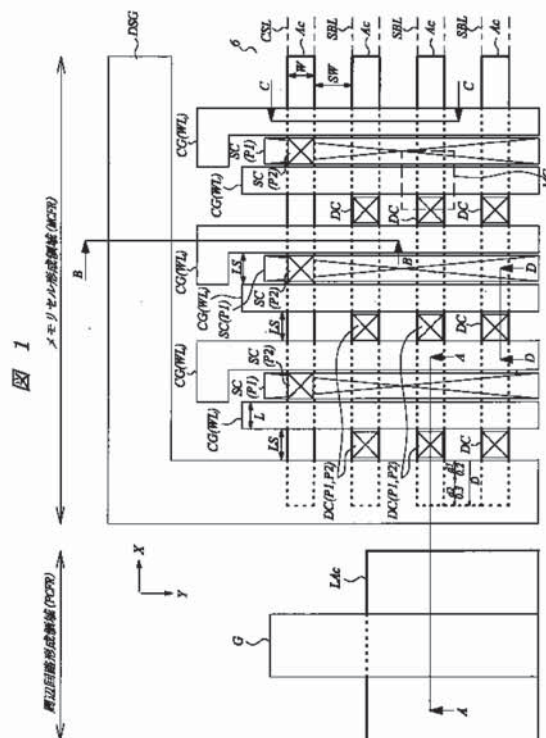
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(54) 【発明の名称】 半導体集積回路装置およびその製造方法

(57) 【要約】

【課題】 不揮発性メモリのメモリセルが形成される素子形成領域内の欠陥を低減させ、リーク電流の低減を図る。

【解決手段】 不揮発性メモリセルが形成される素子形成領域A cの端部を、ダミー導電性膜D S Gの下領域を利用して長さDだけ伸長することにより、かかる伸長した領域に、素子形成領域A cを囲む絶縁膜6から加わる応力を集中させる。その結果、メモリセルが形成される領域までは、欠陥が延びず、メモリセルのリーク電流を低減することができる。





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