

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MACRONIX INTERNATIONAL CO., LTD., MACRONIX ASIA
LIMITED, MACRONIX (HONG KONG) CO., LTD. and MACRONIX
AMERICA, INC.

Petitioners

v.

SPANSION LLC

Patent Owner

Case No. IPR2014-00898

Patent Number 7,151,027

Before the Honorable DEBRA K. STEPHENS, JUSTIN T. ARBES, and
RICHARD E. RICE, *Administrative Patent Judges*.

DECLARATION OF BENJAMIN J. BARRETT

I, BENJAMIN J. BARRETT, hereby certify that the following is, to the
best of my knowledge and belief, true and accurate:

1. The document attached as Appendix A, "JP2003078040(A) [Page 1]," is
a true and accurate translation of the cover page of "JP2003078040(A)" (copy
attached as Appendix C) from Japanese into English.

2. The document attached as Appendix B, “JP2003078040(A) [Paragraph 0035],” is a true and accurate translation of paragraph 0035 of “JP2003078040(A)” (Appendix C) from Japanese into English.

3. The Japanese term “[少なくする]” in paragraph 0035 of “JP2003078040(A),” in the context in which it appears, should be accurately translated into English as “decrease,” as shown in Appendix B

4. I have more than fifteen years of experience in translating Japanese documents into English and more than fifteen years of experience in translating Japanese patents and patent applications into English.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on October 2, 2014 in La Conner, Washington.



NAME BENJAMIN J. BARRETT
ADDRESS 713 MAPLE STREET, LA CONNER, WA 98257

[0035] Furthermore, a dummy conductive film DSG, formed in the same layer as control electrode CG, is formed in the peripheral area of the memory array. This dummy conductive film DSG is formed in order to reduce the influence of impurities generated during memory cell formation, decrease the level difference between the memory formation region and the peripheral circuit formation region, and the like.

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(71)出願人 000005108

株式会社日立製作所

東京都千代田区神田駿河台四丁目6番地

(72)発明者 塚本 恵介

東京都青梅市新町六丁目16番地の3 株式会社日立製作所デバイス開発センタ内

(72)発明者 池田 良広

東京都青梅市新町六丁目16番地の3 株式会社日立製作所デバイス開発センタ内

(74)代理人 100080001

弁理士 筒井 大和

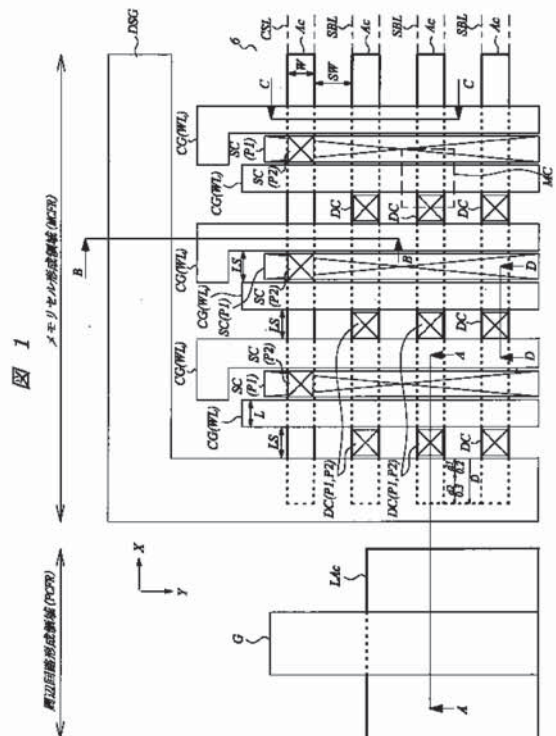
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(54)【発明の名称】 半導体集積回路装置およびその製造方法

(57)【要約】

【課題】 不揮発性メモリのメモリセルが形成される素子形成領域内の欠陥を低減させ、リーク電流の低減を図る。

【解決手段】 不揮発性メモリセルが形成される素子形成領域A cの端部を、ダミー導電性膜D S Gの下の領域を利用して長さDだけ伸長することにより、かかる伸長した領域に、素子形成領域A cを囲む絶縁膜6から加わる応力を集中させる。その結果、メモリセルが形成される領域までは、欠陥が延びず、メモリセルのリーク電流を低減することができる。



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