

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MACRONIX INTERNATIONAL CO., LTD., MACRONIX ASIA LIMITED,
MACRONIX (HONG KONG) CO., LTD. and MACRONIX AMERICA, INC.
Petitioners

v.

SPANSION LLC
Patent Owner

Case No. IPR2014-00898
Patent Number 7,151,027

Before the Honorable DEBRA K. STEPHENS, JUSTIN T. ARBES, and
RICHARD E. RICE, *Administrative Patent Judges*.

DECLARATION OF SHUKRI SOURI, Ph.D.

I, Shukuri Souri, hereby declare under penalty of perjury under the laws of the United States of America:

I. Qualifications

1. I am currently a Corporate Vice President at Exponent, Inc. (“Exponent”), an engineering and scientific consulting firm, headquartered at 149 Commonwealth Drive, Menlo Park, California 94025. I am based in, and the Director of, Exponent’s New York office. I am also the Director of Exponent’s Electrical Engineering and Computer Science practice.

2. I received a Master’s Degree in Electrical Engineering from Stanford University in 1994, and a Ph.D. in Electrical Engineering, also from Stanford University, in 2003. I have extensive experience with semiconductor devices, including the design, fabrication, modeling, measurement, and testing of integrated circuits. While at Stanford University, I taught several courses on integrated circuit fabrication, optical fiber communications, and networking. Before joining Stanford, I was a member of the staff at Raychem Corporate Research and Development Laboratories, where I worked on semiconductor materials and electrical circuit protection devices. I am a named inventor on four U.S. patents related to semiconductor processes, devices, and integrated circuits.

3. My education, experience, and qualifications, including a list of my publications and a list of matters in which I have testified as an expert, are set forth in my curriculum vitae, attached hereto as EX2006. My opinions, as expressed in this

report, are based on my education, career, and relevant experience, as well as the materials reviewed.

4. I have been retained on behalf of Patent Owner Spansion LLC to offer statements and opinions regarding the understanding of a person of ordinary skill in the art (discussed below) as it relates to U.S. Patent No. 7,151,027 (the '027 Patent) assigned to Patent Owner, as well as other references presented to me by counsel for Patent Owner.

5. I am a salaried employee of Exponent. Exponent charges an hourly rate of \$495 plus expenses for my work performed in connection with this *Inter Partes* Review. I have received no additional compensation for my work in this *Inter Partes* Review, and my compensation does not depend on the contents of this report, any testimony I provide, or the ultimate outcome of this *Inter Partes* Review.

II. Materials Considered

6. In developing my opinions below relating to the '027 Patent, I have considered the following materials:

- U.S. Patent No. 7,151,027 (Exhibit MX027II-1001);
- Corrected Petition for *Inter Partes* Review of U.S. Patent No. 7,151,027 (“Petition” or “Pet.”) (Paper No. 6);
- Patent Owner’s Preliminary Response (Paper No. 12);
- Decision – Institution of *Inter Partes* Review (Paper No. 13) (“ID”);
- Declaration of Dhaval J. Brahmbhatt (Exhibit MX027II-1002);

- U.S. Patent No. 6,458,655 to Yuzuriha, *et al.* (“Yuzuriha”) (Exhibit MX027II-1003);
- U.S. Patent Application Publication No. 2003/0042520 to Tsukamoto (Exhibit MX027II-1004);
- C.-F. Lin *et al.*, *A ULSI shallow trench isolation process through the integration of multilayered dielectric process and chemical-mechanical planarization*, THIN SOLID FILMS 248-52 (1999) (Exhibit MX027II-1007);
- S. Wolf & R.N. Tauber, *Silicon Processing for the VLSI Era: Vol. 1 – Process Technology* 2d Ed. (Lattice Press 2000) (Exhibit MX027II-1008);
- CV of Dhaval J. Brahmbhatt (Exhibit MX027II-1009);
- U.S. Patent No. 5,371,030 to Bergemont (“Bergemont”) (Exhibit MX027II-1010);
- U.S. Patent No. 4,571,819 to Rogers *et al.* (“Rogers”) (Exhibit MX027II-1011);
- Excerpts of Transcript of Videotaped Deposition of Dr. Dhaval Brahmbhatt (July 2, 2014) (EX2005);
- Transcript of Videotaped Deposition of Dr. Dhaval Brahmbhatt (July 3, 2014) (EX2004);
- Transcript of Videotaped Deposition of Mr. Dhaval Brahmbhatt (September 24, 2014) (EX2008) and Deposition Exhibits (EX2000 – EX2003);
- Yuzuriha *et al.*, *A 14-ns 1-Mbit CMOS SRAM with Variable Bit Organization*, IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, October 1988 (EX2009);
- Certified Translation of Excerpts of JP 2003-078040 and Accompanying Appendices (EX2010);
- All other materials referenced herein.

III. Level of Ordinary Skill for the '027 Patent

7. I understand that the factors that may be considered in determining the ordinary level of skill in the art include: (1) the levels of education and experience of

persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology. I understand that a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above.

8. It is my opinion that at least as of June 1, 2004, the filing date of the '027 Patent, a person of ordinary skill in the art would have had a Bachelor's of Science degree in materials science, electrical engineering, physics or the equivalent and about two years of processing experience related to memory device fabrication.

9. I note that Mr. Brahmhatt has opined that "a person of ordinary skill in the art would have a bachelor's degree in Electrical Engineering and 2-3 years of experience in design or fabrication of semiconductor memories. An individual with additional education or industry experience could also be one of ordinary skill in the art if that additional experience compensated for a deficit in the other aspect stated above." MX027II-1002 at ¶ 28.

10. Unless otherwise stated, when I state that something would be known or understood by a person of ordinary skill in the art, I am referring to a person with the level of education and experience expressed in ¶¶ 8-9 above, as of June 1, 2004. As described above and in my CV (EX2006), I have decades of experience with semiconductor devices, including the design and fabrication of memory devices. As of June 1, 2004, I would have qualified as one of ordinary skill in the art according to

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