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Paper 13
Entered: August 13, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MACRONIX INTERNATIONAL CO., LTD.,
MACRONIX ASIA LIMITED, MACRONIX (HONG KONG) CO., LTD.,
and MACRONIX AMERICA, INC.,
Petitioner,

v.

SPANSION LLC,
Patent Owner.

Case IPR2014-00898
Patent 7,151,027 B1

Before DEBRA K. STEPHENS, JUSTIN T. ARBES, and
RICHARD E. RICE, *Administrative Patent Judges.*

RICE, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Macronix International Co., Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. (collectively "Petitioner") filed a Corrected Petition (Paper 6, "Pet.") to institute an *inter partes* review of claims 7 and 14 of U.S. Patent No. 7,151,027 B1 (Ex. 1001, "the '027 patent") pursuant to 35 U.S.C. §§ 311-319. Pet. 1. Patent Owner Spansion LLC ("Patent Owner") filed a Preliminary Response (Paper 12, "Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314. For the reasons that follow, the Board has determined to institute an *inter partes* review.

I. BACKGROUND

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a):

> THRESHOLD—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Petitioner challenges claims 7 and 14 as unpatentable under 35 U.S.C. § 103(a). Pet. 4. We grant the Petition, as discussed below.

A. Related Proceedings

Petitioner discloses that the '027 patent is asserted in: (1) *Spansion LLC v. Macronix International Co., Ltd.*, Civ. No. 3:13-cv-03566 (N.D. Cal.); and (2) *In re Flash Memory Chips and Products Containing Same*, Inv. No. 337-TA-893 (U.S. Int'l Trade Comm'n). *Id.* at 2.

Petitioner also discloses that the '027 patent is involved in IPR2014-00108, captioned *Macronix International Co., Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. v. Spansion LLC*, in which we instituted an *inter partes* review of claims 1-6 and 8-13, but not claims 7 and 14. *Id.*

B. The '027 Patent (Ex. 1001)

Figures 3A-3G of the '027 patent illustrate steps in a process for forming an interface structure between a memory array and a periphery of a memory device. *See* Ex. 1001, 3:18-22, 54-57. At the step illustrated in Figure 3D of the '027 patent, which is reproduced below, "second polysilicon layer (poly-2) 320" is deposited above dielectric material 315 and substrate 300. *Id.* at 4:22-24.

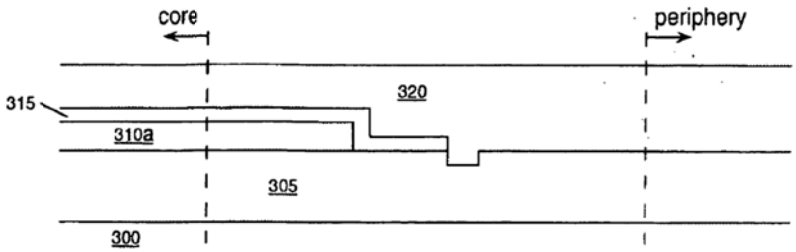

Figure 3D

A vertical dashed line on the left of Figure 3D denotes the approximate border between a memory array ("core") and an interface area, and a vertical dashed line on the right of the figure denotes the approximate border between the interface area and a periphery. *See id.* at 3:54-57 (referring to Figure 3A). As depicted in Figure 3D, first polysilicon layer 310a, referred to as "gate polysilicon ('poly-1') 310a" in the '027 patent, is disposed beneath dielectric material 315. *Id.* at 3:50-53. Figure 3D also

depicts substrate 300, isolation area 305, and second polysilicon layer 320 ("poly-2"). *See id.* at 3:51-52 (referring to Figure 3A); 4:22-25.

Figure 3E of the '027 patent, which is reproduced below, depicts the step of etching a portion of poly-1 layer 310a, dielectric material layer 315, and poly-2 layer 320, proximate to the memory array. *Id.* at 4:27-30.

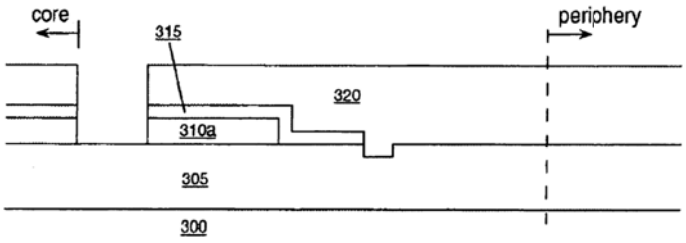

Figure 3E

The '027 patent discloses that "a known process (such as a stacked gate etch)" is used for the etching step in Figure 3E. *Id.*

Figure 3F of the '027 patent, which is reproduced below, depicts the step of etching a portion of poly-2 layer 320 proximate to the periphery. *Id.* at 4:38-40. As described in the '027 patent, "a known process (such as a second gate etch)" is used for the etching step depicted in Figure 3F. *Id.* The etching step is used to form interface structure 360, which is illustrated in Figure 3F. *Id.* at 4:41.

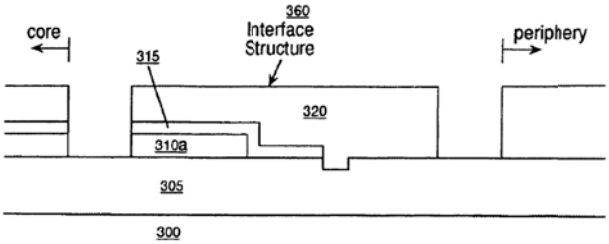

Figure 3F

As depicted in Figure 3F and described in the '027 patent, "interface structure 360 is the same height as the memory array proximate to the memory array and the same height as the periphery proximate to the periphery, such that step size is smoothed out reducing the occurrence of stringers from spacer etching." *Id.* at 4:49-54.

C. Illustrative Claim

Claims 1 and 8 are independent. Claim 7 depends directly from claim 1, and claim 14 depends directly from claim 8. Challenged claims 7 and 14 recite similar limitations. Claims 8 and 14, which are reproduced below, are illustrative:

> 8. A method for fabricating a memory device, said method comprising:
>
> forming a poly-1 layer above a substrate at an interface between a memory array and a periphery of said memory device;
>
> forming a poly-2 layer above said poly-1 layer at said interface;
>
> etching said poly-1 layer and said poly-2 layer proximate to said memory array; and
>
> etching said poly-2 layer proximate to said periphery, such that an interface structure including a portion of said poly-1 layer and a portion of said poly-2 layer remains at said interface.

> 14. The method as recited in claim 8 wherein said interface structure is a same height as said memory array proximate to said memory array and a same height as said periphery

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