United States Patent [19]

Rogers et al.

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[45] **Date of Patent: Feb. 25, 1986**

[54] **METHOD FOR FORMING TRENCH ISOLATION STRUCTURES**

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[73] Assignee: **NCR Corporation,** Dayton, Ohio

[21] Appl. No.: **667,181**

[22] Filed: **Nov. 1, 1984**

[51] **Int. Cl.**[4] **H01L 21/95**

[52] **U.S. Cl.** .... **29/576 W;** 29/580; 148/1.5; 148/191; 148/DIG. 43; 148/DIG. 50; 148/DIG. 133; 357/49; 357/50; 357/54; 156/653; 427/93

[58] **Field of Search** .... 29/576 W, 576 T, 580; 148/1.5, 191, DIG. 43, DIG. 50, DIG. 85, DIG. 86, DIG. 133; 357/49, 50, 54; 156/653, 657; 427/86, 93, 94, 95

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Rung et al., "Deep Trench Isolated CMOS Devices", IEDM 82, pp. 237–240.

Kurosawa et al., "A New Bird's-Beak Free Field Isolation Technology for VLSI Devices", IEDM 81, pp. 384–387.

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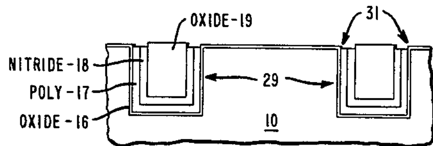
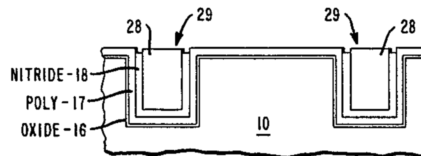
Assistant Examiner—Alan E. Schiavelli
Attorney, Agent, or Firm—Wilbert Hawk, Jr.; Casimer K. Salys

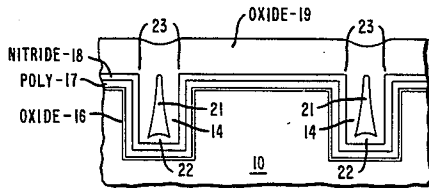
[57] **ABSTRACT**

A method for forming trench isolation oxide using doped silicon dioxide which is reflowed at elevated temperatures to collapse any voids therein and produce surface planarity. An underlying layered composite selected from oxide, polysilicon and silicon nitride permits the formation and reflow of the doped isolation oxide and remains in place in the trench to contribute to the trench isolation structure.

16 Claims, 10 Drawing Figures







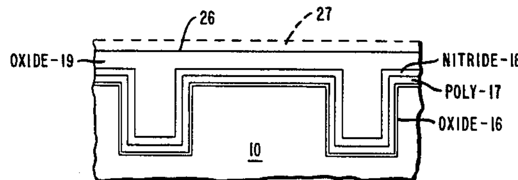


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FIG. 1

PRIOR ART

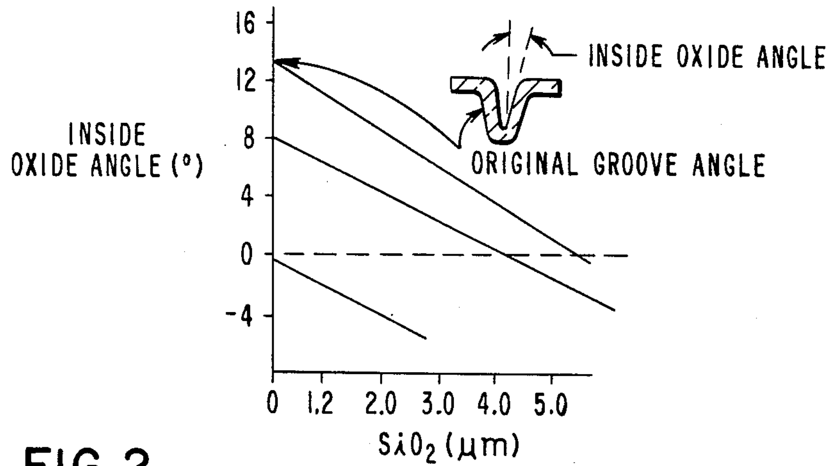

FIG. 2

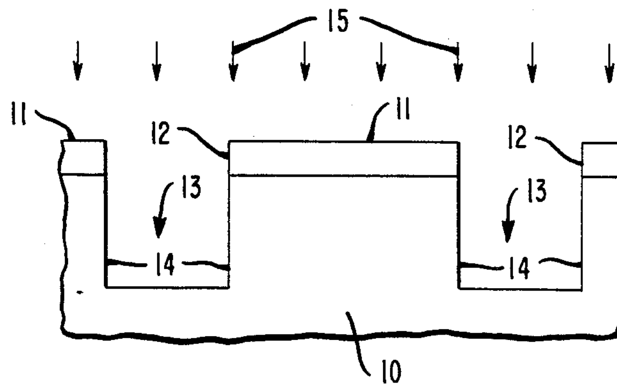

FIG. 3

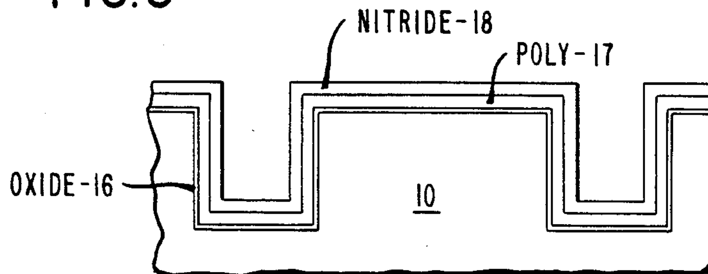

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FIG. 3A

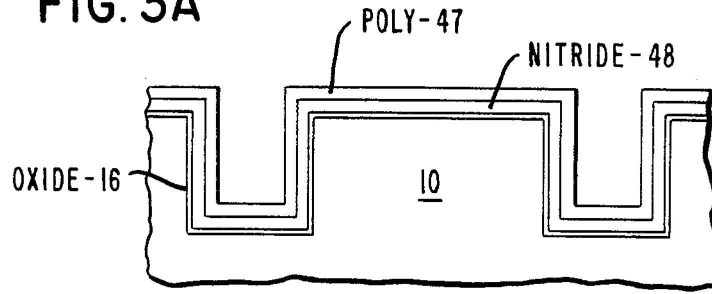

FIG. 3B

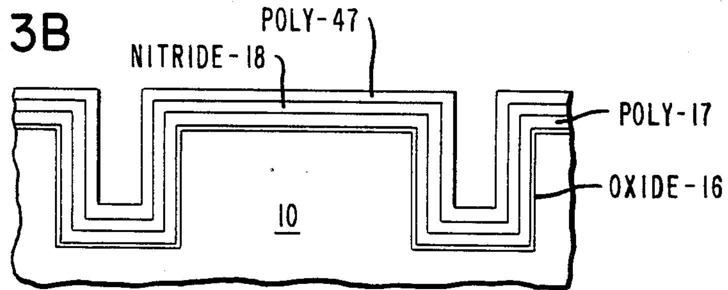

FIG. 4

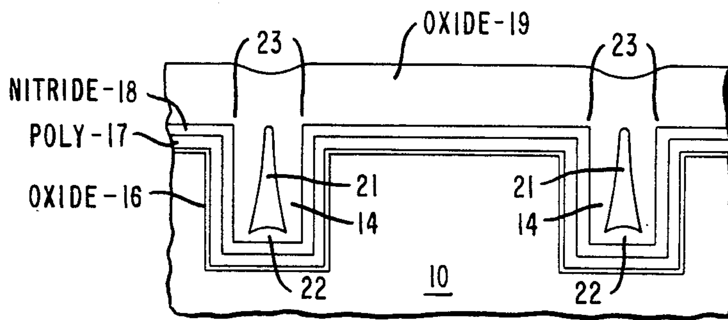

FIG. 5

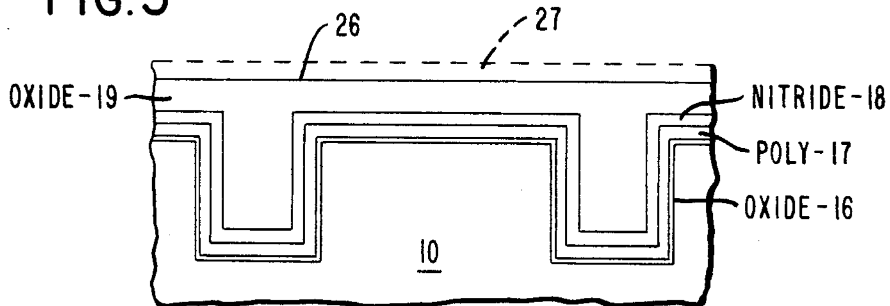

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FIG. 6

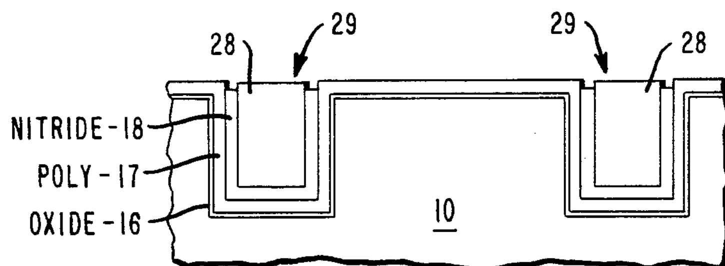


FIG. 7

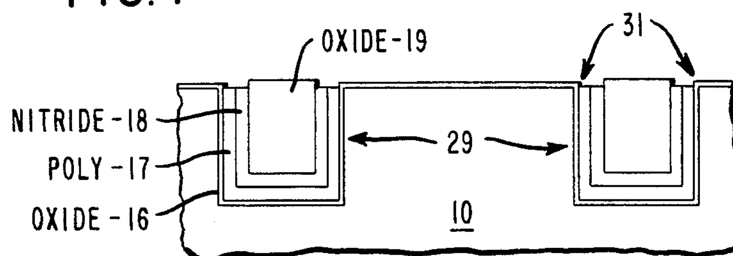
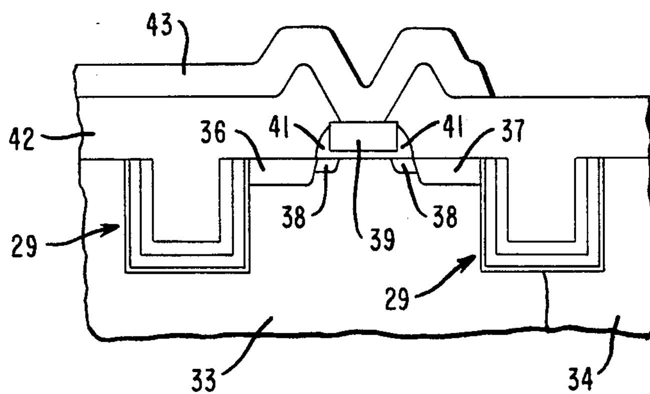


FIG. 8



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METHOD FOR FORMING TRENCH ISOLATION STRUCTURES

BACKGROUND OF THE INVENTION

This invention relates to techniques for electrically isolating semiconductor devices and components in monolithic integrated circuits. In particular, the invention is a method for forming void-free, planarized dielectric trench structures. The method uses doped oxide reflow to provide a void-free planar isolation layer and a multiple underlayer which functions as an etch stop and dopant/oxidation barrier.

Dielectric isolation techniques have been the preferred technology for isolating integrated circuits and their constituent devices and elements, at least in part because of the ability to closely pack the isolation dielectric and the circuit elements. Integrated circuit isolation by the so-called local oxidation of silicon (LOCOS) has been known for a number of years, as have the attendant problems. The well-known limitations of the LOCOS process include at least three factors which may constrain the process from applicability to future small geometry, highly dense LSI and VLSI structures. These limitations are, first, the formation of the so-called bird's beak oxide configuration and the associated encroachment of the field oxide beneath the oxidation mask. Encroachment by the bird's beak oxide limits the percentage of chip surface area which is available for device formation. Secondly, the limited thickness results in undesirably high circuit capacitances. Third, the characteristic non-planar surface topography makes it difficult to perform the increasingly high resolution photolithographic operations which are required to fabricate VSLI circuits. In turn, the decreased resolution increases the minimum feature sizes and minimum tolerances and, as a consequence, decreases the achievable device densities.

The use of LOCOS isolation has persisted, however, because of the past shortcomings of the available substitute isolation technologies. Typical trench isolation processes involve etching grooves about 1 to 6 microns deep into the semiconductor substrate, filling the grooves with a suitable dielectric and performing a planarization operation. The dielectric material typically is undoped silicon dioxide or polysilicon. Typical prior art approaches are discussed, for example, in Rung, Momose and Nagakubo, "Deep Trench Isolated CMOS Devices", *IEDM* 82, pp. 237–240. The Rung et al. article discusses a trench isolation process which involves oxidizing the silicon substrate trench sidewalls, filling the trench with polysilicon or deposited oxide, etching the poly/oxide, then capping the structure with oxide. Another typical trench isolation approach is described in the article "A New Bird's-Beak Free Field Isolation Technology For VLSI Devices", by Kurosawa, Shibata and Iizuka, *IEDM* 81, pp. 384–387. The Kurosawa et al. technique involves the selective etching of stressed silicon dioxide following confomal deposition, combined with a lift-off of the silicon dioxide over the active regions.

In particular, trench isolation technology has the inherent potential advantages of small width-to-depth ratios, relative process simplicity, well-defined vertical-wall isolation regions and surface planarity. Like other VSLI features, however, the width of isolation trenches must be scaled downward to near micron and even submicron size to achieve the densities required in VSLI and future monolithic integrated circuit technologies. Unfortunately, it becomes increasingly difficult to completely fill the narrow, yet relatively deep trench configurations which are used for VSLI isolation. The resulting tendency to form voids is well-known and is shown, for example, by the data of Bondur et al, U.S. Pat. No. 4,104,086. Bondur et al. discloses a process for eliminating voids by precisely tapering the walls of the trenches, which tapers vary in relation to the sizes of the trenches. FIG. **1** illustrates the data of Bondur et al., which show that for vertical side wall trenches, the deposited silicon dioxide forms negative sloping side walls and, thus, voids.

Several approaches have been proposed which have as their purpose the control or elimination of such voids.

For example, Riseman, U.S. Pat. No. 4,356,211, forms a composite dual-oxide trench isolation structure in which a first oxide layer is formed, then a layer of polysilicon is deposited, anisotrophically etched, and heavily doped at the upper edge of the trench to accelerate silicon dioxide formation at such upper edge. Thereby the voids are sealed by the differential oxidation rate of the polysilicon. Clearly the parameters of the Riseman process do not provide for applications in which trenches of varying dimension are being processed simultaneously.

The above-mentioned Bondur et al. U.S. Pat. No. 4,104,086 uses tapered trench sidewalls to control the depth of isolation oxide voids relative to the substrate surface in a silicon substrate which has a highly doped near-surface region. Briefly, the Bondur et al process involves (1) forming the trench to a tapered profile, as by the use of reactive ion etching (RIE); (2) growing a thin layer of thermal oxide in the trench outline; (3) depositing CVD oxide; (4) etching back the CVD oxide using RIE; and (5) optionally, annealing in steam at 900° to 950° C. to enhance the "quality" of the silicon dioxide. The data disclosed in the Bondur et al patent indicate the vertical walls (which, of course, are desirable for density and resolution) inherently product voids in the deposited silicon oxide (see FIG. **1** herein). Also, the voids are buried deeper in the oxide relative to the substrate surface as the trench width increases and the taper increases. Conversely, the voids are formed closer to the surface and to exposure by the planarization etch-back in the case of narrower, vertical grooves.

Sakurai, U.S. Pat. No. 4,404,735, discloses a process for forming trench isolation structures. Initially, dry etching such as plasma etching, reactive sputter etching or ion beam etching is used for form the trench. The trench is then covered with a thin layer of deposited silicon dioxide which is formed to a thickness of between 500 to 1,000 angstroms to prevent substrate heating by the subsequent laser reflow process, prevent doping of the substrate from the isolation layer, and to isolate the silicon isolation layer from the substrate. Next, a CVD layer is formed to a thickness which is less than the trench depth and less than one-half the trench width using silicon or doped glass (phosphosilicate glass, PSG). The PSG/silicon is subsequently reflowed by laser heating. Essentially, the Sakurai process is a laser reflow process for filling narrow trenches from a thin silicon or PSG layer. In other words, the trench-filling layer is formed to an initial shallow thickness within the trench and laser heating is used to redistribute material from outside the trenches into the trenches.

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