Silicon Processing

for the VLSI Era

Volume 1 - Process Technology

Second Edition

S. Wolf and R.N. Tauber

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Table 15.4 DESIRED PROPERTIES OF INTERLEVEL DIELECTRICS FOR VLSI [7]

1. Low dielectric constant for frequencies up to ~20 MHz, in order to keep capacitance between metal lines low;
2. High breakdown field strength (> 5 MV/cm);
3. Low leakage, even under electric fields close to the breakdown field strength. Bulk resistivity should exceed 10^{15} Ω-cm.;
4. Low surface conductance, surface resistivity should be >10^{15} Ω-cm;
5. No moisture absorption or permeability to moisture should occur;
6. Films should exhibit low stress, and the preferred stress is compressive (~5x10^8 dynes/cm^2), since dielectric films under tensile stress exhibit more of a tendency to crack;
7. Good adhesion to aluminum, and of aluminum to the dielectric. (Good adhesion is also needed to the other conductors used in ULSI, such as doped polysilicon and silicides.) In cases of poor adhesion (such as with Cu or W), a glue layer (such as Ti or TiN) may need to be applied between the conductor and the dielectric;
8. Good adhesion to dielectric layers above or below. Such dielectric layers could be thermal oxides, doped-CVD oxides, nitrides, oxynitrides, polyimides, or spin-on glasses;
9. Stable up to temperatures of 500°C;
10. Easily etched (by wet or dry processing).
11. Permeable to hydrogen. This is important for IC processing, in which an anneal in a hydrogen containing ambient must be used to reduce the concentration of interface states between Si and the gate oxides of MOS devices (see Chap. 8);
12. No incorporated electrical charge or dipoles, some polyimides in particular contain polar molecules that can orient themselves in an electric field and give rise to an electric field even when the externally applied field is removed;
13. Contains no metallic impurities;
14. Step coverage that does not produce reentrant angles;
15. Good thickness uniformity across the wafer, and from wafer to wafer.
16. In the case of doped oxides, good dopant uniformity across the wafer, and from wafer to wafer;
17. Low defect density (pinholes and particles);
18. Contains no residual constituents that outgas during later processing to the degree that they degrade the properties of other layers of the interconnect system (e.g., outgassing from some polyimide films, SOG films, or low-temperature TEOS films)

Pre-metal dielectric (PMD) films can be flowed and reflowed at temperatures in excess of 800°C. However, when Al is present on the wafer surface, the maximum temperature of the intermetal dielectric layers is limited to ~450°C.

15.3 PLANARIZATION OF INTERLEVEL DIELECTRIC LAYERS

As pointed out in the chapter introduction, the planarization of interlevel dielectrics is one of three critical issues that must be addressed when implementing a multilevel interconnect system for VLSI applications. This assertion is now justified and the various approaches developed for dealing with this issue are described.

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15.3.1 Terminology of Planarization in Multilevel Interconnects

As additional levels are added to multilevel-interconnection schemes and circuit features are scaled to submicron dimensions, the required degree of planarization is increased. Such planarization can be implemented in either the conductor or the dielectric layers. In this section processes developed to planarize dielectric layers are described. In later sections, techniques for planarizing conductor layers and vias will be considered.

The term planarization is employed quite frequently (and loosely) both here and in other technical literature. Therefore it is useful to define this term more completely, especially as it applies to planarization of dielectric layers in multilevel-interconnect technology. The example case used for this discussion is that of a dielectric layer (IMD) deposited after Metal 1 is patterned. In the case where no planarization exists (Fig. 15-4a), the step heights on the DM1 surface closely approximate the step heights of the Metal 1 layer and the underlying topography. Furthermore, in this case the steps on the IMD surface also have steep slopes (i.e., vertical, or even reentrant).

15.3.1.1 Degree of Planarization: The steps on the surface of DM1 can be made less severe through various planarization processes. The degree to which this can be successfully accomplished differs according to the technique used. The degree of planarization is classified according to the following qualitative planarization criteria:

1. The first degree of planarization (smoothing) involves a lessening of the step slopes at the IMD surface (Fig. 15-4b). The step heights in this case, however, are not significantly reduced in magnitude.
2. In the second degree of planarization (partial or semi-planarization) the step heights are reduced (but not eliminated), and the slopes of the steps are also smoothed (Fig. 15-4c).
3. In the third degree of planarization (complete local planarization), the steps at the surface of IMD are completely eliminated wherever the spaces in the underlying topography are relatively close together (e.g., <10 μm apart), but the steps at isolated, wide features still exhibit a step (Fig. 15-4d).
4. In the fourth degree of planarization (complete global planarization), the surface of the IMD is completely planarized over arbitrary topography (Fig. 15-4e).

A quantitative measure of the step-height reduction, referred to as the planarization factor, β, is given by[8]

$$\beta = 1 - (t^f_{step}/t^i_{step}) \qquad \textbf{(15.4)}$$

where t^i_{step} and t^f_{step} are the initial and final step heights, respectively. In complete-planarization cases, $\beta = 1$. If no planarization (or only smoothing) exists, then $\beta = 0$.

15.3.1.2 The Need for Dielectric Planarization: As the number of levels in an interconnect technology is increased, the stacking of additional layers on top of one another produces a more and more rugged topography. Consider, for example, a two-level metal, single-poly CMOS process. Assume the step height of the semi-recessed field oxide is 0.3 μm, and the thicknesses of the poly and the first and second metals are 0.4, 0.5 and 1.0 μm, respectively. The maximum height of the steps on the wafer surface after each of these processes will be 0.3, 0.7, 1.2, and

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