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Product Brief

MC68360 QUad Integrated Communication Controller (QUICC™)

INTRODUCTION

The MC68360 QUad Integrated Communication Controller (QUICC™) is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in communications activities. The QUICC (pronounced “quick”) can be described as a next-generation MC68302 with higher performance in all areas of device operation, increased flexibility, major extensions in capability, and higher integration. The term "quad" comes from the fact that there are four serial communications controllers (SCCs) on the device; however, there are actually seven serial channels: four SCCs, two serial management controllers (SMCs), and one serial peripheral interface (SPI).

QUICC Key Features

The following list summarizes the key MC68360 QUICC features:

- CPU32+ Processor (4.5 MIPS at 25 MHz)
  - — 32-Bit Version of the CPU32 Core (Fully Compatible with the CPU32)
  - — Background Debug Mode
  - — Byte-Misaligned Addressing
- Up to 32-Bit Data Bus (Dynamic Bus Sizing for 8 and 16 Bits)
- Up to 32 Address Lines (At Least 28 Always Available)
- Complete Static Design (0–25-MHz Operation)
- Slave Mode To Disable CPU32+ (Allows Use with External Processors)
  - — Multiple QUICCs Can Share One System Bus (One Master)
  - — MC68040 Companion Mode Allows QUICC To Be an MC68040 Companion Chip and Intelligent Peripheral (22 MIPS at 25 MHz)
  - — Also Supports External MC68030-Type Bus Masters
  - — All QUICC Features Usable in Slave Mode
- Memory Controller (Eight Banks)
  - — Contains Complete Dynamic Random-Access Memory (DRAM) Controller
  - — Each Bank Can Be a Chip Select or Support a DRAM Bank
  - — Up to 15 Wait States
  - — Glueless Interface to DRAM Single In-Line Memory Modules (SIMMs), Static Random-Access

Memory (SRAM), Electrically Programmable Read-Only Memory (EPROM), Flash EPROM, etc.
  - Four CAS lines, Four WE lines, One OE line
  - Boot Chip Select Available at Reset (Options for 8-, 16-, or 32-Bit Memory)
  - Special Features for MC68040 Including Burst Mode Support
- Four General-Purpose Timers
  - Superset of MC68302 Timers
  - Four 16-Bit Timers or Two 32-Bit Timers
  - Gate Mode Can Enable/Disable Counting
- Two Independent DMAs (IDMAs)
  - Single Address Mode for Fastest Transfers
  - Buffer Chaining and Auto Buffer Modes
  - Automatically Performs Efficient Packing
  - 32-Bit Internal and External Transfers
- System Integration Module (SIM60)
  - Bus Monitor
  - Double Bus Fault Monitor
  - Spurious Interrupt Monitor
  - Software Watchdog
  - Periodic Interrupt Timer
  - Low Power Stop Mode
  - Clock Synthesizer
  - Breakpoint Logic Provides On-Chip Hardware Breakpoints
  - External Masters May Use On-Chip Features Such As Chip Selects
  - On-Chip Bus Arbitration with No Overhead for Internal Masters
  - IEEE 1149.1 Test Access Port
- Interrupts
  - Seven External IRQ Lines
  - 12 Port Pins with Interrupt Capability
  - 16 Internal Interrupt Sources
  - Programmable Priority Between SCCs
  - Programmable Highest Priority Request
- Communications Processor Module (CPM)
  - RISC Controller
  - Many New Commands (e.g., Graceful Stop Transmit, Close RxBD)
  - 224 Buffer Descriptors
  - Supports Continuous Mode Transmission and Reception on All Serial Channels
  - 2.5 Kbytes of Dual-Port RAM
  - 14 Serial DMA (SDMA) Channels
  - Three Parallel I/O Registers with Open-Drain Capability
  - Each Serial Channel Can Have Its Own Pins (NMSI Mode)
- Four Baud Rate Generators
  - Independent (Can Be Connected to Any SCC or SMC)
  - Allows Changes During Operation
  - Autobaud Support Option

- Four SCCs
  - Ethernet/IEEE 802.3 Optional on SCC1 (Full 10-Mbps Support) (Available only on the MC68EN360)
  - HDLC/SDLC™ (All Four Channels Supported at 2 Mbps)
  - HDLC Bus (Implements an HDLC-Based Local Area Network (LAN))
  - AppleTalk®
  - Signaling System #7
  - Universal Asynchronous Receiver Transmitter (UART)
  - Synchronous UART
  - Binary Synchronous Communication (BISYNC)
  - Totally Transparent (Bit Streams)
  - Totally Transparent (Frame Based with Optional Cyclic Redundancy Check (CRC))
  - Profibus (RAM Microcode Option)
  - Asynchronous HDLC (RAM Microcode Option) to Support PPP (Point to Point Protocol)
  - DDCMP™ (RAM Microcode Option)
  - V.14 (RAM Microcode Option)
  - X.21 (RAM Microcode Option)
- Two SMCs
  - UART
  - Transparent
  - General Circuit Interface (GCI) Controller
  - Can Be Connected to the Time-Division Multiplexed (TDM) Channels
- One SPI
  - Superset of the MC68302 SCP
  - Supports Master and Slave Modes
  - Supports Multimaster Operation on the Same Bus
- Time-Slot Assigner
- Supports Two TDM Channels
  - Each TDM Channel Can Be T1, CEPT, PCM Highway, ISDN Basic Rate, ISDN Primary Rate, User Defined
  - 1- or 8-Bit Resolution
  - Allows Independent Transmit and Receive Routing, Frame Syncs, Clocking
  - Allows Dynamic Changes
  - Can Be internally Connected to Six Serial Channels (Four SCCs and Two SMCs)
- Parallel Interface Port
  - Centronics™ Interface Support
  - Supports Fast Connection Between QUICCs
- 240 Pins Defined: 241-Lead Pin Grid Array (PGA) and 240-Lead Plastic Quad Flat Pack (PQFP)

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QUICC ARCHITECTURE OVERVIEW

The QUICC is 32-bit controller that is an extension of other members of the Motorola M68300 family. Like other members of the M68300 family, the QUICC incorporates the intermodule bus (IMB). (The MC68302 is an exception, having an M68000 bus on chip.) The IMB provides a common interface for all modules of the M68300 family, which allows Motorola to develop new devices more quickly by using the library of existing modules. Although the IMB definition always included an option for an on-chip 32-bit bus, the QUICC is the first device to implement this option.

The QUICC is comprised of three modules: the CPU32+ core, the SIM60, and the CPM. Each module utilizes the 32-bit IMB. The MC68360 QUICC block diagram is shown in Figure 1.

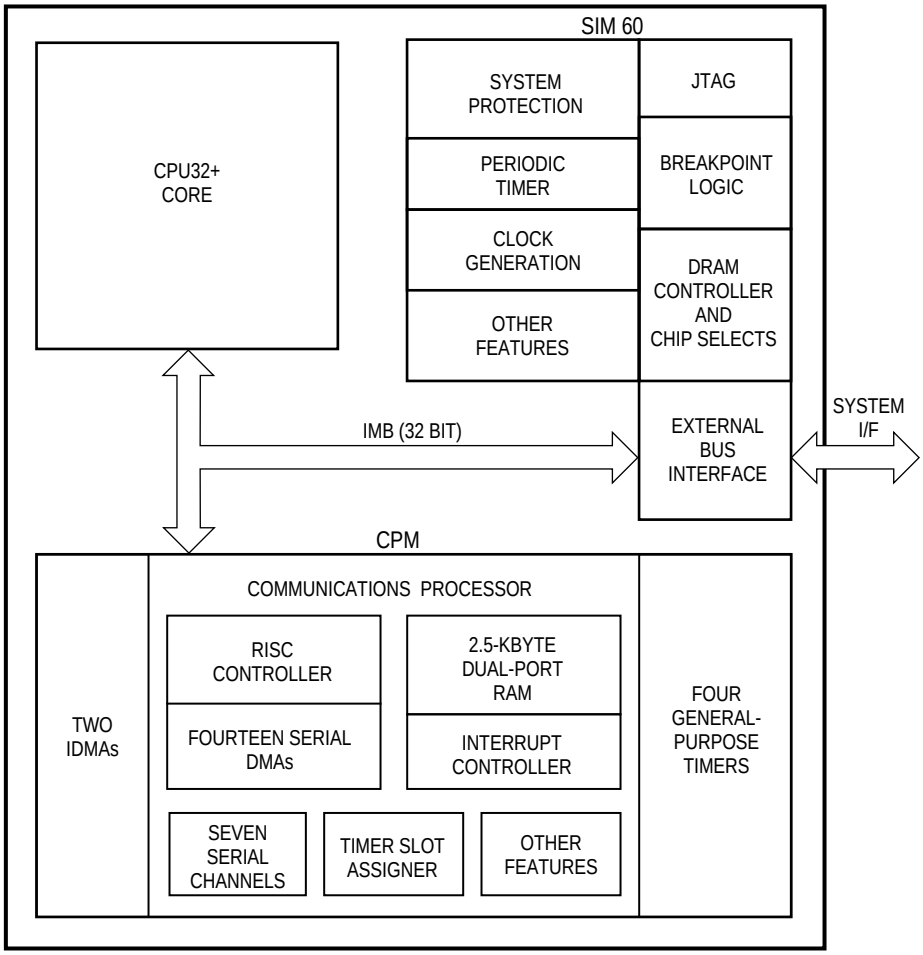

Figure 1. QUICC Block Diagram

CPU32+ Core

The CPU32+ core is a CPU32 that has been modified to connect directly to the 32-bit IMB and apply the larger bus width. Although the original CPU32 core had a 32-bit internal data path and 32-bit arithmetic hardware, its interface to the IMB was 16 bits. The CPU32+ core can operate on 32-bit external operands with one bus cycle. This allows the CPU32+ core to fetch a long-word instruction in one bus cycle and to

fetch two word-length instructions in one bus cycle, filling the internal instruction queue more quickly. The CPU32+ core can also read and write 32-bits of data in one bus cycle.

Although the CPU32+ instruction timings are improved, its instruction set is identical to that of the CPU32. It will also execute the entire M68000 instruction set. It contains the same background debug mode (BDM) features as the CPU32. No new compilers, assemblers, or other software support tools need be implemented for the CPU32+; standard CPU32 tools can be used.

The CPU32+ delivers approximately 4.5 MIPS at 25 MHz, based on the standard (accepted) assumption that a 10-MHz M68000 delivers 1 VAX MIPS. If an application requires more performance, the CPU32+ can be disabled, allowing the rest of the QUICC to operate as an intelligent peripheral to a faster processor. The QUICC provides a special mode called MC68040 companion mode to allow it to conveniently interface to members of the M68040 family. This two-chip solution provides a 22-MIPS performance at 25 MHz.

The CPU32+ also offers automatic byte alignment features that are not offered on the CPU32. These features allow 16 or 32-bit data to be read or written at an odd address. The CPU32+ automatically performs the number of bus cycles required.

System Integration Module (SIM60)

The SIM60 integrates general-purpose features that would be useful in almost any 32-bit processor system. The term “SIM60” is derived from the QUICC part number, MC68360. The SIM60 is an enhanced version of the SIM40 that exists on the MC68340 and MC68330 devices.

First, new features, such as a DRAM controller and breakpoint logic, have been added. Second, the SIM40 was modified to support a 32-bit IMB as well as a 32-bit external system bus. Third, new configurations, such as slave mode and internal accesses by an external master, are supported.

Although the QUICC is always a 32-bit device internally, it may be configured to operate with a 16-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode and 8- and 16-bit peripherals and memory to exist in the 16-bit system bus mode.

Communications Processor Module (CPM)

The CPM contains features that allow the QUICC to excel in communications and control applications. These features may be divided into three sub-groups:

- Communications Processor (CP)
- Two IDMA Controllers
- Four General-Purpose Timers

The CP provides the communication features of the QUICC. Included are a RISC processor, four SCCs, two SMCs, one SPI, 2.5 Kbytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and fourteen serial DMA channels to support the SCCs, SMCs, and SPI.

The IDMAs provide two channels of general-purpose DMA capability. They offer high- speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC controller may access the IDMA registers directly in the buffer chaining modes. The QUICC IDMAs are similar to, yet enhancements of, the two DMA channels found on the MC68340 and the one IDMA channel found on the MC68302.

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