Telecommunications Applications of Ferroelectric Liquid-Crystal Smart Pixels

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(Invited Paper)

Abstract— **Ferroelectric liquid crystal over silicon smart pixels offers potential advantages over conventional electronic and waveguide approaches to telecommunications switching. The role of such smart-pixel architectures in space/wavelength optical interconnect and in high-performance ATM switches based on interconnection of optically accessed memory is discussed.**

I. Introduction

SMART pixels are the subject of considerable interest for telecommunications switching.[1] The purpose of this paper is to review applications of smart pixels based on ferroelectric liquid crystal (FLC) over silicon technology [2]. The large electrooptic effects in liquid crystals and the integratability of large numbers of modulators [e.g., 320×240^2] with the functionality of silicon VLSI gives rise to a number of useful switching applications. The devices discussed employ free-space optics. We review fiber-to-fiber space [6] and wavelength [7] switches that use FLC as phase modulators. We discuss fiber-to-fiber switches[3] and ATM switch structures [9] with optically accessed silicon memories (opto-RAM) [10] that both use FLC shutters in a matrix–matrix [11], [12] configuration.

The ever-increasing bit rate and the economic pressures on network operators to reduce the number of nodes in national networks leads to increasing node complexity and a potential electronic demultiplexing bottleneck. At the same time, the introduction of the EDFA [13], [14] to both submarine [15] and terrestrial routes[4] increases the potential for WDM techniques and wavelength routing in such networks. A schematic view of a future optoelectronic node is shown in Fig. 1. With the possibility of aggregated switch node throughputs of 1 Tbps being required beyond the turn of the century, it would seem desirable, if not inevitable, that much of the transit node traffic will at least be only partially demultiplexed, if at all.

There is a growing need for fiber matrix switches both in association with electronic switches (such as replacements to current digital crossconnects) and ultimately as space-wavelength routing switches. This is represented by the upper part of Fig. 1. Optical transparency is essential for bit-rate independence, and the switching speeds necessary for network restoration and management, route protection, and maintenance are approachable by FLC over silicon technology. Such devices might become an important part of wavelength-routed networks. The photonics group at Cambridge University is actively involved in research into such switches for both national and local area networks as part of the UK EPSRC POETS (parallel optoelectronic telecommunications systems)[5] and OST (optical switching testbed) projects.[6]

The core switch technology represented by the lower part of Fig. 1 is seen as essentially a silicon electronic system, but optical interconnections will clearly be needed to achieve the necessary aggregate capacity. Switch capacities measured in Tb/ps are currently being postulated. Future deployment of public broadband ATM-based services [16] is likely to place severe demands on all-electronic approaches to switch design. While there have undoubtedly been impressive efforts in the density of gates achievable on silicon, this has never been matched by the performance of the metal-based interconnect between chips, either for multichip modules or backplanes. Since an ATM switching fabric requires a considerably higher degree of interconnectivity than that necessary for circuit switching, electronic interconnectivity is identified as a severe limitation of present approaches to broadband switch design. A

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[1] See, for example, [1] and this issue.

[2] A 320×240 array of modulators on a 14-mm silicon chip is currently being built under DRA Contract MAL 1b/2256. See also [3] (176×176 modulator array) and [4], [5] (256×256 array).

[3] The OCPM project (optically connected parallel machines) is a collaboration between British Aerospace (Sowerby Research Centre), BNR Europe (Nortel), Herriot Watt University, the University of Bath, and Thorn EMI CRL. Work at BNR Europe was subcontracted to the Engineering Department at the University of Cambridge. The project was coordinated by British Aerospace and was funded in part by the DTI and EPSRC. (DTI Reference No. IED2-430-30-004) See also Final Report: OCPM-039 013-ADM-BAe-HW 960 223 and [8].

[4] For example, MCI/Pirelli link between Chicago, IL, and Salt Lake City, UT.

[5] Parallel Optoelectronic Telecommunications Systems (POETS), UK EPSRC GR/J44773. The POETS project involves Cambridge University (coordinator), King's College, London, and University College London.

[6] Optical Switching Testbed UK EPSRC GR/J44728 (Cambridge University Engineering Department and Computer Laboratories).

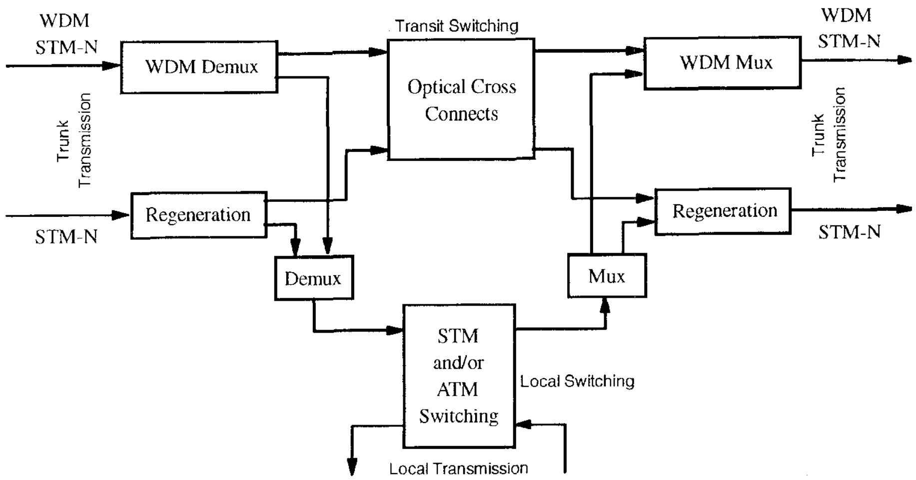


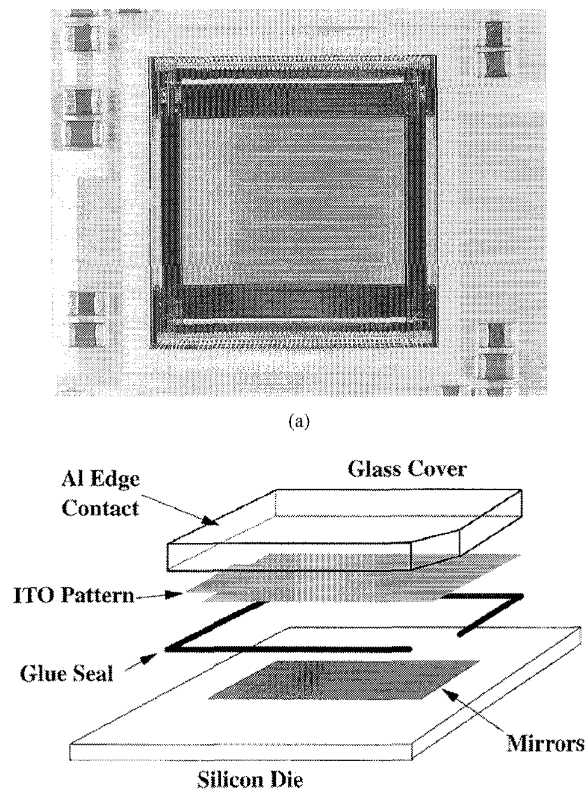
Fig. 1. Schematic of a possible future optoelectronic node.

free-space optically assisted approach to an ATM switch fabric may help by using its inherent spatial bandwidth to increase the connectivity and reduce the limiting effects of buses, low pin-out integrated circuits, printed circuit boards, and multichip modules. Unless overcome, such pin-out limitations can result in suboptimal system partitioning and architectures. Previous important attempts at harnessing free-space optics have been technologically limited to a small switch node functionality as well as low fan-out [17]. Such a limitation has the effect of increasing the number of stages of switching necessary to produce a suitably connected fabric.

In contrast to the many attempts at alleviating interconnection bottlenecks by the selective replacement of electrical connections with on-board optical equivalents [18], we have adopted a fresh approach to the problem in an attempt to understand how a hybrid optoelectronic approach may fundamentally affect the design of an ATM switch fabric from a theoretical performance as well as an interconnection perspective. Clearly, any successful approach must partition the optics and electronics in a befitting manner. Such partitioning has already been described within the context of multiple-quantum-well devices [19]. FLC over silicon opto-RAM [10] allows the incorporation of a degree of optical switching to assist the electronic switching. Some of the available optical parallelism must be used to obtain a high enough chip-to-chip transfer rate due to the modest switching speed currently available from this form of light modulator. However, chip-to-chip transfer rates are ideally matched to the read/write times of silicon VLSI structures, rather than the data rates of the incoming links.

II. FLC over Silicon Smart-Pixel Technology

The addition of a thin layer of ferroelectric liquid crystal to standard CMOS silicon yields an optoelectronic technology that boasts the versatility of VLSI with massively parallel optical input/output [2]. Photodetectors can be implemented within CMOS design rules and the very large electrooptic effects of the liquid crystal enable the implementation of both intensity and π-phase modulators (see Section III). A



(a)

(b)

Fig. 2. FLC on silicon technology.

schematic construction of a smart-pixel device and a photograph of a recently designed 320 × 240 modulator chip are shown in Fig. 2.

The modulator bandwidth is a function of the required electrooptic effect and the permissible driving voltage. A recent optical interconnect project, optically connected parallel machine (OCPM), demonstrated intensity shutters with a reconfiguration time of less than 20 μs at 45 °C using addressing voltages of 10 V [8]. The fastest reconfiguration time for

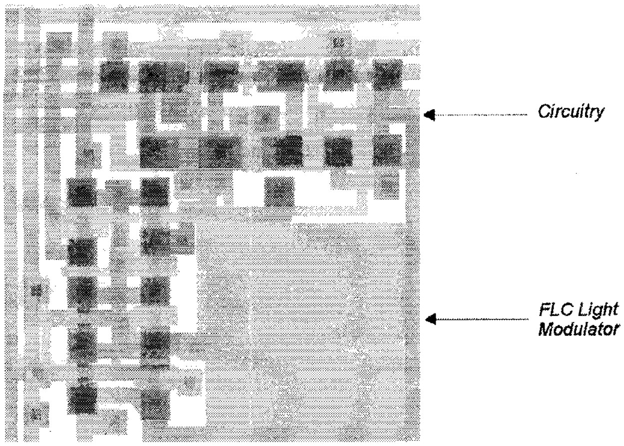


Fig. 3. Opto-RAM cell (single pixel).

intensity modulation suitable for interconnect is extrapolated to be about 1 μs at 80 °C [20]. To achieve efficient phase modulation, a larger switching angle of up to $\pi/2$ radians is required [21]. For fields of 10 Vμm^{-1} or less, this limits the switching times for currently available materials to the order of 400 μs at 45 °C but times below 40 μs have been obtained at 80 °C [22]. Switching down to 200 ns has been observed for much smaller switching angles ($\leq 2°$) in electroclinic liquid crystals [23]. While the implied lack of contrast/loss would probably make electroclinic LC's unsuitable for optical interconnect, they do have promise for signaling modulators in architectures such as the opto-RAM. The driver circuitry can be as simple as a single transistor (DRAM), so that given a small-geometry CMOS process, the limiting smart pixel packing density will be the optical input/output (photodiode/modulator) geometry, even for relatively complex pixel logic. The layout for an experimental optical read opto-RAM memory pixel is shown in Fig. 3.

The pixel shown in Fig. 3 is on a 70-μm pitch with a modulator size of approximately 30 μm. The large dimensions are due to the 2.0-μm CMOS used and to allow a large read beam to simplify alignment in our experimental system. As liquid crystal technology matures and switching voltages decrease, it will be possible to reduce the process geometry. Also, as the optical beam used to illuminate the modulator becomes closer to being diffraction limited, then the modulator will be of order 5 μm. Previous work has focused two beams into a 6-μm$\times$ 20-μm area [24], although with ferroelectric liquid crystals only one beam is required. This is because the transmission of a reference beam is not required due to a high contrast ratio alleviating any problems associated with variations in receiver threshold over the area of a die. Therefore, feasible pixel pitches will be of order 15 μm with the die size approaching 20 mm. (Crosstalk considerations suggest a limiting pixel pitch of about 8 μm [11]). This will allow for at least 10^6 pixels per single chip.

III. Liquid-Crystal Modulation Schemes

Ferroelectric liquid crystal modulators can be configured as either phase or intensity modulators and drive schemes

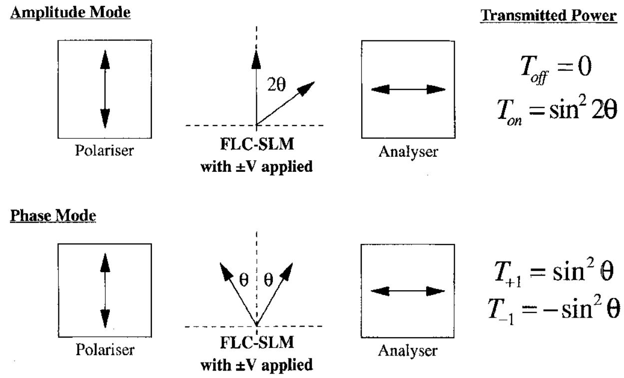


Fig. 4. Modulation schemes for FLC smart pixels.

can be chosen for continuous or synchronized read-out [25]. The choice of modulation and drive scheme have important consequences for smart-pixel system design. The thin layer of (surface stabilized) ferroelectric liquid crystal can be optically modeled as a rotatable waveplate with fast and slow axes in the plane of the modulator, i.e., perpendicular to the direction of light propagation. The alignment layers are usually chosen so that the crystal will lie in one of two bistable states such that there is an angle of 2θ between the fast axes of the two states where θ is known as the tilt angle of the crystal. Application of an electric field is required to switch from one state to the other and the field must be reversed to switch back. The ferroelectricity (spontaneous polarization) of the LC implies that charge needs to be transferred to and from the crystal—too little charge will result in incomplete switching. To ensure long lifetime of the crystal, charge balancing should also be maintained. Interconnect applications demand a drive scheme which permits continuous viewing. The preferred scheme for the smart-pixel architectures uses an alternating front electrode (ITO on glass) voltage. Thus, depending on the phase of the silicon pad voltage, an FLC field is produced which, in one half cycle, switches pixels needing to change from state 1 to state 2 and, in the next half cycle, those changing from state 2 to state 1, otherwise leaving a net zero voltage across the crystal so that pixels not needing to change are left unaltered.

The schemes for intensity and phase modulation are depicted in Fig. 4. A fuller description may be obtained from Jones' matrix analysis [26], but a more qualitative description is adopted here.

Perhaps the key difference between intensity and phase modulation, which has only been fully elucidated relatively recently [27] is that, to obtain high contrast, intensity modulation is polarization sensitive, requiring crossed polarizers at the input and output, and therefore, polarization control of the source. However, when phase modulators are used to form a (binary) phase grating or hologram, the relative modulation between pixels in alternate states is always π radians irrespective of the input polarization. Thus, in the output plane, there will be a central (zero-order spot) whose intensity will vary as $\sin^2(2\theta)$

$$I(\text{zero order}) = I_o\left[1 - \sin^2(2\theta)\sin^2\frac{\delta}{2}\right] \qquad (1)$$

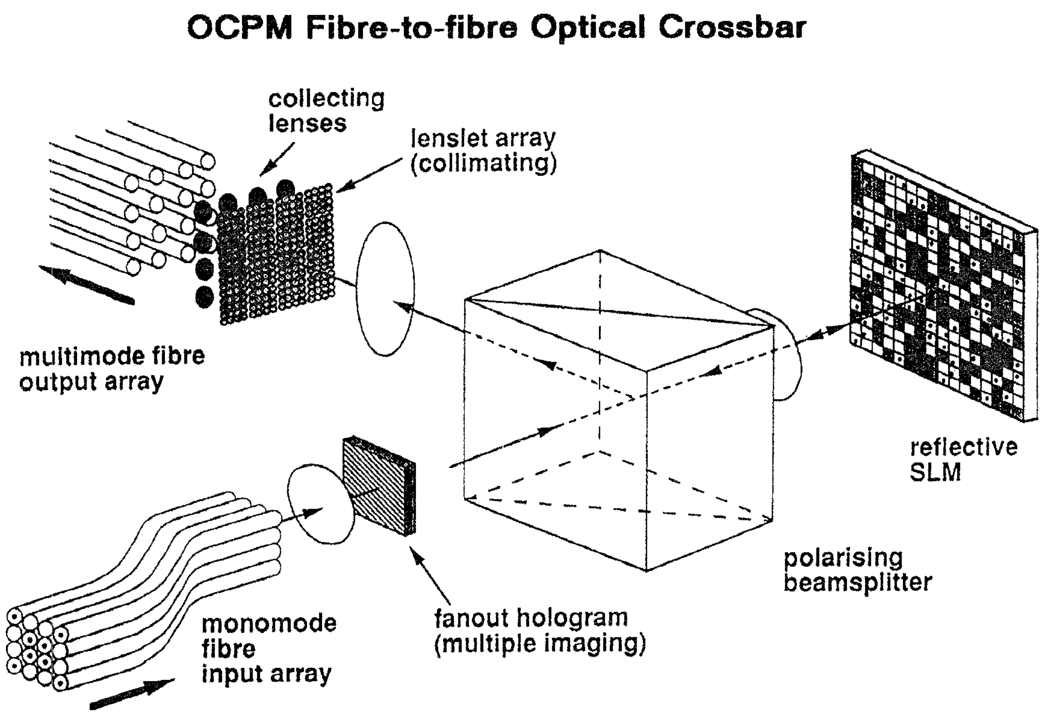


Fig. 5. The matrix–matrix intensity crossbar.

where I_o is the incident intensity and δ is the optical path difference between the fast and slow axes expressed in radians) and the intensity of the diffracted spots will be independent of the input polarization. It is this unique feature which enables the design and implementation of optically transparent beam-steering switches for telecommunications systems. Furthermore, the attainment of binary phase is wavelength independent, being essentially a symmetry property. Thus, the phase holograms can be expected to be broadband, the only limitation being the unavoidable shifts in spot position from the wavelength dependence of diffraction.

IV. Space-Switch Architectures

A. Matrix–Matrix Intensity Switches

The majority of implementations of optical switches using FLC have been of the full crossbar architecture, since the use of free-space optics permits high fan-out and fan-in. The OCPM demonstrator, for example, uses an input array of 64 single-mode high-birefringence fibers and an output array of 64 multimode fibers. The interconnect is based on the matrix–matrix principle [11], [12] with holographic fan-out and fan-in. The matrix–matrix crossbar makes more efficient use of the numerical aperture than, for example, the vector-matrix multiplier [28]. As it performs a full crossbar function it allows both broadcast and multicast. A schematic of the matrix–matrix crossbar is shown in Fig. 5. The critical performance parameters are the loss (and scaleability), isolation/crosstalk, and the ease of implementation of the routing algorithm.

1) Loss: Fan-out losses of $1/N$ are unavoidable through the replication of the inputs to achieve the full crossbar function. Holographic replication can be achieved with low excess loss ($\sim$1 dB) [29] at the expense of making the switch relatively narrow-band ($\sim \pm 1$ nm). For the matrix–matrix crossbar, the fan-in losses are reduced by the use of multimode fiber but would scale as $1/N$ if single-mode output were required. A single-mode fiber-to-multimode fiber loss of 28 dB was achieved in the first prototype 64×64 switch against an intrinsic fan-out loss of 18 dB.

2) Isolation: The isolation that can be achieved is directly related to the intensity contrast of the individual FLC pixels. There is usually a single pixel acting as each crosspoint. A single port isolation of 16.6 dB was measured in the OCPM demonstrator, which was dominated by the poor 40:1 contrast ratio of the SLM. With better quality mirrors, it is reasonable to expect a contrast of 25–30 dB to be achievable with FLC over silicon devices.

3) Control and Arbitration: The use of a single-stage crossbar architecture with intensity pixels acting as single crosspoints permits the trivial routing algorithm: open the requisite pixel to make the connection. Likewise, arbitration requires that only one pixel in a block associated with each output is open at one time.

For applications where polarization control of the source fibers is permitted and where multimode fibers can be used, the single-stage matrix–matrix crossbar remains attractive for moderate switch sizes. The OCPM 64×64 demonstrator was tested at 270 Mb/ps at 10^{-12} BER using 3 mW in fiber laser power at 800 nm. An existing optical design suggests a 33-dB power budget at 2.5 Gb/ps with a +3 dBm source and −33-

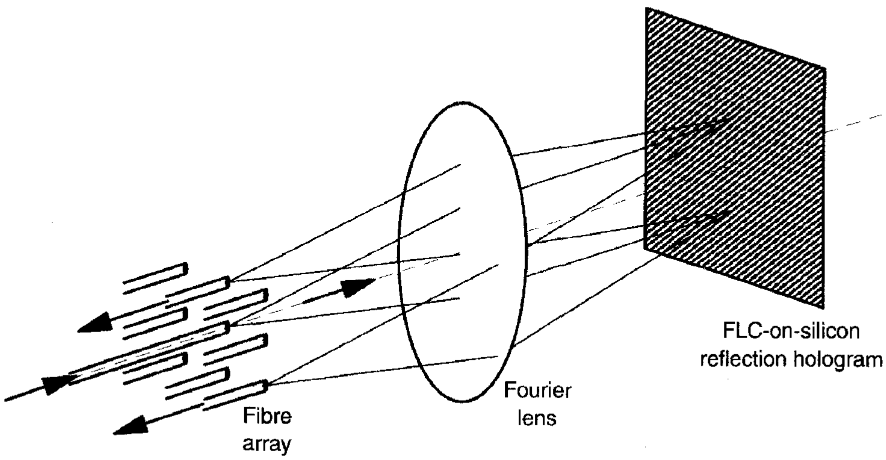


Fig. 6. Schematic of one possible implementation of a holographic crossbar.

dBm receiver with an excess loss of 7.5 dB over the intrinsic fan-out losses. Subject to the acceptable contrast, these figures would support a 144 × 144 crossbar at 10^{-12} BER.

B. Holographic Beam-Steering Switches

Since the first proposal for FLC on silicon modulators to be used as (binary) phase holograms for optical interconnect [30], [31], there has been much debate over their best configuration for switching. The architectures and implementation differ from the polarization-dependent, intensity-based matrix–matrix crossbar in a number of important respects. First, the use of groups of phase pixels associated with each input permits beam-steering architectures. Although a single-stage crossbar can be implemented, it is more power- and crosstalk-efficient to use a two-stage architecture such as the deflector-selector [32]. The fan-out of a single stage is determined by the space-bandwidth product (number of pixels) and the physical dimensions of the output fiber array. Clearly, if the fan-out does prove a limitation for very large switches, then banyan, Clos, or other architectures might be employed, with a concomitant increase in the complexity of control and arbitration. However, single-stage dynamic fan-out of 1:64 or 1:128 appears technologically feasible—routing on array sizes of this dimension has been demonstrated in the laboratory, but not yet to single-mode fiber arrays. A schematic of one mode of interconnection for a $1:N$ switch using a FLC silicon backplane is shown in Fig. 6.

1) Loss: The loss of a single $1:N$ or $N:1$ stage is predominantly a function of the efficiency of the beam-steering FLC phase hologram. Binary phase holograms, because of the output plane symmetry, incur a loss to a single spot of about 4 dB. This may not be so severe if it is remembered that the symmetric spot might be usefully employed to provide redundancy.

Free-space single-mode to single-mode fiber losses of 2–3 dB have been observed in simple laboratory switch rigs. The other potential source of loss is the use of nonoptimal FLC switching angle and thickness. While this has hampered experimental demonstrations to date (typically incurring a 6 dB penalty), new FLC materials such as low molar mass siloxanes [22] have been shown in the laboratory to obviate this penalty.

2) Isolation: Unlike the matrix–matrix crossbar, the isolation of the holographic beam-steering switch is not so critically dependent on the liquid crystal alignment, since binary-phase operation is assured. Rather, it is dependent on the number of pixels associated with the beam-steering hologram and residual scattering losses. A crude estimate for the single-port isolation is [33] is

$$\text{Isolation} \sim 10 \log_{10} \left[\frac{m\eta}{2(1-\eta)}\right] \text{dB} \qquad (2)$$

where m is the number of pixels in the routing hologram and η is the hologram efficiency. Equation (2) assumes that power is distributed evenly over the output plane away from the desired spot. Various solutions can be theoretically determined which dramatically reduce the power at other fiber positions than the desired output [34], [35]. However, experimentally determined isolation to date has yielded figures more closely in agreement with (2) (typically 25–35 dB). For example, the fiber switch reported in [27] has a fiber-to-fiber loss of 13 dB and an isolation of 35 dB for a 64 × 64 routing hologram. Of course, in the deflector-selector architecture, the single-stage isolation will be squared (per input port), i.e., 50–70 dB. Such figures are compatible with the stringent requirements on crosstalk for optically transparent [36] and particularly for wavelength-routed systems [35].

3) Control and Arbitration: For a $N \times N$ switch (or each $1:N$ or $N:1$ switch), N different routing holograms will be required. These are of course determined during the switch fabrication. Irregularities in the fiber array can be built into the hologram design, and the precise holograms can be optimized *in situ* [37]. As an example, the 1:16 experimental fiber switch shown in Fig. 7 used a series of search holograms to determine the core positions of the fibers in the array and hence the optimum hologram set. It is envisaged that further monitoring and optimization should be possible during the lifetime of the switch. It should be possible to extend the FLC over silicon smart-pixel technology to incorporate the (digital) hologram patterns in on-chip memory (a 1:64 module would

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