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[11]

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Sonohara et al.

[54] INVERSE MODIFIED DISCRETE COSINE TRANSFORM SIGNAL TRANSFORMING SYSTEM

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Related U.S. Application Data

[60] Continuation of Ser. No. 458,338, Jun. 2, 1995, abandoned, which is a division of Ser. No. 119,003, Sep. 9, 1993, abandoned.

[30] Foreign Application Priority Data

- Sep. 28, 1992 [JP] Japan 4-282440
- [51] Int. Cl.⁶ H04B 14/00

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[45] Date of Patent: Jul. 8, 1997

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[57] ABSTRACT

An MDCT calculating circuit includes an x₀₁ calculating circuit for multiplying input signals with a forward transforming window and a linear forward transforming unit for linear forward transforming an output signal of the calculating circuit. The linear forward transforming unit includes an x_{02} calculating circuit and an x_{03} calculating circuit for pre-processing the output signal of the x₀₁ calculating circuit and an integration and summation processing circuit for executing integration and summation processing operations on an output signal of the pre-processing unit. The integration and summation processing circuit executes an integration and summation operation on an N/2 number of input signals from the pre-processing unit by grouping a k number of input signals as a processing unit and iteratively executes the integration and summation processing operations a N/(2*K) number of times for outputting a sum total of N/2 number of signals.

16 Claims, 7 Drawing Sheets





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FIG.4

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