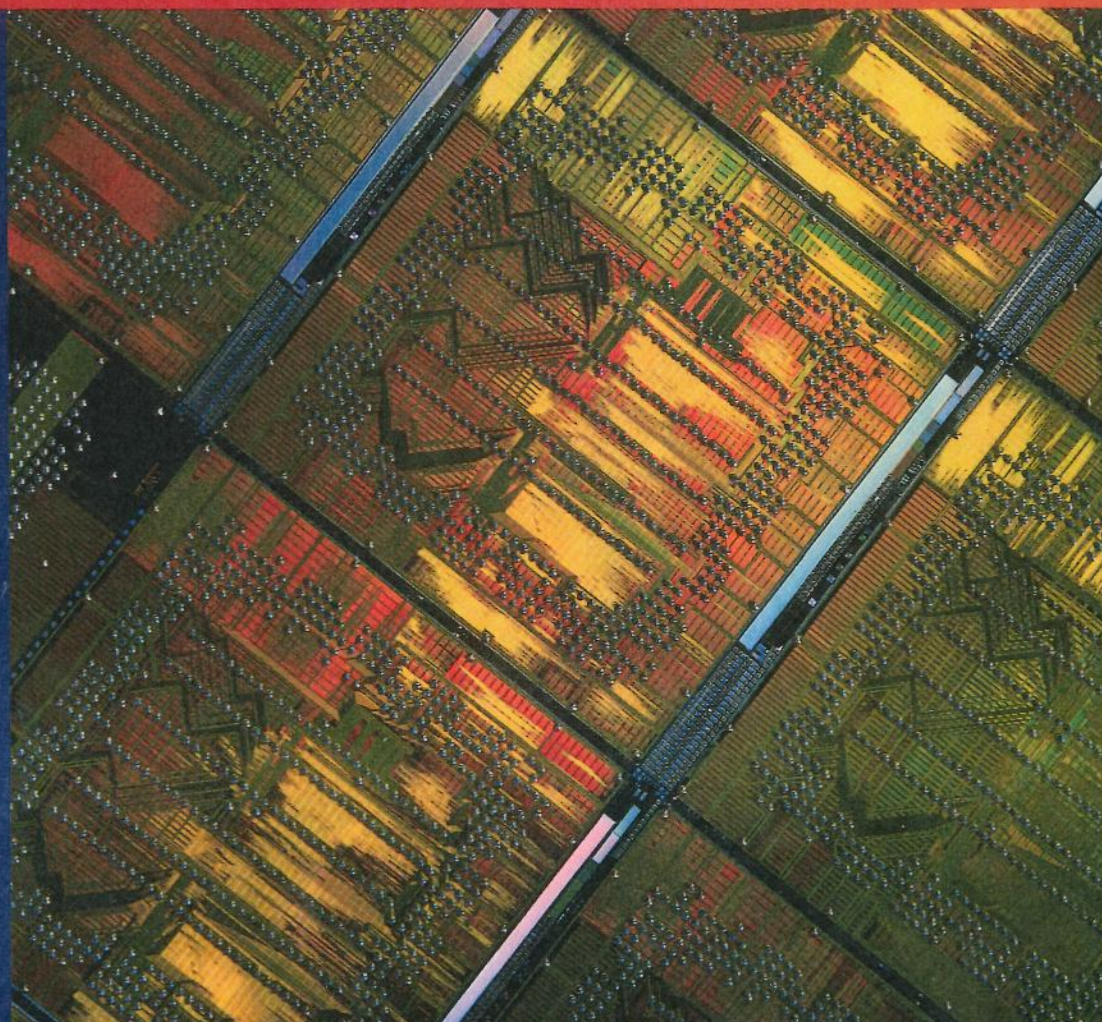
Fourth Edition

SOLID STATE ELECTRONIC DEVICES



Ben G. Streetman

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FOURTH EDITION

Solid State Electronic Devices

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lem for bipolar circuits. We mentioned in Section 8.3.6 that using a field oxide about ten times as thick as the gate oxide increases V_T in these areas. We cannot make the field oxide arbitrarily thick, however, because of practical problems of deposition and the fact that metallization patterns must be deposited over the "hills and valleys" of the resulting surface. A further increase in the field threshold voltage can be obtained by doping the region between transistors with the impurity type of the substrate (Fig. 9-13). For example, a masking and implant or diffusion step can be used to dope the field region prior to forming the source and drain regions. Such doping increases V_T in the field by increasing Q_d (see Fig. 8-17). Combined with a small value of C_i due to the thick field oxide, the Q_d/C_i term can lead to very high threshold voltage between devices. The disadvantage of channel stop doping is that the breakdown voltage of the source and drain junctions is reduced by the more heavily doped channel stop. Therefore, it is necessary to control the field doping carefully to increase V_T appropriately without significant lowering of the junction breakdown voltage. This close control of doping makes ion implantation particularly attractive for this application.

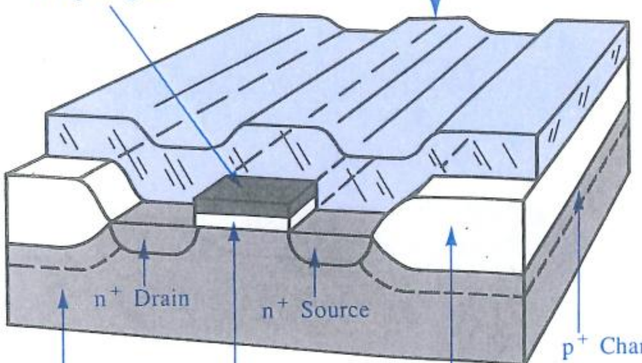

Figure 9-13 The use of thick field oxide and channel stops to prevent inadvertent channel formation outside the active region of the MOS transistor. Shown also is a chemical-vapor deposited SiO_2 glass layer that will be patterned prior to metallization. This glass overlayer is often doped with phosphorus and boron and heated to the softening point to flatten out the surface before patterning for metallization (a process called *reflow* glass).

LDD and Sidewall Spacers. The use of the lightly doped drain (LDD) structure was described in Section 8.3.9 as a way of reducing the high field in the drain junction of small-geometry devices. Figure 9-14 illustrates the formation of an LDD transistor for application in integrated circuits. An important aspect of LDD fabrication is the use of *sidewall spacers* on each side of the gate. After formation of the thin gate oxide and polysilicon gate, an n-type implant forms the shallow, lightly doped source and drain regions (a). Then a thick oxide layer is deposited by a low-temperature chemical-vapor-deposition pro-

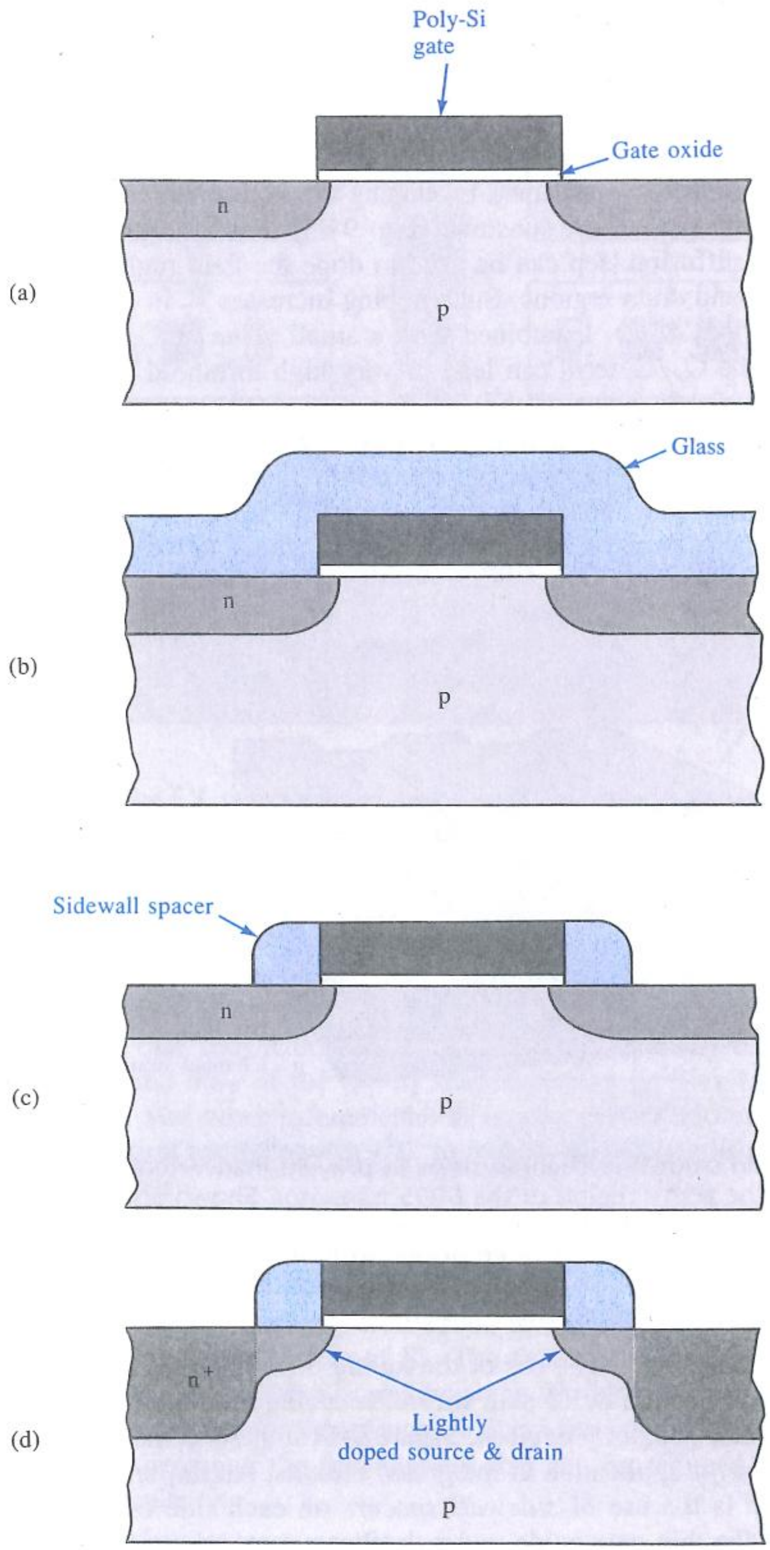

Figure 9-14 Fabrication of the lightly doped drain structure, using sidewall spacers. The polysilicon gate covers the thin gate oxide and masks the first low-dose implant (a). A thick oxide layer is deposited by low temperature CVD (b) and is anisotropically etched away to leave only the sidewall spacers (c). These spacers serve as a mask for the second, high-dose implant. After a drive-in diffusion, the LDD structure results (d).

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