

(12) **United States Patent**  
**Nakagawa**

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(54) **NONVOLATILE SEMICONDUCTOR MEMORY AND PROCESS FOR FABRICATING THE SAME**

6,064,592 A \* 5/2000 Nakagawa et al. .... 365/185.05

FOREIGN PATENT DOCUMENTS

(75) Inventor: **Ken-ichiro Nakagawa**, Tokyo (JP)

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(73) Assignee: **NEC Corporation**, Tokyo (JP)

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(\* ) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

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\* cited by examiner

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

*Primary Examiner*—Tom Thomas

*Assistant Examiner*—Thien F Tran

(74) *Attorney, Agent, or Firm*—Young & Thompson

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Nov. 26, 1998 (JP) ..... 10-335171

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 29/76**

(52) **U.S. Cl.** ..... **257/314; 257/315; 257/316; 257/317**

(58) **Field of Search** ..... **257/314-317**

(56) **References Cited**

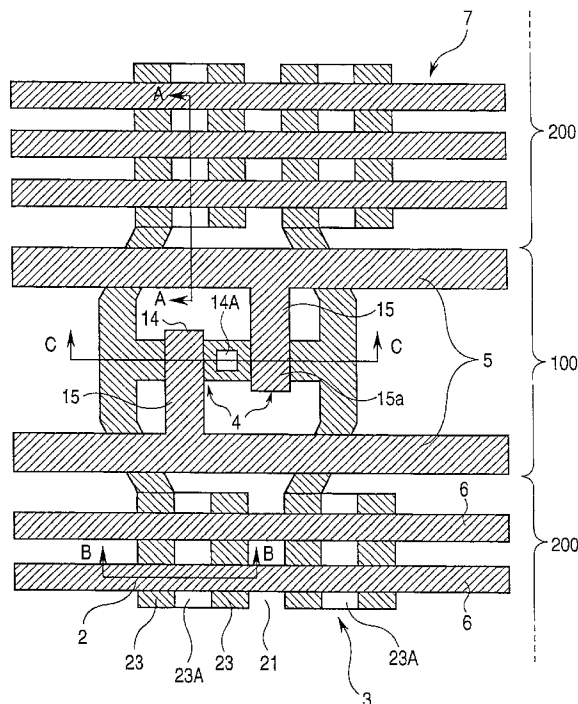
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(57) **ABSTRACT**

A nonvolatile semiconductor memory comprises a memory cell region including a number of memory cells formed therein and each having a floating gate and a control gate formed above the floating gate, a plurality of word lines extending in a first direction in parallel to each other, separately from each other, and a selection transistor region positioned adjacent to the memory cell region and including one selection transistor formed therein and a selection signal line extending in parallel to the word lines. The selection signal line is formed on an inactive region in a substrate to extend in parallel to a boundary line between the memory cell region and the selection transistor region.

**14 Claims, 9 Drawing Sheets**



**EXHIBIT**  
**Macronix**  
**MX027-1006**

Fig. 1 Prior Art

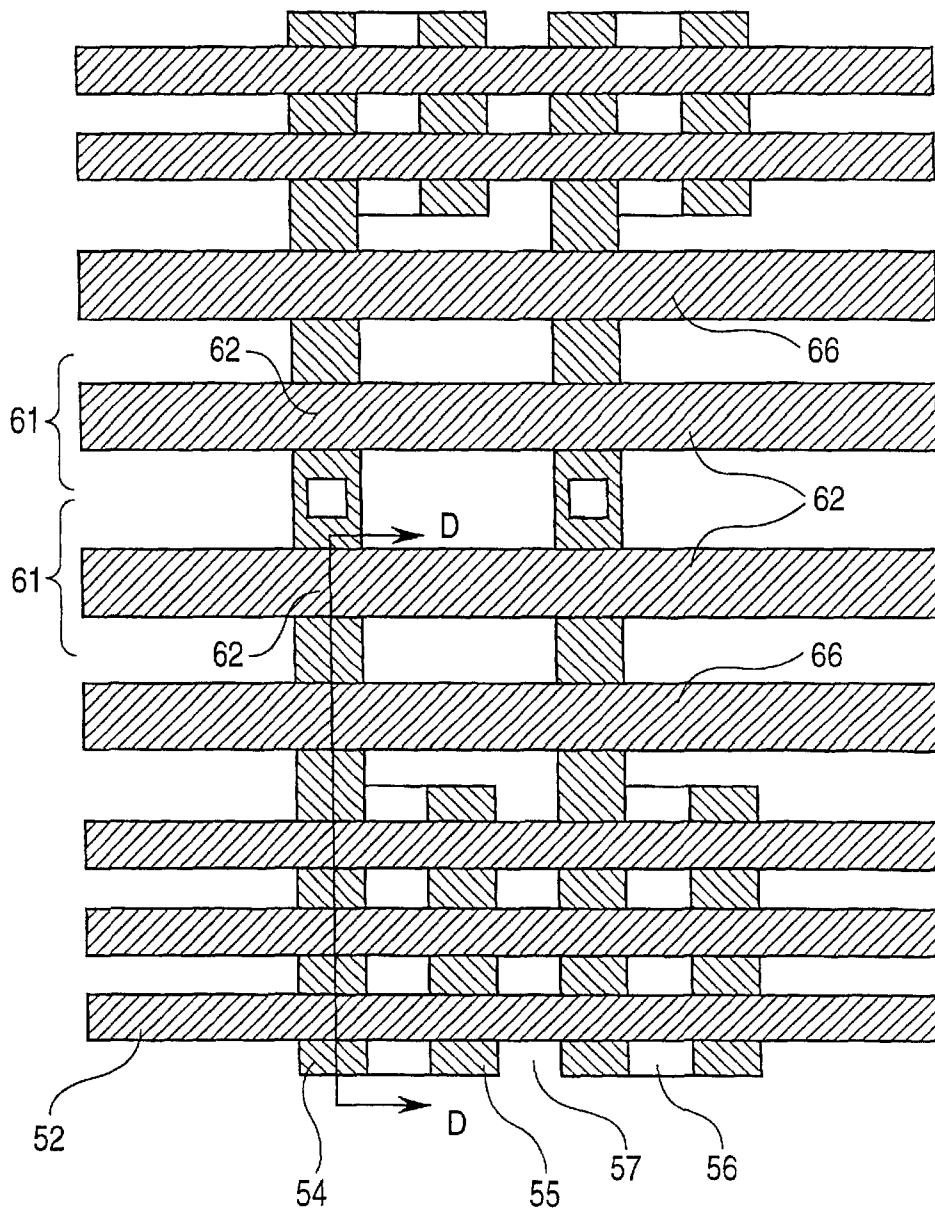


Fig. 2 Prior Art

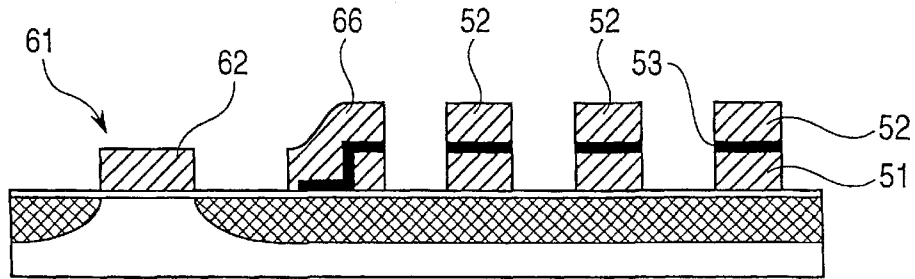


Fig. 3A Prior Art

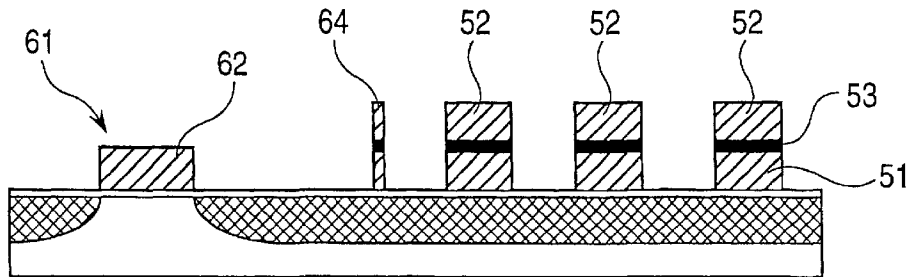


Fig. 3B Prior Art

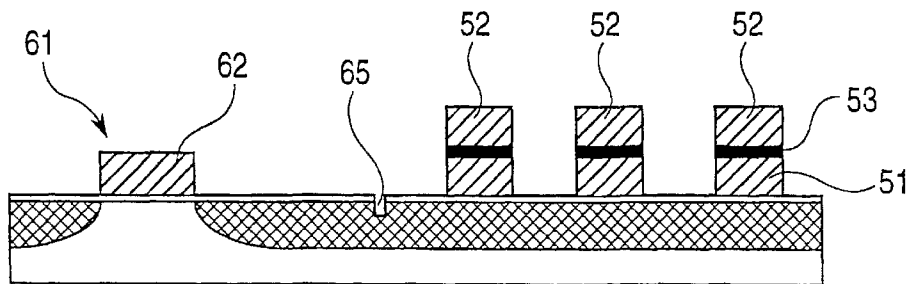


Fig. 4

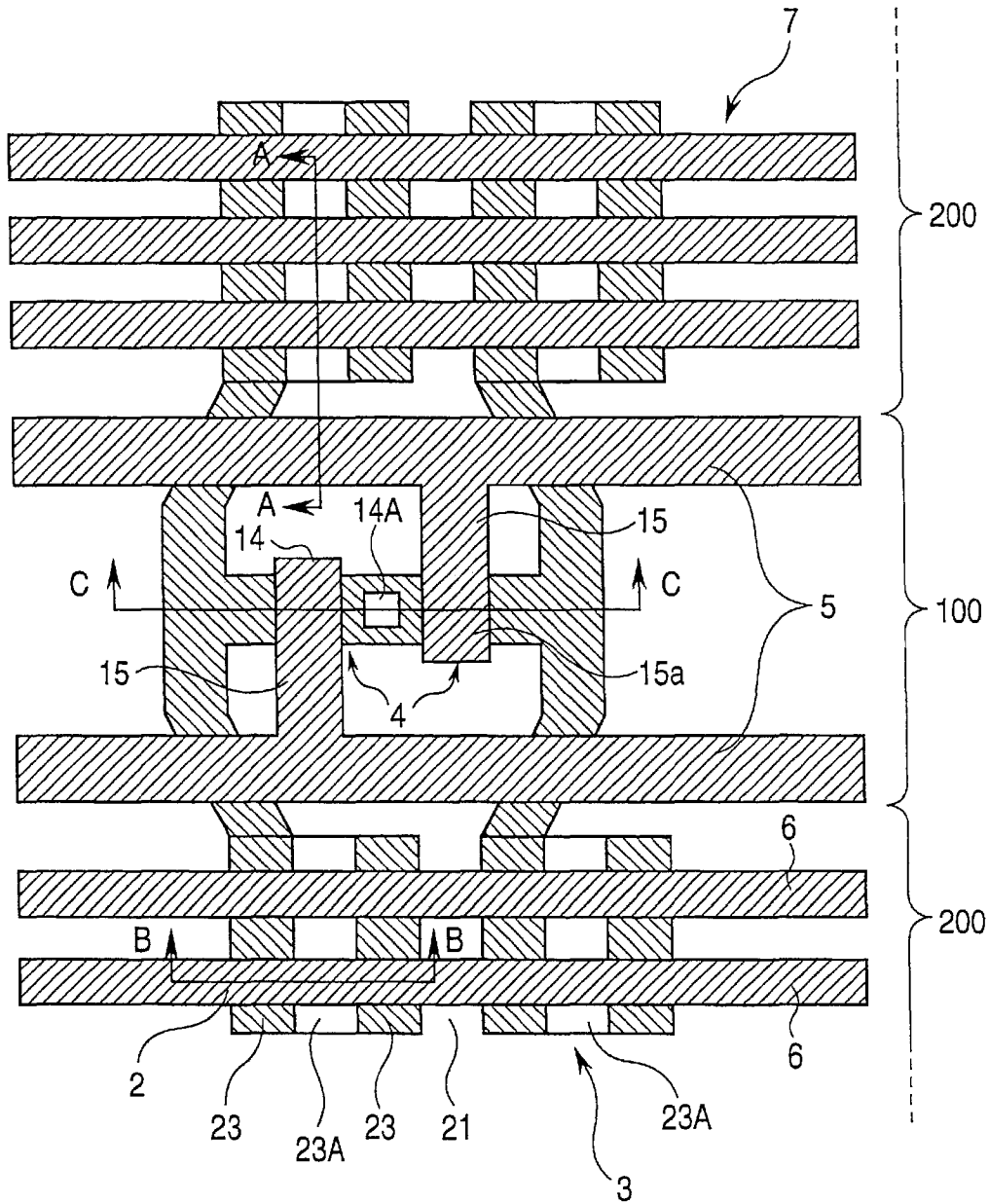


Fig. 5A

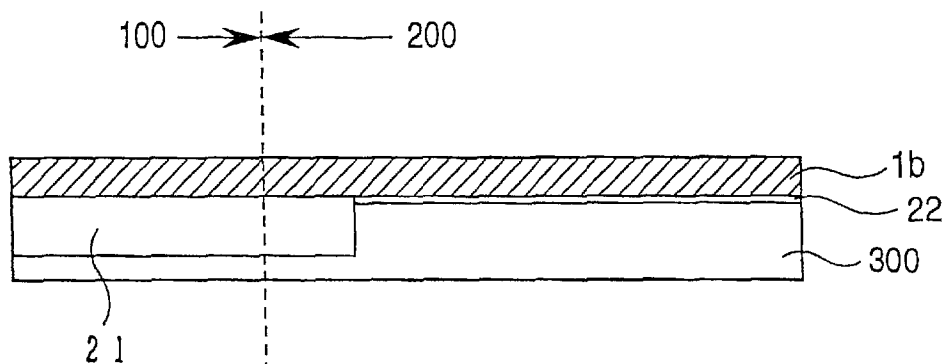


Fig. 5B

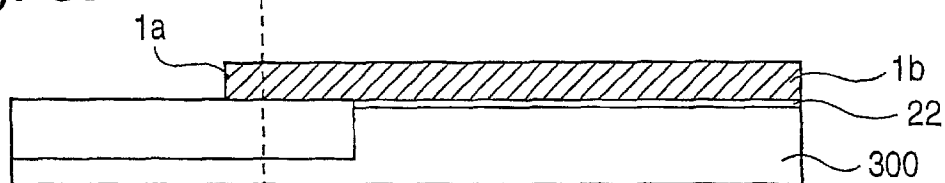


Fig. 5C

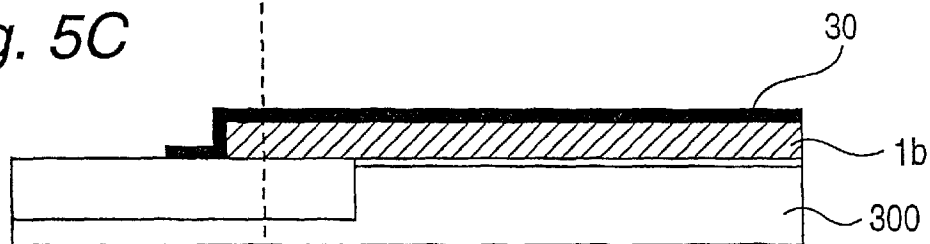
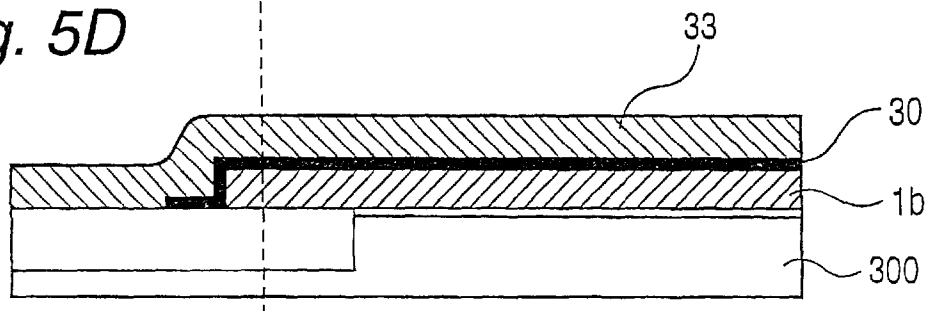


Fig. 5D



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