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Paper 16
Entered: May 8, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MACRONIX INTERNATIONAL CO., LTD.,
MACRONIX ASIA LIMITED, MACRONIX (HONG KONG) CO., LTD.,
and MACRONIX AMERICA, INC.
Petitioner

v.

SPANSION LLC
Patent Owner

Case IPR2014-00108
Patent 7,151,027 B1

Before DEBRA K. STEPHENS, JUSTIN T. ARBES, and
RICHARD E. RICE, *Administrative Patent Judges.*

RICE, *Administrative Patent Judge.*

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

Macronix International Co., Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. (collectively "Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1-14 of U.S. Patent No. 7,151,027 B1 (Ex. 1001, "the '027 patent") pursuant to 35 U.S.C. §§ 311-319. Pet. 3. Patent Owner Spansion LLC ("Patent Owner") filed a Preliminary Response (Paper 14, "Prelim. Resp.") to the Petition. We have jurisdiction under 35 U.S.C. § 314. For the reasons that follow, the Board has determined to institute an *inter partes* review.

I. BACKGROUND

The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a):

> THRESHOLD—The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Petitioner challenges claims 1-14 as unpatentable under 35 U.S.C. §§ 102(b) and 103(a). Pet. 3-4. We grant the Petition as to claims 1-6 and 8-13 on certain grounds, but not as to claims 7 and 14, as discussed below.

A. Related Proceedings

Petitioner discloses that the '027 patent is asserted in: (1) *Spansion LLC v. Macronix International Co., Ltd.*, Civ. No. 3:13-cv-03566 (N.D. Cal.); and (2) *In re Flash Memory Chips and Products Containing Same*, Inv. No. 337-TA-893 (U.S. Int'l Trade Comm'n). Pet. 1.

B. The '027 Patent (Ex. 1001)

The '027 patent, titled "Method and Device for Reducing Interface Area of a Memory Device," issued on December 19, 2006. According to the '027 patent, the operational and peripheral components of a memory device conventionally are fabricated using separate processes, resulting in "steps" between structures in the interface area. Ex. 1001, 1:24-40; fig. 1. Further, "stringer spacers," i.e., small components that easily are peeled or removed from the memory device, are formed in the interface area at the steps. *Id.* at 1:45-48; fig. 1. Conventionally, the risk of damage to the memory device from stringer spacer debris is eliminated by fabricating a salicide block (layer) over the interface area. *Id.* at 1:54-57; fig. 1.

The '027 patent, by smoothing out any steps caused by etching in the interface area, addresses the problem of stringer spacers and eliminates the need for a salicide layer. *Id.* at 2:57-3:2. In one embodiment, a polysilicon interface structure, the height of which is easy to control, is used to smooth out any such steps. *Id.* at 2:59-65.

Figures 3A-3G of the '027 patent illustrate steps in a process for forming interface structure 360. *Id.* at 3:18-22.

At the step illustrated in Figure 3D of the '027 patent, which is reproduced below, "second polysilicon layer (poly-2) 320" is deposited above dialectric material 315 and substrate 300. *Id.* at 4:22-24.

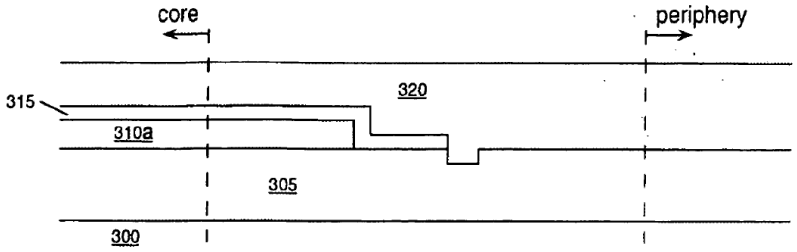

Figure 3D

A vertical dashed line on the left of Figure 3D denotes the approximate border between a memory array ("core") and the interface area, and a vertical dashed line on the right of the figure denotes the approximate border between the interface area and the periphery. *Id.* at 3:54-57. As depicted in Figure 3D, first polysilicon layer 310a, referred to as "gate polysilicon ('poly-1') 310a" in the '027 patent, is disposed beneath dielectric material 315. *Id.* at 3:50-53. Figure 3D also depicts isolation area 305. *Id.* at 3:51-52.

Figure 3E of the '027 patent, which is reproduced below, depicts the step of etching a portion of poly-1 layer 310a, dielectric material layer 315, and poly-2 layer 320, proximate to the memory array. *Id.* at 4:27-30.

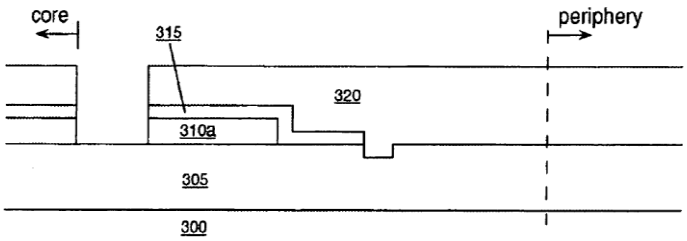

Figure 3E

The '027 patent discloses that "a known process (such as a stacked gate etch)" is used for the etching step in Figure 3E. *Id.*

Figure 3F of the '027 patent, which is reproduced below, depicts the step of etching a portion of poly-2 layer 320 proximate to the periphery. *Id.* at 4:38-40. As described in the '027 patent, "a known process (such as a second gate etch)" is used for the etching step depicted in Figure 3F. *Id.* The etching step is used to form interface structure 360, which is illustrated in Figure 3F. *Id.* at 4:41.

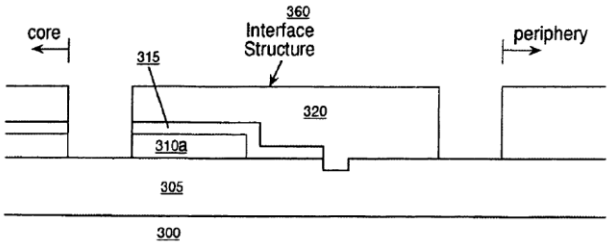

Figure 3F

As depicted in Figure 3F and described in the '027 patent, "interface structure 360 is the same height as the memory array proximate to the memory array and the same height as the periphery proximate to the periphery, such that step size is smoothed out reducing the occurrence of stringers from spacer etching." *Id.* at 4:49-54.

C. Illustrative Claims

Claims 1 and 8 are independent. Claims 2-7 depend directly or indirectly from claim 1, and claims 9-14 depend, directly or indirectly, from claim 8. Claims 8 and 14, which are reproduced below, are illustrative:

> 8. A method for fabricating a memory device, said method comprising:
>
> forming a poly-1 layer above a substrate at an interface between a memory array and a periphery of said memory device;
>
> forming a poly-2 layer above said poly-1 layer at said interface;

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