UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MACRONIX INTERNATIONAL CO., LTD., MACRONIX ASIA LIMITED, MACRONIX (HONG KONG) CO., LTD., and MACRONIX AMERICA, INC.
Petitioners

v.

SPANSION LLC
Patent Owner

Case: IPR2014-00108

CORRECTED DECLARATION OF DHAVAL J. BRAHMBHATT

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Patent Trial and Appeal Board
United States Patent and Trademark Office
PO Box 1450
Alexandria, Virginia 22313–1450
Submitted Electronically via the Patent Review Processing System

EXHIBIT
Macronix
Corrected
MX0027-1002

I, Dhaval J. Brahmbhatt, hereby declare as follows:

I. Introduction and Qualifications

1. I am the founder and am currently the president and CEO of PHYchip Corporation ("PHYchip"). Among other things, PHYchip provides expert services in the design of high-speed analog and mixed-signal integrated circuit ("IC"), a variety of memory devices, with a particular focus on non-volatile memory devices such as Flash memory modules.

2. I have prepared this Declaration on behalf of Macronix International Co., Ltd., Macronix Asia Limited, Macronix (Hong Kong) Co., Ltd., and Macronix America, Inc. (collectively, "Macronix") in connection with a petition for Inter Partes Review of U.S. Patent No. 7,151,027 ("the '027 Patent") (MX027-1001).

3. I have summarized in this section relevant aspects of my educational background and career history. My full resume is attached as Appendix A to this Declaration.

Educational Background

4. In 1977, I received a Master of Science Degree in Physics with a specialization in Solid State Electronics from Gujarat University in India. In 1978, I received a second Master of Science Degree, this one in Electrical Engineering, from the University of Cincinnati in Ohio. I also hold certificates in

management trainings from Stanford University Graduate School of Business, a certificate in marketing from University of London in Ontario, Canada and a certificate in nanotechnology from the California Institute of Nanotechnology.

Career History

5. I have over 30 years of substantive experience in the field of IC memory device design and manufacture. I began my career in 1978 at a Fairchild Semiconductor, working on the design and development of Erasable Programmable Read-Only Memory ("EPROM") products. I later worked on the design and production of single power supply Electronically Erasable Programmable Read-Only Memory ("EEPROM") products for Synertek, which was a subsidiary of Honeywell International, Inc., and then I worked for National Semiconductor as a design manager for high density EEPROM memory devices.

6. In 1996, I was named Vice President of Technology and Business Development for the Smart Modular Corporation. In that position, I oversaw the design, development, and marketing of advanced IC memory-based modules such as Flash memory cards for portable devices produced by major multinational technology companies.

7. I later consulted in the Flash memory card industry and served as a "C" level officer in several start-up companies that developed IC devices prior to founding PHYchip Corporation in 2002.

8. I am the sole inventor on ten patents and the lead inventor on all eleven patents listed under my name at the USPTO. Most of these patents relate to EPROM, EEPROM, and/or Flash memory IC design, memory cell design, memory array architecture, etc.

II. Scope of Assignment

9. I have been asked to provide my opinion on the validity of the ’027 Patent. In particular, I have been asked to consider whether the inventions recited in claims 1-14 of the ’027 Patent are unpatentable over certain published prior art references. This Declaration sets forth my opinion on this topic.

10. In my analysis, I considered the ’027 Patent and its file history, as well as the prior art references and related documentation discussed below. I have considered these documents in light of the general knowledge in the art at the time of the alleged inventions. In formulating my opinion, I have relied upon my experience, education, and knowledge in the relevant art. I have also helped prepare and reviewed in detail the claim charts that are to be included with the petition for Inter Partes Review of the ’027 Patent, to which this Declaration relates.

11. Additional information may become available which would further support or modify the conclusions that I have reached to date. Accordingly, I reserve the right to modify and/or enlarge this opinion or the bases thereof upon

consideration of any further discovery, testimony, or other evidence, or based upon the interpretations of or conclusions about any claim term by the Patent Office different than those proposed in this declaration.

III. The ’027 Patent

12. It appears from the face of the ’027 Patent that it issued from U.S. patent application number 10/859,369, which was filed on June 1, 2004. It does not appear the patent claims an earlier filing date.

13. The ’027 Patent generally relates to a method for manufacturing a semiconductor memory device. More particularly, the ’027 Patent is intended to reduce the interface area of a memory device, by forming an interface structure in the area between the memory core and the periphery.

14. The ’027 Patent discloses an embodiment of the steps required to form this interface structure in Figures 3A through 3G, along with the accompanying text. In the following discussion, each of Figures 3A through 3G have been annotated to help distinguish the various layers.

15. First, as shown in Figure 3A, a first layer of polysilicon, or “poly-1,” (green) is formed over an isolation area (light blue) over a silicon substrate (darker blue). *See* MX027-1001 at 3:50-67.

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