INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2003 EDITION

LITHOGRAPHY

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LITHOGRAPHY

SCOPE

In 2003 and beyond, lithographers are confronted with two sets of challenges. The first is a consequence of the difficulties inherent in extending optical methods of patterning to physical limits, while the second follows from the need to develop entirely new, post-optical lithographic technologies capable of being implemented into manufacturing. Not only is it necessary to invent technical solutions to very challenging problems, it is critical that die costs not be increased because of the new methods. Each new generation of lithographic technology requires advances in all of the key elements of the following lithography infrastructure:

- Exposure equipment
- Resist materials and processing equipment
- Mask making, mask making equipment, and materials
- Metrology equipment for critical dimension (CD) measurement, overlay control, and defect inspection

This chapter provides a 15-year roadmap defining lithography's difficult challenges, technology requirements, and potential solutions. Additionally, this chapter defines the Lithography International Technology Working Group (ITWG) interactions with and dependencies on the crosscut TWGs for Environment, Safety, and Health (ESH); Yield Enhancement; Metrology; and Modeling and Simulation.

Since the earliest days of the microelectronics industry, optical lithography has been the mainstream technology for volume manufacturing, and it is expected to continue as such through the 45 nm node, through the application of resolution enhancement techniques such as off-axis illumination (OAI), phase shifting masks (PSM), optical proximity corrections (OPC), and possibly liquid immersion. In addition to resolution enhancement techniques, lenses with increasing numerical apertures and decreasing aberrations will be required to extend the life of optical lithography, and liquid immersion is also being considered as a means of extending optical lithography. It should be noted that it becomes much more difficult to implement OPC and resolution enhancement at the 65 nm node and beyond, compared to preceding nodes.

The requirements of the 32 nm node and beyond are viewed as beyond the capabilities of optical lithography. Extension of the Roadmap will require the development of next-generation lithography (NGL) technologies, such as extreme ultraviolet lithography (EUV), electron projection lithography (EPL), and imprint lithography. Because next generation lithographies will require the development of substantially new infrastructure, the costs of these technologies will put great pressure on manufacturing costs.

DIFFICULT CHALLENGES

The ten most difficult challenges to the continued shrinking of minimum feature sizes are shown in Table 76. Mask-making capability and cost escalation continue to be critical to future progress in lithography and will require continued focus. As a consequence of prior aggressive Roadmap acceleration—particularly the MPU gate linewidth (post etch), and increased mask error factors (MEFs) associated with low k_1 lithography—mask linewidth control appears as a particularly significant challenge going forward. For example, in the 1997 roadmap the 70 nm node requirements showed 4× masks needing 9 nm of CD control for isolated lines and 14 nm for contacts. The 2003 requirements are 6.4 nm for isolated lines and 5.5 nm for contacts assuming mask error factor (MEF) values of 1.0 (assuming alt-PSM masks) and 3.0, respectively. MPU gate CD control requirements will stress many other aspects of lithography process control, including lenses, resist processing equipment, resist materials, and metrology.

Mask equipment and process capabilities are in place for manufacturing masks with complex OPC and PSM, while mask processes for post-193 nm technologies are in research and development. Mask damage from electrostatic discharge (ESD) has long been a concern, and it is expected to be even more problematic as mask feature sizes shrink. Furthermore, masks for 157 nm lithography will be kept in ambient atmospheres nearly free of water, so the risk of ESD damage to masks will increase. A cost-effective pellicle solution has not yet been fully developed for 157 nm masks, further complicating mask handling for lithography at that wavelength.

While lithography has long contributed significantly to over-all semiconductor manufacturing costs, there is even greater concern going forward regarding cost control and return-on-investment (ROI). These issues of masks and lithography costs are relevant to optical, as well as next-generation lithography. To be extended further, optical lithography will require new resists that will provide both good pattern fidelity when exposed with short wavelengths (193 nm, possibly under immersion, and 157 nm), and improved performance during etch. Inadequacies in resist performance and CaF_2 quality and supply have already led to a slowdown in the pace of advances in lithography.

Process control, particularly for overlay and linewidths, also represents a major challenge. It is unclear whether metrology, which is fundamental to process control, will be adequate to meet future requirements as needed for both development and volume manufacturing. Resist line edge roughness (LER) is becoming significant, as gate linewidth control becomes comparable to the size of a polymer unit. Next-generation lithography will require careful attention to details as the exposure tools are based upon approaches that have never been used before in manufacturing. These tools must be developed and proven to be capable of meeting the reliability and utilization requirements of cost-effective manufacturing.

Table 76 Lithography Difficult Challenges

Five Difficult Challenges/ ≥ 50 nm Through 2009	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Registration, CD control, defectivity, and 157 nm pellicles; defect free multi-layer EUV substrates or EPL membrane masks Equipment infrastructure (writers, inspection, repair)
Cost Control and Return on Investment (ROI)	Achieving constant/improved ratio of tool cost to throughput over time Cost-effective resolution enhanced optical masks and post-optical masks Sufficient lifetimes for the technologies Resources for developing multiple technologies at the same time High output, cost-effective, EUV light source
Process Control	Processes to control gate CDs to less than 1.8 nm (3 sigma) New and improved alignment and overlay control methods independent of technology option to < 19 nm overlay Accuracy of OPC
Resists for ArF, Immersion Lithography and F_2	Outgassing, LER, SEM-induced CD changes, defects ≥ 30 nm.
CaF_2	Yield, cost, quality
Five Difficult Challenges/ < 45 nm Beyond 2010	
Mask Fabrication and Process Control	Defect-free NGL masks Equipment infrastructure (writers, inspection, repair) Mask process control methods
Metrology and Defect Inspection	Capability for critical dimensions down to 7 nm and metrology for overlay down to 7.2 nm, and patterned wafer defect inspection for defects < 30 nm
Cost Control and ROI	Achieving constant/improved ratio of tool cost to throughput Development of cost-effective post-optical masks Achieving ROI for industry with sufficient lifetimes for the technologies
Gate CD Control Improvements, Process Control, Resist Materials	Development of processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness Development of new and improved alignment and overlay control methods independent of technology option to < 7.2 nm overlay
Tools for Mass Production	Post optical exposure tools capable of meeting requirements of the Roadmap

SEM—scanning electron microscope

LITHOGRAPHY TECHNOLOGY REQUIREMENTS

The lithography roadmap needs are defined in the following tables:

- Lithography Requirements (Tables 77a and b)
- Resist Requirements (Tables 78a, b, and c)
- Mask Requirements (Tables 79a, b, and c)

Because of the particular challenges associated with imaging contact holes, contact hole size after etch will be smaller than the lithographically imaged hole, similar to the difference between imaged and final MPU gates. This is important to comprehend in the Roadmap, because contacts have very small process windows and large mask error factors, and minor changes in the contact size have large implications for mask CD control requirements. Small MPU gates after etch are pursued aggressively and create significant challenges for metrology and process control.

Photoresists need to be developed that provide good pattern fidelity, good linewidth control (including roughness), and low defects. As feature sizes get smaller, defects and polymers will have comparable dimensions with implications for the filtering of resists.

The masks for all next-generation lithographies are radically different from optical masks, and no NGL technology can support a pellicle. Because the requirements for NGL masks are substantially different than those for optical lithography, separate tables have been included for Optical, EUV, and EPL masks (Tables 79a, b, and c, respectively). These masks have tight requirements for linewidth control and registration, because they will be applied at the 45 nm and beyond. EUV masks must also have very tight flatness control, and there are additional requirements for various parameters associated with reflectivity of EUV masks. EPL masks are comprised of thin membranes, and have special requirements. NGL masks, being different in form from optical masks, will also require the development of new defect inspection capabilities. Solutions for protecting the masks from defects added during storage, handling and use in the exposure tool need to be developed and tested, because there are no known pellicle options for NGL masks. These very different NGL mask requirements can be expected to exacerbate, rather than relieve, the high costs associated with masks that are already being encountered with optical masks.

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