

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SYNOPSYS, INC.  
Petitioner

v.

MENTOR GRAPHICS CORPORATION  
Patent Owner

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Case IPR2012-00041  
Patent 6,947,882 B1

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Before SALLY C. MEDLEY, HOWARD B. BLANKENSHIP, and  
JENNIFER S. BISK, *Administrative Patent Judges*.

BISK, *Administrative Patent Judge*.

DECISION  
Institution of *Inter Partes* Review  
*37 C.F.R. § 42.108*

Synopsys, Inc. filed a petition to institute an *inter partes* review of U.S. Patent 6,947,882 B1 (the “882 patent”). 35 U.S.C. § 311. For the reasons that follow, the Board, acting on behalf of the Director, has decided not to institute an *inter partes* review. 35 U.S.C. § 314.

OPINION

I. INTRODUCTION

A. Background

Petitioner requests *inter partes* review of claims 1-14 and 17-20 of the '882 patent alleging that each of the claims is unpatentable under 35 U.S.C. §§102 and 103 based on the following prior art references: U.S. 5,960,191 (Ex. 1002) (“Sample '191”) including U.S. 5,475,830 (Ex. 1003) (“Chen”) incorporated by reference; U.S. 6,020,760 (Ex. 1004) (“Sample '760”); and U.S. 5,761,484 (Ex. 1005) (“Agarwal”). Of the challenged claims, claims 1 and 5 are independent, claims 2-4 depend from claim 1, and claims 6-14 and 17-20 depend from claim 5. The grounds specified by the Petitioner are detailed below.

Reference	Claims challenged under §§ 102 and 103
Sample '191 including Chen	1-14, 17-20
Sample '760	5-8, 17-20
Agarwal	5-8, 17, 20

The '882 patent is involved in concurrent district court litigation. On August 17, 2012, Mentor Graphics filed an infringement complaint against EVE-USA, Inc. and Emulation and Verification Engineering, S.A. *Mentor Graphics v. EVE-USA, Inc.*, 12-cv-01500 (D. Or.). That proceeding has not been stayed and currently has a Markman hearing scheduled for July 23, 2013 and a five day jury trial set for June 16, 2014. Minutes of Tel. Conference, *Id.* (Dec. 12, 2012), ECF No. 60.

B. The '882 patent (Ex. 1001)

The '882 patent generally relates to systems for emulating integrated circuit designs. '882 col. 1, ll. 8-9. In particular, the patent describes a “regionally time multiplexed emulation system”—an emulation system with increased capacity over the prior art due to an emulator separated into different regions, each region constituting a separate time domain. *See* '882 Abstract; col. 11, 41-42. The patent states that this separation of the emulator into separate time domain regions allows asynchronous logic to be emulated without hard-wiring signals to dedicated pins and reduces the problem of synchronizing clock signals across a large area. '882 col. 11, ll. 41-49.

The challenged claims encompass two independent claims, reproduced below, with emphasis added:

1. An emulation system comprising:
  - a first plurality of reconfigurable logic devices;
  - a second plurality of reconfigurable logic devices;
  - a third plurality of reconfigurable logic devices;
  - a first time multiplexed interconnection coupled to and situated between the first plurality of reconfigurable logic devices and the second plurality of reconfigurable logic devices; and
  - a second time multiplexed interconnection coupled to and situated between the second plurality of reconfigurable logic devices and the third plurality of logic devices, *wherein clocking of the second time multiplexed interconnection is independent of clocking of the first time multiplexed interconnection.*

5. An emulator for emulating a circuit design, comprising:
  - a first reconfigurable logic device that includes a first plurality of reconfigurable logic elements and first input/output circuitry;
  - a second reconfigurable logic device that includes a second plurality of reconfigurable logic elements and second input/output circuitry;
  - a first clock signal for clocking the first plurality of reconfigurable logic elements;
  - a second clock signal for clocking the second plurality of reconfigurable logic elements; and
  - at least one signal routing clock signal for clocking at least one of the first input/output circuitry and the second input/output circuitry, *wherein the signal routing clock signal is independent of the first clock signal and the second clock signal.*

## II. DECISION ON PETITION

### A. Overview

For the reasons described below, we decline to institute an *inter partes* review of any of the challenged claims based on any of the proposed grounds.

### B. Claim Construction

As a step in our analysis for determining whether to institute a trial, we determine the meaning of the claims. Consistent with the statute and the legislative history of the AIA, the Board will interpret claims using the broadest reasonable construction. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012); 37 CFR § 100(b). There is a “heavy presumption” that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002). By “plain meaning” we refer to the

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ordinary and customary meaning the term would have to a person of ordinary skill in the art. Such terms have been held to require no construction. *See, e.g., Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1349 (Fed. Cir. 2001) (finding no error in non-construction of “melting”); *Mentor H/S, Inc. v. Med. Device Alliance, Inc.*, 244 F.3d 1365, 1380 (Fed. Cir. 2001) (finding no error in court’s refusal to construe “irrigating” and “frictional heat”).

Petitioner submits that for purposes of this review, the claim terms take on the ordinary and customary meaning that the terms would have to one of ordinary skill in the art. Pet. 5. Patent Owner does not appear to dispute this. *See generally* Prelim. Resp. With one exception, we agree that for purposes of this decision the claim terms require no construction and we give those claims their plain and ordinary meaning in the context of the specification.

The one exception is “wherein clocking of the second time multiplexed interconnection is independent of clocking of the first time multiplexed interconnection” as required by independent claim 1 or “wherein the signal routing clock signal is independent of the first clock signal and the second clock signal” as required by independent claim 5 (collectively, the “independent clock signal limitation”). Petitioner implicitly asserts that the independent clock signal limitation encompasses asynchronous clock signals originating from a single clock. For example, in a claim chart, Petitioner cites, without further explanation, the following text in Sample ’191 and Chen as disclosing the independent clock signal limitation.

A High Speed Asynchronous Clock Signal **144** is distributed to all chips in

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