

SEL EXHIBIT 2014

INNOLUX CORPORATION v. PATENT OF SEMICONDUCTOR ENERGY
LABORATORY CO., LTD.

IPR2013-00068

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
3
4

5 INNOLUX CORPORATION,

Petitioner,

6 vs.

No. IPR2013-00060

7 Patent 7,697,102

PATENT OF SEMICONDUCTOR,

8 ENERGY LABORATORY CO., LTD.,

9 Patent Owner.
10 -----
11
12

13 VIDEOTAPED DEPOSITION OF MILTIADIS HATALIS, Ph.D.

14 Irvine, California

15 Friday, July 12, 2013
16
17
18
19

20 Reported by:

21 SHERRY A. CASE, RPR, CLR,

22 CSR No. 2989

23 Job No. 1683387
24

25 PAGES 1 - 178

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8 Patent 7,697,102

9 PATENT OF SEMICONDUCTOR,
10 ENERGY LABORATORY CO., LTD.,

11 Patent Owner.
12

13 Videotaped Deposition of
14 MILTIADIS HATALIS, Ph.D., taken on behalf of Patent
15 Owner, at 3 Park Plaza, Suite 1100, Irvine,
16 California, beginning at 9:03 a.m., and ending at
17 6:53 p.m. on Friday, July 12, 2013, before
18 SHERRY A. CASE, Certified Shorthand Reporter
19 No. 2989, CLR, RPR.
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16 VERITEXT LEGAL SOLUTIONS

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I N D E X

WITNESS: MILTIADIS HATALIS, Ph.D.

EXAMINATION

BY MR. SCHLITTER:

8

E X H I B I T S

EXHIBIT	DESCRIPTION	PAGE
Exhibit 1005	Exhibit CMI 1005 captioned "Declaration of Miltiadis Hatalis, Ph.D."	10
Exhibit 1001	United States Patent 7697102 Hirakata previously marked as CMI Exhibit 1001	16
Exhibit 1003	Previously been marked as CMI Exhibit 1003, Shiba, et al., United States Patent No. 5684555	60
Exhibit 2006	Enlarged version of Figure 4 from the Shiba reference	76
Exhibit 2007	Enlarged version of Figure 3	118
Exhibit 1004	CMI Exhibit 1004	172

1 Irvine, California; Friday, July 12, 2013 09:02
2 9:03 A.M.
3 09:03
4 THE VIDEO OPERATOR: Good morning. 09:03
5 We are on the record at 9:03 a.m. on July 12th, 09:03
6 2013. This is the video-recorded deposition of 09:03
7 Dr. Milt Hatalis. 09:03
8 I'm Scott Slater, here with our court reporter, 09:03
9 Sherry Case. We are here from Veritext Legal 09:04
10 Solutions at the request of the patent owner. 09:04
11 This deposition is being held at 3 Park Plaza, 09:04
12 Suite 1100, in the City of Irvine, California 92614. 09:04
13 The caption of this case is Innolux Corporation versus 09:04
14 Patent of Semiconductor Energy Laboratory Co. dot -- 09:04
15 or Co., LTD, Case No. IPR 2013-00060, Patent 7697102. 09:04
16 Please note that audio and video recording will 09:04
17 take place unless all parties agree to go off the 09:04
18 record. The microphones are sensitive and may pick up 09:04
19 whispers, private conversations, or cellular 09:04
20 interference. 09:05
21 I am not authorized to administer an oath. I 09:05
22 am not related to any party in this action, nor am I 09:05
23 financially interested in the outcome in any way. 09:05
24 May I please have an agreement from all parties 09:05
25 that we may proceed. 09:05

1 MR. SCHLITTER: We agree. 09:05

2 MR. CORDREY: Yes. 09:05

3 THE VIDEO OPERATOR: Thank you. 09:05

4 At this time, will counsel and all present 09:05

5 please identify themselves for the record. 09:05

6 MR. SCHLITTER: Stan Schlitter and Doug 09:05

7 Peterson from Steptoe & Johnson for the patent owner, 09:05

8 and also Sean Flood from Robinson & Marshall 09:05

9 Intellectual Property Office for the patent owner. 09:05

10 MR. CORDREY: Gregg Cordrey of Jeffer, Mangels, 09:05

11 Butler & Mitchell on behalf of the petitioner, Innolux 09:05

12 Corporation. 09:05

13 THE VIDEO OPERATOR: Thank you very much. 09:05

14 Will the court reporter please administer the 09:05

15 oath. 09:05

16 THE COURT REPORTER: You do solemnly swear that

17 the testimony you're about to give in the cause now

18 pending to be the truth, the whole truth, and nothing

19 but the truth.

20 THE WITNESS: I do.

21

22 MILTIADIS HATALIS, Ph.D.

23

24 having been first administered an oath, was examined

25 and testified as follows:

EXAMINATION

1
2 09:05
3 BY MR. SCHLITTER: 09:05
4 Q Good morning, Dr. Hatalis. 09:05
5 A Good morning. 09:05
6 Q Since your deposition's been taken several 09:05
7 times before, I will skip some of the preliminary 09:06
8 things about depositions, but just remind you, of 09:06
9 course, you're under oath and -- and obligated by law 09:06
10 to tell the truth to all the questions. 09:06
11 Do you understand that? 09:06
12 A Yes. 09:06
13 Q And also, if I ask a question that you do not 09:06
14 understand, please let me know. If you -- if you 09:06
15 don't let me know that, it will be assumed that you've 09:06
16 understood the question that I asked. 09:06
17 A Okay. 09:06
18 Q Did you do anything to prepare for your 09:06
19 deposition today? 09:06
20 A I did. 09:06
21 Q What did you do? 09:06
22 A I review my declaration. I review the 09:06
23 petition. I review the initial response, preliminary 09:06
24 response of the patent owner. I review the decision 09:06
25 from -- of the board. I review the relevant patent, 09:07

1 the '102 Patent, and the -- the prior art patent that 09:07
2 I list in my declaration, namely, the Shiba patent and 09:07
3 the Moriyama patent. 09:07

4 Q Did you review any other document to prepare 09:07
5 for your deposition today? 09:07

6 A I -- I review briefly the transcripts of the 09:07
7 last three depositions, particularly as -- as one of 09:07
8 them related to the Shiba. 09:07

9 The Shiba was a prior art in another recent 09:07
10 deposition of mine. 09:07

11 Q Do you remember which deposition it was? 09:07

12 A Was that 206? It was... 09:07

13 MR. CORDREY: 204. 09:07

14 THE WITNESS: 204. Okay. 09:07

15 BY MR. SCHLITTER: 09:07

16 Q Is that the only transcript you reviewed? 09:07

17 A Recently. 09:08

18 A few weeks ago, I review the -- the 09:08
19 transcripts for the first three depositions that 09:08
20 were -- were held in this room in May. 09:08

21 Q Your depositions, you mean? 09:08

22 A Right, my depositions in re to '480 and '978. 09:08

23 I didn't read those ones for today's 09:08
24 deposition. 09:08

25 And I also met with a -- with my counsel. 09:08

1 Q When did you meet? 09:08

2 A The last two days. 09:09

3 Q Who specifically did you meet with? 09:09

4 A Mr. Glenn Cordrey and his colleague, 09:09

5 Ali Shalchi. 09:09

6 Q Other than reviewing those depositions and the 09:09

7 meeting you had for the last two days, did you do 09:09

8 anything else to prepare for your deposition today? 09:09

9 A I -- I don't recall. No. 09:09

10 Q Okay. I've put in front of you what was 09:09

11 previously marked as Exhibit CMI 1005 captioned 09:09

12 "Declaration of Miltiadis Hatalis, Ph.D." 09:09

13 Do you recognize this? 09:09

14 A Yes. This is my declaration in support of the 09:10

15 petition for the Patent '102. 09:10

16 (Exhibit 1005 was previously marked

17 for identification and is attached

18 hereto.)

19 BY MR. SCHLITTER:

20 Q Referring to Appendix A, which is your 09:10

21 curriculum vitae, is this accurate and up to date? 09:10

22 A More or less as of the time of -- of the 09:10

23 writing, which was in November. 09:10

24 Q Was there a change you would make to update it 09:11

25 as of today? 09:11

1 litigation cases this case, regard this case. 09:13

2 And in the area of -- of the grants, research 09:13

3 funding, which is the -- the last section in mine, I 09:13

4 receives two additional research gifts since the time 09:13

5 that this vitae was prepared. 09:14

6 Q Were any of the grants that you've received 09:14

7 recently that are not listed on this Appendix A ones 09:14

8 you received from industry? 09:14

9 A They were all from industry. 09:14

10 Q Were any of them from any company outside the 09:14

11 United States? 09:14

12 A No. 09:14

13 These are U.S.-based companies. Some of them 09:14

14 may have international divisions, but they are 09:14

15 U.S.-based companies. 09:14

16 One of them -- actually, that one, I think, was 09:14

17 listed. 09:14

18 One gift was from Supralaboratories of America, 09:15

19 SLA. They're -- it's a U.S.-based company. 09:15

20 But the other company is Sharp in Japan. 09:15

21 Q Did you read every word of this declaration 09:15

22 before you signed it? 09:15

23 A This is my declaration. Of course I read every 09:15

24 word, to make sure there are not inaccuracy and stuff 09:16

25 like that. 09:16

1 But I have also prepared this declaration. 09:16

2 Q What was the process that you went through to 09:16
3 prepare this declaration? 09:16

4 A I review the '102 Patent. I review prior art, 09:16
5 literature, namely, patents. And I received guidance 09:16
6 from the -- from the counsel related to the format and 09:16
7 the -- the process of preparing because this is a new 09:17
8 proceeding. 09:17

9 By the time of '102, I have already prepared 09:17
10 one or two. They may be not the sequence. This is 09:17
11 probably the third or the fourth in -- in a series of 09:17
12 five that I worked on in the fall of 2012. 09:17

13 Q Did you do any prior art searching in 09:17
14 connection with preparing this declaration? 09:17

15 A I was provided with a folder of -- that 09:17
16 included several pieces of -- of prior art, and I 09:17
17 became familiar with those pieces of prior art, and I 09:17
18 selected the ones most relevant to prepare this 09:17
19 declaration. 09:18

20 Q Who provided you that folder of prior art 09:18
21 patents? 09:18

22 A The counselor, Oblon. 09:18

23 Q Who specifically? 09:18

24 A Scott McHugh is the lead counsel. I -- 09:18
25 I -- I worked with other attorneys at Oblon. 09:18

1 declarations of mine, which means -- which means prior 09:21
2 to the onset of these preparations, which means prior 09:21
3 to, I guess, September of 2012. 09:21

4 Before working on the '102 Patent, I worked on 09:21
5 the '480 Patent, and the '102 and '480 share the same 09:21
6 specifications. So right before '102, I became 09:21
7 familiar with the '480. 09:21

8 But prior to the September of 2012, I do not 09:21
9 recall seeing these -- any of these patents. 09:21

10 Q Who prepared the first draft of this 09:22
11 declaration? 09:22

12 A The outline, the format of what needs to be 09:22
13 done, the different sections, because I've never done 09:22
14 this before. As I said, these are new proceedings, 09:22
15 was provided by the Oblon. 09:22

16 But the content in the different sections, 09:22
17 these were my content. This is content that I 09:22
18 provided. 09:23

19 Q So I have handed you a copy of United States 09:23
20 Patent 7697102, Hirakata, et al. It's marked 09:23
21 previously as CMI Exhibit 1001. 09:23

22 Is this the so-called '102 Patent you've been 09:23
23 referring to? 09:23

24 A Yes. 09:23

25 (Exhibit 1001 was previously marked 09:24

1 for identification by the court

2 reporter and is attached hereto.)

3 BY MR. SCHLITTER:

4 Q Do you understand that this '102 Patent 09:24

5 discloses first, second, and third internal conducting 09:24

6 lines? 09:24

7 A Yes. 09:24

8 Q So, for example, Claim 15 refers to a first 09:24

9 internal conducting line and a second internal. 09:25

10 conducting line. 09:25

11 What do those correspond to, in your opinion, 09:25

12 in the '102 Patent? 09:25

13 MR. CORDREY: Objection. Form. 09:25

14 THE WITNESS: The '102 Patent is describing 09:25

15 connections between an extractor terminal and the 09:25

16 common contact portions, and there are four sets of 09:26

17 common contact portions that provide a signal to the 09:26

18 counter electrode. 09:26

19 Starting from the extractor terminal -- 09:26

20 BY MR. SCHLITTER: 09:26

21 Q Are you referring to a figure? 09:26

22 A Figure 13 is the common contact portions, and 09:26

23 Figure 3 lists the four sets in common contact -- the 09:26

24 presence of four sets contact -- common contact 09:27

25 portions. 09:27

1 Q Where are the common contact portions shown in 09:27
2 Figure 3? 09:27

3 A These are the 206a, 206b, 206c, 206d. 09:27

4 Q Are extractor terminals shown in Figure 3? 09:27

5 A The ones connected to the common contact 09:27
6 portions are the 205a and the 205b. 09:27

7 Q Are there other extractor terminals in 09:27
8 Figure 3, other than 205a and 205b? 09:27

9 A Yeah. 09:27

10 There are a plurality of -- of... 09:27

11 Q Do you understand that numeral 205 was a lead 09:27
12 line going to inside of a dashed line to encompass 09:28
13 extractor terminals, to identify extractor terminals? 09:28

14 A Give me one second, please. 09:28

15 There are many extractor terminals highlighted 09:29
16 or labeled as 205 that provide electric power and 09:29
17 control signals from the outside to the various parts 09:29
18 on the substrate 201, and those parts are the 09:29
19 peripheral circuits that drive the display. These are 09:29
20 the -- peripheral circuits are the 203 and 204. 09:30

21 And two of those extractor terminals are 09:30
22 connected and provide the power to the common contact 09:30
23 portions which I have identify a moment ago, 206a, b, 09:30
24 c and d. 09:30

25 Q Are the two extractor terminals that provide 09:30

1 power to the common contact portions labeled in 09:30
2 Figure 3? 09:30
3 A These are 205a and 205b. 09:30
4 Q Are 205a and 205b referred to in the '102 09:31
5 Patent as common terminals? 09:31
6 A That is correct. 09:31
7 That is in Column 8, Line 15. It is 09:31
8 electrically connected with common terminals 205a and 09:31
9 205b, respectively. 09:31
10 Let me read the whole quote. Column 8, 09:31
11 Line 14, it reads, 09:31
12 "The internal lines 207a and 207b 09:32
13 extend to the extractor terminals 205 09:32
14 and are electrically connected with 09:32
15 common terminals 205a and 205b, 09:32
16 respectively." 09:32
17 So the bigger question, of course, related to 09:32
18 the first internal conducting line and the second 09:32
19 internal conducting line. These are lines that are 09:32
20 used in these internal lines 207a and 207b. 09:32
21 Q If you look at Claim 15, one of the elements of 09:32
22 Claim 15 reads as follows, 09:33
23 "A first internal conducting line 09:33
24 electrically connected to the common 09:33
25 terminal in the contact hole wearing 09:33

1 the first internal conducting line and 09:33
2 a gate electrode of the thin-film 09:33
3 transistor are created by a first 09:33
4 processing step." 09:33
5 Is the first internal conducting line shown in 09:33
6 Figure 3? 09:33
7 A It is the line 207c. 09:33
8 And in Column 9, Line 61, it reads, 09:34
9 "The internal conducting lines 207c 09:34
10 and the gate electrode 307 were 09:34
11 created by the same processing step." 09:34
12 Q Referring again to Claim 15, another element of 09:35
13 Claim 15 reads as follows, 09:35
14 "A second internal conducting line and 09:35
15 a source electrode and a drain 09:35
16 electrode of the thin-film transistor 09:35
17 created by a second processing step." 09:35
18 Is a second internal conducting line shown in 09:35
19 Figure 3? 09:35
20 A It is shown. 09:35
21 Q Where is that shown? 09:36
22 A For example, line 207a. 09:36
23 Q Claim 39 includes the following element, 09:36
24 "A third internal conducting line 09:37
25 formed from a same layer as the source 09:37

1 electrode and the drain electrode of 09:37
2 the thin-film transistor, the third 09:37
3 internal conducting line electrically 09:37
4 connected to the first internal 09:37
5 conducting line and the third internal 09:37
6 conducting line electrically connected 09:37
7 to the common terminal." 09:37
8 Is a third internal conducting line shown in 09:37
9 Figure 3? 09:37
10 A Let me first complete my answer to your 09:38
11 previous question and I will answer this question. 09:38
12 Your previous question was is a second internal 09:38
13 conducting line shown in Figure 3, and I answered it 09:38
14 is shown. 09:38
15 And you asked me where is that shown, and I 09:38
16 gave you an example of line 207a. 09:38
17 Within the context of the limitations described 09:38
18 in Claim 15, another example of the second internal 09:39
19 conducting line is the line 207b. So if we look at 09:39
20 the Claim 15, there are two lines that meeting the 09:39
21 limitations of the second internal conducting line. 09:39
22 Turning to the latest question, related to 09:39
23 Claim 39, in the third internal conducting line, 09:39
24 the -- one of those two lines, namely, 207a or 207b, 09:40
25 can be viewed as the third internal conducting line. 09:40

1 So within the context of the Claim 39, one of 09:40
2 the 207a and 207b is the third internal conducting 09:40
3 line and the other is the second internal conducting 09:40
4 line. 09:41

5 Q You identified terminals 205a and 205b as the 09:41
6 common terminals, correct? 09:41

7 A That is correct. 09:41

8 Q What material are those terminals formed from 09:41
9 in the '102 Patent? 09:41

10 A The claims refer to the common terminal as 09:41
11 being formed from the same layer as the pixel 09:42
12 electrode, but the common terminals 205a and 205b, as 09:42
13 shown in Figure 3, are electrically connected to the 09:43
14 wiring that leads to 206a and 206d, and that wiring -- 09:43
15 since 207a and 207b, which we have identified them as 09:43
16 the second internal conducting lines is made by the 09:43
17 same material as the drain electrodes and the source 09:43
18 electrodes, the layer of the common terminal made by 09:43
19 the pixel electrode material is connected to the layer 09:44
20 of material made by the source and drain electrode. 09:44

21 So the common terminal or the extractor 09:44
22 terminal is the multi-layer structure. The upper 09:44
23 layer, referred to as the common terminal, is made by 09:44
24 the pixel electrode layer, whereas the lower layer is 09:44
25 made by the source and drain electrode layer. 09:44

1 In this particular embodiment. It could be 09:44
2 made with another material as well. It could be made 09:45
3 with the same material as the -- as that used to make 09:45
4 the first internal conductor lines. It is not clear 09:45
5 how it is made. 09:45

6 The claim specifies that the common terminal, 09:45
7 the layer which is made by the pixel electrode 09:45
8 material, is electrically connected to the first 09:45
9 internal conducting lines. So someone skilled in the 09:46
10 art could see that one way to do that is to have a 09:46
11 layer of the first internal conducting lines being 09:46
12 connected -- electrically connected in the extractor 09:46
13 terminal region itself. 09:46

14 The specifications are not clear, and I believe 09:46
15 they're not providing a cross-section of the extractor 09:46
16 terminals itself. There is enough detail in the 09:46
17 cross-sections provided for the common contact 09:46
18 portions. 09:46

19 Another approach is to have the lower level -- 09:47

20 Q Stop right there. 09:47

21 Where in the specification is there a 09:47
22 disclosure that the common terminals are more than a 09:47
23 single layer of material? 09:47

24 A In the specifications or in the claims? 09:47

25 Q In -- in the '102 Patent specification. 09:47

1 A For example, in Column 10, Line 15, it reads, 09:50
2 "Moreover, the contact holes for 09:51
3 connecting the internal conducting 09:51
4 lines 318," and in parentheses, "207a 09:51
5 and 207b," close parentheses, "with 09:51
6 the common terminals 205a and 205b at 09:51
7 the extractor terminals 205 were 09:51
8 formed." 09:51
9 So in this section here, Column 10, Line 15 to 09:51
10 18, it indicates that in the extractor terminal we 09:51
11 have the common terminals, and there is a contact hole 09:51
12 in the extractor terminal that connects with another 09:51
13 layer, and that layer could be the same layer as that 09:52
14 used to make the internal conducting lines 207a and 09:52
15 207b. 09:52
16 So someone skilled in the art would understand 09:52
17 that you have the common terminal and there is a 09:52
18 contact hole, there must be another layer below it, 09:52
19 and hence it is disclosed is a multi-layer structure. 09:52
20 Q But yet, you mean -- you think the common 09:53
21 terminal is multi-layer or do you mean this whole 09:53
22 composite of things in that sentence is multi-layer? 09:53
23 A That the extractor terminal is a multi-layer 09:53
24 structure. And one layer, which you have it in the 09:53
25 files, a common terminal, is the Indium tin oxide. 09:53

1 There will be another layer, and the two will 09:53
2 be connected. 09:53

3 Q They will be connecting in the contact hole? 09:53

4 A There will be a contact hole. 09:53

5 The -- the common terminal may be physically 09:53
6 touching the other metal, and then there is -- 09:54

7 Q "Other metal" meaning what? 09:54

8 What other metal? 09:54

9 A Like the metal that is making the 207a and 09:54
10 207b, for example. 09:54

11 Q Do you mean in the contact hole? 09:54

12 A Well, in general, there are -- in making a 09:54
13 display, there are multiple layers, multiple metal 09:54
14 layers, and there are three such metal layers. There 09:54
15 is a metal layer used to make the gate lines or the 09:54
16 gate electrodes, the metal layer used to make the data 09:54
17 lines and the source and drain electrodes, and there 09:54
18 is the metal layer used to make the pixel electrodes. 09:55
19 Two of those layers are used in the extractor 09:55
20 terminals. 09:55

21 Now, in addition to those layers, those 09:55
22 conductive layers, there are two insulating layers. 09:55

23 Q Where are the two layers -- where is it 09:55
24 disclosed that the extractor terminals are two layers? 09:55

25 Let me back up and withdraw that question. 09:55

1 claims refer to as the common terminal. That is -- 09:57
2 that's the upper layer. The upper exposed metal 09:57
3 layer. 09:57
4 But the section I quoted -- 09:58
5 Q Meaning Lines 15 through 18? 09:58
6 A Right. It says that at the extractor terminals 09:58
7 there are contact holes, and that the internal 09:58
8 conducting lines and the common terminals are 09:58
9 connected in the extractor terminal regions. 09:58
10 So there are multi-layer structures that are 09:58
11 connected. Different layers are connected in the 09:58
12 extractor terminals. 09:58
13 Q What do you understand is meant in Lines 15 and 09:59
14 16 by the phrase "contact holes for connecting the 09:59
15 internal conducting lines 318," paren, "207a and 09:59
16 207b," close paren, "with the common terminals 205a 09:59
17 and 205b"? 09:59
18 That's actually Lines 15 to 17. 09:59
19 A As I stated earlier, there are three metal 10:00
20 layers and there are also two insulating layers. The 10:00
21 one insulating layer is the gate electric. Oh, 10:00
22 actually, to be clear, it depends upon the device 10:00
23 structure, there may be three insulating layers. 10:00
24 For the -- the structure depicted in the -- in 10:01
25 the prior art, which is a top gate TFT, the three 10:01

1 dielectric layers are the gate dielectric, the 10:01
2 incremental dielectric between the scan line material, 10:01
3 the gate dielectric metal, and the drain electrode 10:01
4 metal. And then there is the passivation layer that's 10:01
5 the third dielectric. All these are above the TFT 10:01
6 structure. 10:01

7 Q Are you referring to a figure? 10:01

8 A Figure 13. 10:01

9 Q The gate dielectric in Figure 13 is unlabeled, 10:01
10 correct? 10:02

11 There's not a number by it? 10:02

12 A No, it's not labeled. 10:02

13 Q But it's the one that would override the gate 10:02
14 lines or the gate electrodes? 10:02

15 A It would be below the gate electrodes. It 10:02
16 would be between the gate electrodes and the 10:02
17 semiconductor that makes the thin-film transistor. 10:02
18 That's the gate electrode in these structures here. 10:02

19 In amorphous silicon technology, which they 10:02
20 have the bottom gate, in that technology the gate 10:02
21 electrode is above. The gate electrode, in this 10:02
22 technology, is below the gate electrode. 10:02

23 Q Is this a bottom gate or top gate technology? 10:02

24 A In Figure 13, it is a top gate. 10:02

25 Do you want me to show you on the figure where 10:03

1 it is? 10:03

2 Q Is it under the crossed-hatched rectangle 10:03

3 towards the left -- bottom left of Figure 13? 10:03

4 A If you're referring to the gate electrode in 10:03

5 the middle of the transistor, yes. 10:03

6 Q The first white strip right under the 10:03

7 crossed-hatched gate electrode would be the gate 10:03

8 dielectric, correct? 10:03

9 A Right. 10:03

10 It's a very thin layer in this schematic. 10:03

11 Q Then there's a second dielectric, also 10:04

12 unlabeled, that overlies both the gate dielectric and 10:04

13 the gate electrode in this Figure 13, correct? 10:04

14 A Correct. 10:04

15 Q That's what you referred to as -- did you say 10:04

16 intern metal -- 10:04

17 A Right. It's -- the -- consider the gate 10:04

18 electrode is a metal and the source and drain 10:04

19 electrode is also made by metal, then that dielectric 10:04

20 serves the two metals being in electrical isolation. 10:04

21 So then the gate lines and data lines do not 10:04

22 have electrical connection when they're crossing, and 10:04

23 there will be many such crossings in the display area. 10:04

24 Q Is the third insulating layer that you 10:04

25 mentioned the passivation layer shown in Figure 13? 10:05

1 A The third is label 18, the element 18 in 10:05
2 Figure 13. So there you have the three metal layers. 10:05
3 And in this technology here, the three insulating 10:05
4 layers. 10:05
5 And referring to the extractor terminal, one 10:05
6 possible way of making the extractor terminal will be 10:05
7 exactly the same as that shown in Figure 13 as the 10:05
8 common contact portion. 10:05
9 And in a way, it -- it -- someone skilled in 10:06
10 the art will look at the common contact portion, and 10:06
11 there are four such areas where these common contact 10:06
12 portions are made, and then will implement the exact 10:06
13 same structure in the extractor terminal. 10:06
14 And in this technology where the metals are 10:06
15 laying in this particular order and the dielectrics, 10:06
16 the insulating layers that we referred to are also put 10:06
17 down in this specific order, then, in the extractor 10:06
18 terminal, the -- what will be the common terminal, 10:07
19 which is a layer made of the pixel electrode, will go 10:07
20 down to an opening, which we'll call it contact hole, 10:07
21 and will then touch, as shown in Figure 13, the lower 10:07
22 layer, which is made of the source and drain electrode 10:07
23 material, and the structure there would be similar 10:07
24 here. So the upper layer will be like layer element 10:07
25 22 of Figure 13, and the lower layer will be like the 10:07

1 element 21 in Figure 13, and then there will be a 10:07
2 contact hole as shown in Figure 13. 10:08

3 But that's one of -- of -- of possible two 10:08
4 implementations in this particular embodiment, in this 10:08
5 particular way of putting the material down, this is 10:08
6 how it would be made. 10:08

7 Q You said this is one of two possible 10:08
8 implementations. 10:08

9 What is the other possible implementation, in 10:08
10 your opinion? 10:08

11 A The other possible implementation will be to 10:08
12 have the -- so we start from the metal -- the source 10:08
13 and drain metal layer. And looking at Figure 13, it's 10:08
14 the element labeled 21. 10:08

15 There are two layers above that metal layer 10:08
16 labeled 21. It is the insulating layer label 18 and 10:09
17 the metal layer that forms element 22 and 19, which is 10:09
18 the pixel electrode layers. In this particular 10:09
19 embodiment, at least the 18 -- the insulating layer 10:09
20 above 21, and 19 and 22 above 18. 10:09

21 The other way to build this structure is to 10:09
22 reverse the order and put the pixel electrode layer 10:09
23 that forms the elements 19 and 22 after patterning 10:09
24 right above element 21 and right above the source and 10:09
25 drain electrode shown in the pixel region, and then 10:10

1 put the insulating layer 18 above them. 10:10

2 You will still need to have an opening so that 10:10

3 the conductive particles 26 will make a contact to the 10:10

4 counter electrode, element 24. 10:10

5 In the second approach that I just highlight, 10:10

6 one would have to adjust the design so that the 10:10

7 element 19 that you see in the pixel region will not 10:10

8 extend and will not overlap with the other device 10:10

9 terminal, will only make physical contact with one of 10:10

10 the device terminals. And the other one -- 10:11

11 Q By "device terminals," you mean source or 10:11

12 drain? 10:11

13 A Right. 10:11

14 The -- the device is very symmetric. We'll 10:11

15 call them one source and the other drain. And one 10:11

16 side is connected to the data lines and the other side 10:11

17 is connected to the pixel electrode. 10:11

18 In the embodiment that you put 19 right on top 10:11

19 of the, say, drain electrode, you want to make -- if 10:11

20 we call the ones touching the drain electrode, the 10:11

21 other one, we will call it source, will be connected 10:11

22 to the gate lines, and 19 should not touch the source 10:11

23 electrode because then it will be connected to the 10:11

24 data lines. 10:11

25 So you need to adjust the -- the layout so that 10:11

1 19 will only touch one of the two electrodes. 10:12

2 In any way, that region which overlaps the -- 10:12

3 the source electrode and the gate line -- the drain 10:12

4 lines, these are not -- non-illuminating regions 10:12

5 because the metal blocks the light. 10:12

6 So stopping the pixel electrode short of 10:12

7 touching the other metal, the other side of 10:12

8 transistor, will not have any effect on the properties 10:12

9 of the transmissive display because the -- the metal, 10:12

10 anyway, will -- will be blocking the light. 10:12

11 Q So Figure 13, which is labeled prior art, that 10:12

12 you're talking about, in your modification you would 10:12

13 make layer 22 the same layer as the pixel electrode 10:13

14 and eliminate -- on the outside of the pixel region, 10:13

15 you would eliminate insulating layer 18; is that 10:13

16 correct?

17 A No. I would not eliminate 18. 18 will -- will 10:13

18 be over that extra layer. 10:13

19 Q Okay. You would put it on top of layer 22 10:13

20 instead of beneath it? 10:13

21 A Correct. 10:13

22 And then you will form the opening so the 10:13

23 conductive particle 26 makes the electrical connection 10:13

24 to the counter electrode 24. 10:13

25 Q Then, are you -- are you saying the pixel 10:14

1 electrode 19 would be at the same -- be formed from 10:14
2 the same layer as the layer 22? 10:14
3 A Yes. 10:14
4 You still have three metal layers. 10:14
5 Q So at the same time you lay down the pixel 10:14
6 electrodes, you -- you would lay down layer 22, 10:14
7 correct?
8 A Well, 19 and 22 are from -- from the same 10:14
9 initial metal layer. 10:14
10 Q Would they both -- 10:14
11 A After -- after patterning, the elements 19 and 10:14
12 22 are formed. 10:14
13 Q If you put the drain on -- I mean, the pixel 10:14
14 electrode 19 beneath the insulating film 18, 10:14
15 insulating layer 18, would the spacers 25 then be 10:15
16 riding on top of the insulating film 18, in your 10:15
17 modified version, in the pixel region? 10:15
18 A If I understand your question, well, that would 10:15
19 depend upon whether in the pixel region you leave the 10:15
20 layer 18, that insulating layer, intact; in other 10:15
21 words, you do not form an opening to expose the pixel 10:15
22 electrode 19. And in that case, the insulating -- the 10:15
23 spacers 25, they would be above 18. 10:16
24 Q So they would just rest on 18 in your modified 10:16
25 version? 10:16

1 A Well, my modify version has, in that particular 10:16
2 region, two other modifications. In one modification 10:16
3 is what we just discussed, in which the 18 stays 10:16
4 intact. And in that case, 25 are above 18. 10:16

5 The other modification that one can do in the 10:16
6 pixel region is to create an opening on top of the 10:16
7 pixel electrode same way that you have the opening in 10:16
8 the common contact portion, in -- in where, above the 10:16
9 pixel electrode region, you will remove the insulating 10:17
10 layer 18. 10:17

11 In that case, the spacers 25, they will be on 10:17
12 top of the pixel electrode 19. In that case, they 10:17
13 could be the same size as 26. 10:17

14 Q None of that is disclosed in the '102 Patent, 10:17
15 is it? 10:17

16 A Well, all that are natural extensions of -- 10:17
17 of -- of what was known in the prior art, and here it 10:17
18 shows one particular implementation, one particular 10:17
19 embodiment, one particular structure. 10:17

20 The motivation for removing 18 above the pixel 10:17
21 electrode is to reduce the driving voltage, the 10:18
22 operating voltage for the display. All those -- all 10:18
23 those things were well known in the art. 10:18

24 Q What is the function, in Figure 13, of the 10:18
25 insulating layer 18 in the pixel region? 10:18

1 A Well, it serves to provide a protection and a 10:18
2 passivation to the thin-film transistor and to the 10:18
3 conductive lines that are on the display. 10:18

4 There are hundreds or thousands of data lines 10:19
5 that go across the display and interconnect each pixel 10:19
6 to the circuit or to the external drivers, so then 10:19
7 the -- each pixel will receive the right signal. And 10:19
8 those lines, they will need to be protected and be 10:19
9 locally isolated. 10:19

10 Q Does the transistor labeled 17 in Figure 13 10:19
11 show a source and drain electrode? 10:19

12 A Yes, it shows them. They're not labeled, but 10:19
13 it -- it shows them.

14 Q And then one of them is connected to the pixel 10:20
15 electrode 19, correct? 10:20

16 A Yes.

17 Q The other one is not connected to pixel 10:20
18 electrode 19, is it? 10:20

19 A Correct. 10:20

20 Q Would the device function if both the source 10:20
21 and drain electrodes were connected to the pixel 10:20
22 electrode 19? 10:20

23 A As I said -- as I said a few lines above in my 10:20
24 previous answer, that the pixel electrode 19 will have 10:20
25 to be modified so it will not touch the other 10:20

1 transistor terminal. 10:20

2 Q So it won't function if it touches the other 10:20

3 transistor terminal, correct? 10:20

4 A It will not function. 10:20

5 And that's why it has to be isolated from it, 10:20

6 and that's a simple change in the mask, and that's how 10:20

7 all pixels designs that employ such structure have 10:21

8 been referred to in -- in the literature. They always 10:21

9 were known, and it was shown in -- in the path, even 10:21

10 the one side used that are not touching it, even if 10:21

11 they are right above it. 10:21

12 Q In Figure 13, isn't it correct that insulating 10:21

13 layer 18 serves to electrically isolate the source and 10:21

14 drain electrodes from each other? 10:21

15 A The source and drain electrodes are -- are not 10:21

16 connected in -- in Figure 13 with or without the 10:22

17 insulating layer 18. 10:22

18 The insulating layer 13 -- 10:22

19 Q You mean 18? 10:22

20 A Yes. Yes, insulating layer 18. 10:22

21 The insulating layer 18 provides further 10:22

22 protection in those two layers and protection against 10:22

23 corrosion or mechanical scratches. And if it is 10:22

24 moisture, maybe removes conductive paths through the 10:22

25 moisture. That is not that the source and drain 10:22

1 electrode are isolated, because 18 is right above it. 10:22

2 But even in the modification structure that I 10:23

3 have described, you still use layer 18. You -- you 10:23

4 have a modified 19, and then you will still put 18 10:23

5 above it. So the purpose of 18 will still be 10:23

6 maintained to provide the protection and further 10:23

7 isolation of the TFT structure. 10:23

8 Q Which of the terminals in Figure 13 of the 10:23

9 transistor connects to the pixel electrode 19? 10:23

10 A Looking at the figure, it is the terminal on 10:23

11 the right. 10:23

12 Q Call that the drain? 10:23

13 A We can call that the drain. 10:24

14 Q Okay. So the drain in Figure 13 of the TFT 17 10:24

15 connects to pixel electrode 19, correct? 10:24

16 A Correct. 10:24

17 Q In Figure 13, is it correct that pixel 10:24

18 electrode 19 needs to be electrically isolated from 10:24

19 the other terminal of the transistor, the TFT 17, 10:24

20 which would be the source electrode? 10:24

21 A It has to be isolated. And that's why, if you 10:24

22 have 19 above the drain electrode, 19 will be -- will 10:24

23 have a different shape, an outline than the one shown 10:24

24 in Figure 13. It will not extend over it. 10:24

25 See, this particular display structure is shown 10:25

1 in Figure 13, is a reflective type display. This was 10:25
2 a -- a special type of -- of -- of displays not 10:25
3 commonly used. And in a reflective display, you would 10:25
4 like to maximize the area where the light gets 10:25
5 reflected. 10:25

6 So in -- in making a reflective display, you 10:25
7 will probably choose to make the structures as shown 10:25
8 in Figure 13, where you would choose to put the 10:25
9 insulating layer first, 18, and then put the pixel 10:25
10 electrode 19. So then you can overlap other metal 10:25
11 lines and maximize the amount of light that you will 10:25
12 reflect from the top surface. 10:26

13 And that's why the section that you -- you 10:26
14 skipped earlier, it causes the pixel electrodes -- it 10:26
15 is a metal layer and we call it highly reflective 10:26
16 metal layer that includes aluminum. 10:26

17 Q Where did you see that? 10:26

18 A See what? 10:26

19 Q The aluminum. The pixel electrode layer 10:26
20 includes aluminum. 10:26

21 A So if we look at Column 10, I believe that is 10:26
22 the section that you were still reading a moment ago, 10:26
23 and you skip some sections. 10:26

24 So in Column 10, line 31, it reads: 10:26

25 "A thin metal film which would 10:27

1 later be made into pixel electrodes 10:27
2 322 and a conducting pad 323 were 10:27
3 formed to a thickness of 100 to 400 10:27
4 nanometer," period. 10:27
5 "In the present example, the thin 10:27
6 metal film was made of an aluminum 10:27
7 film containing one weight percent 10:27
8 titanium from deposit to a thickness 10:27
9 of 300 nanometer by sputtering. Then 10:27
10 the thin metal film was patterned to 10:27
11 form the pixel electrodes 322 in the 10:27
12 conducting pad 323." 10:27
13 The extractor terminals -- few sentences 10:27
14 below -- were also patent, and that's what you read, I 10:27
15 believe, a moment ago. 10:28
16 So in this particular type of reflective 10:28
17 displays, you need to maximize the pixel electrode 10:28
18 area on the surface because the light will come from 10:28
19 the top, and it will be reflected also from the top. 10:28
20 In a transmissive display, and the great 10:28
21 majority of -- of displays that we use are 10:28
22 transmissive displays, the light will -- will come 10:28
23 from one side of the display and will emerge through 10:28
24 the pixel electrode, will travel through pixel 10:28
25 electrode. They will merge from the other side 10:28

1 of the -- of -- of -- of the other glass, the counter 10:28
2 substrate. 10:28

3 In those -- in -- in the transmissive displays, 10:28
4 any metal layer which is used to form the source 10:28
5 electrode, drain electrode, gate electrodes and data 10:28
6 lines and scan lines, they all are blocking the light. 10:28
7 So there is no motivation for 19 to extend, in a 10:29
8 transmissive display, over the other transistor 10:29
9 terminal because the light there will already be 10:29
10 blocked by the underlying metal. 10:29

11 And because the electron functionality requires 10:29
12 not to be connected, it serves no purpose to -- to 10:29
13 extend it. The display will equally function fine. 10:29

14 It will function, actually, without being 10:29
15 extended, and you will not suffer any limitation in a 10:29
16 transmissive display if you do one structure or the 10:29
17 other structure. The performance of display, it will 10:29
18 be exactly the same if you put 19 above 18 or if you 10:29
19 put 19 below 18. For a transmissive display, the 10:29
20 performance of display, the visual performance will be 10:30
21 exactly the same. 10:30

22 Q You have been describing your proposed 10:30
23 modifications of the prior art structure that's shown 10:30
24 in Figure 13. 10:30

25 But looking now at the -- at the structure that 10:30

1 is the subject of the '102 Patent, that's in Figures 3 10:30
2 and Figure 5, A through G, do you see that Figure 5 10:30
3 shows also three insulating layers? 10:30
4 A Yes. 10:30
5 Q And those would be the gate dielectric, which 10:30
6 would be on top of the substrate, correct? 10:31
7 A The gate dielectric is -- what's shown in 10:31
8 Figure 5A is element 303. 10:31
9 Portions of those films, as you see, are 10:31
10 extended below the gate electrodes, element 305, and, 10:31
11 hence, takes its name gate dielectric because it's 10:31
12 between the gate and the semiconductor, which is the 10:31
13 element label 302. 10:31
14 Q And there's an insulating layer 315 also, 10:31
15 correct?
16 A Right. 10:32
17 This is what we call early in our discussion as 10:32
18 the first incremental dielectric. 10:32
19 Q And then there's a third insulating film 10:32
20 labeled 319, correct? 10:32
21 A Correct. 10:32
22 We'll call that passivation layer. 10:32
23 Q In Figure 5G, passivation layer 319 serves to 10:32
24 electrically isolate the pixel electrode 322 from the 10:32
25 source electrode that is the electrode on the left of 10:32

1 the TFT, correct? 10:32

2 A In this particular embodiment, which is stated 10:32

3 is a reflective display, you would need to maximize 10:33

4 the -- the size of the pixel electrode 322 because 10:33

5 light will come from the top and they will be 10:33

6 reflected again outwards. So light will come in from 10:33

7 the top and would go out from the top. 10:33

8 In that case, you do need to maximize the area 10:33

9 where you have metal that will reflect the light. And 10:33

10 322 is such highly reflective metal -- as you read, 10:33

11 it's aluminum -- and in this type of display, someone 10:33

12 skilled in the art will know that this is the 10:33

13 preferred embodiment because you will maximize the 10:33

14 pixel electrode. 10:33

15 But that's -- approach, that structure, it -- 10:33

16 it is -- is not the approach you will take if you have 10:33

17 a transmissive display. You will not need -- you will 10:34

18 not gain anything by overlapping 322 above the source 10:34

19 electrode because the source electrode and the drain 10:34

20 lines, they will block the light from -- from below. 10:34

21 And you could use them as a black matrix. 10:34

22 That's another -- another approach. But normally 10:34

23 there is a black matrix already on the display, on the 10:34

24 counter substrate. 10:34

25 Q Let me ask the question again, which you did 10:34

1 not answer. 10:34

2 In Figure 5G, is it correct that passivation 10:34

3 layer 319 serves to electrically isolate the pixel 10:34

4 electrode 322 from the source electrode that is the 10:35

5 electrode on the left of the TFT? 10:35

6 A In this particular embodiment, where you need 10:35

7 to maximize the 322, the layer 319 does serve to 10:35

8 electrically isolate the pixel electrode 322 from the 10:36

9 source electrode. 10:36

10 Q Is it your opinion that in a transmissive type 10:36

11 liquid crystal display, it's not important to maximize 10:36

12 the area of pixel electrode? 10:36

13 A You need to maximize the area of the pixel 10:36

14 electrode from the areas that light will go through. 10:36

15 And if you have a metal line, such as the scan line 10:36

16 and the data line and the source electrode, light 10:36

17 cannot go through those areas because the metal lines 10:37

18 will block the light. 10:37

19 So you would not gain advantages by overlapping 10:37

20 the pixel electrode to, say, the data lines. 10:37

21 Q Do you understand, with reference to Figures 5A 10:37

22 through G, that the gate electrode is 308? 10:37

23 You can see that in Column 8, Line 67. 10:37

24 A Yeah, I see that in Figure 5C, label 308. 10:37

25 That's a gate electrode. 10:37

1 Q Because I think earlier you mentioned 305 is 10:37
2 the gate electrode. 10:37

3 A It is shown as the 305 in Figure 5A. 10:37

4 Then there is some processing done in this -- 10:37
5 again, in this particular embodiment, there is some 10:37
6 processing done. There is some anodization step that 10:38
7 grows an oxide to 305. That oxide is labeled 306 in 10:38
8 Figure 5B. After -- and that narrows down the initial 10:38
9 gate electrode 305. 10:38

10 The remaining material after that step is what 10:38
11 is labeled as a 308. 10:38

12 Q Okay. 10:38

13 MR. SCHLITTER: Let's take a break here. 10:38

14 THE VIDEO OPERATOR: Off the record? 10:38

15 MR. SCHLITTER: Sure. 10:38

16 THE VIDEO OPERATOR: We are off the record. 10:38

17 The time is 10:38 a.m. on July 12, 2013. This is the 10:38
18 end of Video No. 1 of the continuing deposition of 10:38
19 Dr. Milt Hatalis. 10:38

20 (Recess taken.) 10:38

21 THE VIDEO OPERATOR: We are on the record. The 11:02
22 time is 11:02 a.m. on July 12, 2013. This is the 11:02
23 beginning of Video No. 2 of the deposition of 11:02
24 Dr. Milt Hatalis. 11:02

25 BY MR. SCHLITTER: 11:02

1 Q In Column 10, the language we looked at before 11:02
2 the break, Lines 15 through 18 talks about "contact 11:02
3 holes for connecting the internal conducting lines 11:02
4 318," paren, "207a and 207b," close paren, "with the 11:02
5 common terminals 205a and 205b at the extractor 11:02
6 terminals." 11:02

7 With reference to Figure 5 of the '102 Patent, 11:02
8 in what layer do you understand the contact holes are 11:03
9 formed? 11:03

10 A Well, in this particular embodiment described 11:03
11 in detail in Figure 5, in the schematics of Figure 5, 11:03
12 the contact holes will be in the final passivation of 11:03
13 layer, which -- which is labeled two different numbers 11:04
14 of -- in Figure 5 is -- so it's -- that -- sorry. It 11:04
15 is labeled as 319. 11:04

16 Q Not a different number, it's just 319? 11:04

17 A Yes. It -- it is shown in Figure -- it is 11:04
18 labeled in Figure 5 as 319. 11:04

19 Q That's an insulating layer, right? 11:04

20 A That is an insulating layer. 11:04

21 In this particular embodiment, the order with 11:04
22 which you lay down the layers is such that on top of 11:04
23 the -- say the wiring 318 made from the source and 11:04
24 drain electrode material, you lay down the insulating 11:05
25 layer 319 above it, you open the contact holes, and 11:05

1 then you put down the pixel electrode material. 11:05

2 Q Do you understand the language that we just 11:05

3 quoted in Column 10 to mean that the common terminals 11:05

4 formed from the pixel electrode layer are connected to 11:05

5 the internal connecting lines 207a and 207b by the 11:05

6 contact holes? 11:05

7 A Well, in this particular embodiment, where you 11:05

8 have an insulating layer between two conductive 11:06

9 layers, without the contact holes the two layers will 11:06

10 not -- will not be in contact. There will be one 11:06

11 above the other one, but there will be an insulating 11:06

12 layer in between them. They will not be able to touch 11:06

13 each other to form an electrical connection. 11:06

14 Q Is it appropriate to put a passivation layer 11:06

15 over a pixel electrode? 11:07

16 MR. CORDREY: Objection. Form. 11:07

17 MR. SCHLITTER: Let me restate the question. 11:07

18 That objection was well-taken. 11:07

19 BY MR. SCHLITTER: 11:07

20 Q Is it appropriate to put a passivation layer on 11:07

21 top of a pixel electrode so that the passivation layer 11:07

22 is between the pixel electrode and the counter 11:07

23 substrate? 11:07

24 A The -- the structure that you describe is in 11:07

25 one of the structures that have been reported in the 11:07

1 prior art quite extensively. And that was... 11:08

2 Q Are you finished? 11:08

3 Let me ask a related question. 11:08

4 Is the passivation layer typically transparent? 11:08

5 A Yes. 11:08

6 You're talking about the insulating layer, 11:08

7 correct? Like the element 319 in the figure of 5A? 11:08

8 Q Do you understand 319 to be a transparent 11:08

9 layer? 11:09

10 In Figure 5? 11:09

11 A I think it's made of a silicone oxide, a 11:09

12 silicone nitrite, and these are transparent layers. 11:09

13 Q Does this -- 11:09

14 A Actually -- 11:09

15 Q Go ahead. 11:09

16 A There are -- there are -- as we've discussed, 11:09

17 there are a multi-layer -- there are multiple 11:09

18 dielectric layers. Some of them are the silicone 11:09

19 oxide and silicone nitrite, or combinations of those 11:09

20 two. 11:09

21 And some of them, this particular one, 319, 11:09

22 which is the second interlayer dielectric film, that 11:09

23 is an organic material. Important to be like -- in 11:10

24 Column 10, it refers to be as a polymite. 11:10

25 Q Is that also a trans -- transient light -- 11:10

1 transparent light? 11:10

2 A Organic -- organic coatings can be made to be 11:10

3 transparent. In this particular display type, where 11:10

4 you're talking about a -- a reflective display, that's 11:10

5 not a requirement. 11:10

6 But in transmissive displays, where light will 11:10

7 come from one side, connect the other side, 11:11

8 the -- all the dielectrics have to be, you know, 11:11

9 transparent. 11:11

10 Q Is it desirable to have the pixel electrode 11:11

11 near to the counter electrode on the counter 11:11

12 substrate? 11:11

13 MR. CORDREY: Objection to form. 11:11

14 THE WITNESS: Earlier on in the art, it -- it 11:11

15 was not placed near. You had the passivation layer on 11:11

16 top of it. 11:11

17 It became evident in the art that if you -- if 11:11

18 you do so, you need higher operating voltages, and 11:11

19 that may have a higher power consumption. And in the 11:11

20 art, the advantages of -- of putting the pixel 11:12

21 electrode on top of the insulating layer were also 11:12

22 recognized. 11:12

23 And in between those two structures you have -- 11:12

24 have the other structure, which I've describe earlier, 11:12

25 where you remove the passivation layer on top of the 11:12

1 pixel electrode and you eliminate it, and -- and that 11:12
2 is almost behaving as you have it on the top. It's 11:12
3 only a wave by the thickness of a dielectric layer 11:12
4 from the counter substrate. 11:12
5 BY MR. SCHLITTER: 11:12
6 Q So it puts the pixel electrode a little farther 11:12
7 away from the counter electrode if you put the 11:12
8 passivation layer on top of the pixel electrode, 11:13
9 correct?
10 A If you put it below -- 11:13
11 Q The question is if you put it above. 11:13
12 A If you put it above it, your gap -- your 11:13
13 distance is whatever is distance of your spacers. If 11:13
14 you put it below, it is the distance -- you've got the 11:13
15 distance of the spacer plus the thickness of the 11:13
16 dielectric. 11:13
17 If you remove the passivation layer on top of 11:13
18 the pixel electrode -- let's say it's below, but you 11:13
19 etch it, you open an opening above it -- then most of 11:13
20 the area is determined by the -- by those openings. 11:13
21 And if you change your spacers, you could adjust 11:13
22 the -- the -- the gap based on the spacer thickness. 11:14
23 I mean, these are all variations that were -- 11:14
24 were implemented in -- in the prior art. They're all 11:14
25 different structures that have been reported, and 11:14

1 advantage, disadvantages of -- of each were well 11:14
2 understood by people in the art. 11:14

3 Q With reference to Column 10, Lines 15 to 18, 11:14
4 and Figure 3 of the '102 Patent, how do you understand 11:14
5 the connection is made between the internal conducting 11:14
6 lines 207a or 207b? 11:14

7 Or -- well, let me just restate that. 11:14

8 The connection between 207a and 205a, how do 11:14
9 you understand that connection to be made? 11:14

10 A One possible way to make that connection -- and 11:14
11 there are many ways to make that connection. 11:15

12 One possible way to make that connection is as 11:15
13 shown in Figure 5. If you replace the element 318 11:15
14 with the element 207a and you extend 207a all the way 11:15
15 out to the extractor terminal regions, that will be 11:15
16 one way to make that structure. 11:16

17 Q In that case, what role does the contact hole 11:16
18 for connecting the lines 207a and 207b to the common 11:16
19 terminals 205a and 205b play? 11:16

20 A In this case, where you have an insulating 11:16
21 layer put on top of the contacting line, the opening 11:16
22 in the insulating layer allows the upper metal layer 11:16
23 to go down the hole and touch the metal layer at 11:16
24 the -- in -- in the region which is between the walls 11:17
25 of the opening, and, thus, the two metal layers stop 11:17

1 contact. 11:17

2 Q For example, common terminal 205a would go down 11:17

3 a contact hole -- or some metal from common terminal 11:17

4 205a -- or the same layer as common terminal 205a 11:17

5 would go down a contact hole and make contact with 11:17

6 internal conducting line 207a? 11:17

7 A The metal would -- forms the common terminal, 11:17

8 or the metal from which the common terminal is made of 11:18

9 will go down the edges of the hole, as shown in 11:18

10 Figure 5, and they will attach the other metal layer 11:18

11 which is used to make the lines 207a -- the line 207a. 11:18

12 Q That corresponds to layer 318 in Figure 5E, 11:19

13 correct?

14 A That is correct. 11:19

15 If we take that particular embodiment and we 11:19

16 use that approach discussed in Figure 5 to make the 11:19

17 common terminals, that will be one way to make that 11:19

18 connection. 11:19

19 Q Is there any other embodiment that's explicitly 11:19

20 disclosed in the '102 Patent? 11:19

21 A Well, the claims -- all the claims require that 11:19

22 the first internal conducting line electrically 11:19

23 connected to the common terminal in the contact hole, 11:19

24 while one way to make the first internal conducting 11:20

25 line to be electrically connected to the common 11:20

1 terminal is to make the lower metal layer, which 11:20
2 extends into the extractor terminal, made from the 11:20
3 same metal that is used to make the first internal 11:20
4 conducting line, and that metal would be the metal 11:20
5 that is used to make the gate electrode of the 11:20
6 thin-film transistor. 11:20

7 Q If you did that, then you would not need a 11:20
8 contact hole; is that right? 11:20

9 A Why do you say that? 11:20

10 Q Well, if the extractor in the common terminal 11:20
11 is same metal and the same layer as internal 11:20
12 conducting line 207a, then they would already be 11:21
13 connected, wouldn't they? 11:21

14 What -- how would you connect layers or two -- 11:21
15 two elements in the same layer with a hole? 11:21

16 How would you do that? 11:21

17 A I hope I didn't misspeak. I simply say you 11:21
18 still have a common terminal made from the same layer 11:21
19 as the pixel electrode. And that layer made from the 11:21
20 pixel electrode, called common terminal, in the 11:21
21 extractor terminal will make an electrical connection 11:21
22 to the first internal conducting line in the common 11:22
23 terminal region. 11:22

24 And as we see -- 11:22

25 Q Well, will it make that connection in a -- in. 11:22

1 the contact hole? 11:22

2 A You require it to have the contact hole because 11:22

3 a first internal conducting line, which is made by the 11:22

4 material of the gate electrode, is also below an 11:22

5 insulating layer. So there are insulating layers 11:22

6 above the first internal conducting line, and, thus, 11:22

7 you would need to have a contact hole to make that 11:22

8 connection. 11:22

9 Q And that same -- that's also true with respect 11:22

10 to the second integral conducting line, 207a or 207b, 11:22

11 for example, and the common terminal 205a and 205b, 11:23

12 right? 11:23

13 They also are separated by an insulating layer 11:23

14 in the '102 Patent? 11:23

15 A In the particular embodiment in '102 Patent, 11:23

16 that is true. 11:23

17 In the case of the first internal conducting 11:23

18 line, there will be insulating layers above the gate 11:23

19 electrode. We -- we -- we see that -- that a layer 11:23

20 315 is above the gate electrode layer. And if we 11:23

21 visualize that the 318 shown in Figure 5A is not made 11:23

22 by the same material as the source and drain 11:23

23 electrode, but it is made by the material of the gate 11:24

24 electrode, then that element 318 will be below 315. 11:24

25 And the layer 315 is a required layer. That 11:24

1 layer serves to isolate the data lines and the scan 11:24
2 lines. So it is -- that order there is -- is an 11:24
3 explicit required order because the data lines and 11:24
4 scan lines will have to be isolated. 11:24

5 So no matter what is the technology, whether 11:24
6 it's a top gate or a bottom gate, there's always -- 11:24
7 there's always an insulating layer between the gate 11:24
8 electrode layer and the source and drain electrode 11:24
9 layer. In that case, a contact hole is -- will be 11:25
10 required. 11:25

11 In the case of the -- where the 318 layer is 11:25
12 made from the same as the -- same as the source and 11:25
13 drain electrode, in that case there are two options to 11:25
14 make -- to put the common terminal above that one. 11:25
15 One is shown, and which we discussed, that you have 11:25
16 the insulating layer above it. You open the -- 11:25

17 Q That would be 319 in Figure 5? 11:25

18 A Correct. 11:25

19 You would open the contact holes and then you 11:25
20 put down the pixel electrode layer, or you put the 11:25
21 pixel electrode layer first and then you open the -- 11:25
22 then you put the passivation layer 319. 11:25

23 Q But that's not disclosed in the '102 Patent, 11:26
24 correct?

25 A In the particular embodiment shown in this 11:26

1 Figure 5, that's not disclosed. 11:26

2 But that was disclosed in the prior art, and 11:26

3 both embodiments were well-known in the art. 11:26

4 Q Do you understand, with respect to Figure 3, 11:26

5 that the internal conducting line 207c is made from 11:26

6 the -- or formed from the same metal as the gate 11:26

7 electrodes? 11:26

8 A And I believe I refer you to the quote. Like 11:26

9 in Column 9, Line 61, it reads, 11:26

10 "The internal conducting lines 207c 11:26

11 and the gate electrode 307 were 11:27

12 created by the same processing steps." 11:27

13 Q Did you also understand that internal 11:27

14 conducting lines 207a and 207b are formed from the 11:27

15 same metal layer as the source, drain electrodes? 11:27

16 A Correct. 11:27

17 As discussed here, that is how they are stated, 11:27

18 and I read you that section earlier. 11:27

19 Q Is it correct that internal conducting line 11:27

20 207c runs between the common contact portions 206b and 11:28

21 206c? 11:28

22 A In the embodiment shown in Figure 3, that 11:28

23 wiring 207c is the only one that has been identified 11:29

24 as having been made by the material of the gate 11:29

25 electrode. So in this particular embodiment, that 11:29

1 will be correct. 11:29

2 However, the claim language is more broad 11:29

3 because the claim language -- that is Column 17 of 11:29

4 Line 60 -- 11:29

5 Q You're consulting your declaration for this? 11:30

6 A I want to refer you to one of the claims, that 11:30

7 it is part of this proceeding. I don't -- there are 11:30

8 many numbers, I didn't remember all of them, and this 11:30

9 is not marked. I don't want to refer you to a claim 11:30

10 that is not part of this proceeding, so... 11:30

11 I believe I refer you to Claim 31, which is not 11:30

12 part of the proceedings. 11:30

13 Q Well, Claim 15 is part of it. 11:30

14 A All right. Yeah. 11:30

15 15 doesn't talk about where those lines are 11:30

16 extended. Some of the other, later claims provide 11:30

17 that language. 11:30

18 Q 27 is another claim in the proceeding. 11:31

19 A Yes. 11:31

20 So if we look at Claim 27, and that's in 11:31

21 Column 17, Line 24, it reads, 11:31

22 "Wherein the first internal conducting 11:31

23 line extends along at least a second 11:31

24 edge of the substrate, the second edge 11:31

25 being opposed to the extractor 11:31

1 terminals and being perpendicular to 11:31
2 the first edge." 11:31
3 So if we look at the Figure 3 -- and you 11:31
4 already have identified the extractor terminals 205 11:31
5 clearly shown in Figure 3 -- the edge which is opposed 11:31
6 to the extractor terminals will be the edge that 207c 11:31
7 will -- will -- will run along. 11:32
8 But the claim language is broad, and it says 11:32
9 that extends along at least that edge, which means 11:32
10 that the wiring or the line that is made of this 11:32
11 material could extend along other edges as well. 11:32
12 Q In the embodiment described in the patent, in 11:32
13 the specification, internal conducting lines 207a and 11:32
14 207b are at the source, drain metal level, and 11:32
15 internal conducting line 207c is at the gate line 11:32
16 level, correct? 11:33
17 A That is correct. 11:33
18 Q Would you say that there is a physical 11:33
19 demarcation between 207a and 207c? 11:33
20 MR. CORDREY: Objection. Vague. 11:33
21 THE WITNESS: Where? In the specifications or 11:33
22 in the claims? 11:33
23 BY MR. SCHLITTER:
24 Q Given the structure of 207a and 207c as 11:33
25 described in the specification, do you understand 11:33

1 there to be a physical demarcation between 207a and 11:33
2 207c? 11:34

3 A Well, the specification describe a particular 11:34
4 embodiment, describe a particular of structure. 11:34

5 Q That's the one I'm talking about. The question 11:34
6 is focused on the one that's described there. 11:34

7 A The one that is described in Figure 3 and refer 11:34
8 to the sections in the text that we refer to in the 11:34
9 specifications, it -- it limits in that edge only. 11:34

10 Q I'm not sure I understood your answer. "It 11:34
11 limits in that edge only"? 11:35

12 Do you mean the answer is that there is a 11:35
13 physical demarcation done between 207a and 207c as 11:35
14 described in the specification and figures of the '102 11:35
15 Patent? 11:35

16 A Well, 207c is shown -- is the element in 11:35
17 Figure 3 which is along the edge which is opposing 11:36
18 that of the extractor terminal. 11:36

19 And in the specifications, it -- in Column 9, 11:36
20 Line 59, it -- it reads, 11:37

21 "These conducting lines 207a and 207b 11:37
22 were connected with internal 11:37
23 conducting lines 207c at the common 11:37
24 contact portions 206b and 206c." 11:37

25 So the -- is an explicit demarcation where the 11:37

1 particular layer ends. I don't think there is an 11:37
2 explicit demarcation where it ends. 11:37
3 Where it connects to 207a and 207b, there is an 11:37
4 explicit demarcation, which is at the common contact 11:37
5 portions 206b and 206c. 11:38

6 Q Is there any disclosure in the specification of 11:38
7 the '102 Patent, an explicit disclosure, that line 11:38
8 207a is anything other than a single layer formed from 11:38
9 the source, drain metal layer? 11:38

10 My question is only with respect to the 11:39
11 specification. 11:39

12 A I understand your question. 11:39

13 With regards to the specification, it states 11:39
14 that internal conducting lines 207a and 207b are made 11:39
15 with the same materials as source and drain 11:39
16 electrodes. But the specifications itself do not 11:39
17 limit that below 207a and 207b made by the material of 11:39
18 the source and drain electrode, that there may not be 11:40
19 another metal that will run in parallel, and the 207a 11:40
20 and 207b refers to the element above the insulating 11:40
21 layer 315 shown in Figure 5 and will not preclude that 11:40
22 something may be running below it. 11:40

23 It doesn't say that -- explicitly that nothing 11:40
24 runs below it. And if -- if it is, please bring that 11:40
25 to my attention. I miss it. 11:40

1 Q Do you consider 207a and 207c, as described in 11:40
2 the specification, to be one continuous line? 11:41

3 A 207a and 207c create a wiring structure that 11:41
4 connects 205a to the common contact portions 206a, b 11:41
5 and c. 11:42

6 I didn't understand what you mean by "one 11:42
7 continuous line." It is one continuous wiring 11:42
8 structure consisting of different materials at 11:42
9 different levels. But they are electrically 11:42
10 connected. 11:42

11 Q I've handed you what has previously been marked 11:42
12 as CMI Exhibit 1003, which is Shiba, et al., 11:43
13 United States Patent No. 5684555. 11:43

14 (Exhibit 1003 was previously marked 11:43
15 for identification by the court
16 reporter and is attached hereto.) 11:43

17 BY MR. SCHLITTER: 11:43

18 Q Is this the so-called Shiba reference that you 11:43
19 have referred to earlier today in your deposition? 11:43

20 A Yes. 11:43

21 Q Do you understand an object of the invention 11:43
22 described in the Shiba patent to be to reduce the 11:43
23 width of the seal region without lowering the strength 11:44
24 over the adhesion between the two substrates of a 11:44
25 liquid crystal display? 11:44

1 result in reducing the outside dimensions of the 11:47
2 panel. 11:47
3 Shiba, as I said, it disclosed a -- a -- a 11:47
4 wiring structure, and that wiring structure has some 11:47
5 additional benefits, which are listed in Column 6, 11:47
6 Line 40, and it reads, "The wiring defect can be 11:47
7 prevented and the manufacturing here can be improved." 11:47
8 And that's an additional benefit of the 11:47
9 disclosure of the invention of -- described in -- in 11:47
10 Shiba, which go beyond just reducing the overall size. 11:48
11 Q Do you understand that the invention described 11:48
12 in Shiba does not increase the number of manufacturing 11:48
13 steps? 11:48
14 I refer to Column 6, Line 30 to 33. 11:48
15 A That's correct. 11:48
16 Q Do you understand Shiba to include three 11:49
17 conductive layers of material on the TFT substrate? 11:49
18 A Correct. 11:49
19 Q What are those layers? 11:49
20 Could you just identify those, please? 11:49
21 A This is the layer that is used to form the gate 11:49
22 electrodes and the scanning lines. That's the one 11:49
23 layer. 11:50
24 Another layer is the layer that form the source 11:50
25 and drain electrodes in the data lines. 11:50

1 And a third layer is one form the pixel 11:50
2 electrodes. 11:50

3 Q Are there any insulating layers on the TFT 11:50
4 substrate in the Shiba structure? 11:50

5 A Yes. 11:50

6 Q What -- what insulating layers are disclosed in 11:51
7 Shiba? 11:51

8 A You have the gate dielectric layer. 11:51

9 Q Does that have a reference number on Figure 4? 11:51

10 A 211. 11:51

11 Another dielectric layer or insulating layer is 11:52
12 the tunnel protecting layer 215 made of silicone 11:52
13 nitrite. 11:52

14 Another dielectric layer or insulating layer is 11:53
15 a protective overcoat, 241, made of silicone nitrite. 11:53

16 Q Any others? 11:53

17 A There is an orientation film of 281. That's 11:53
18 typically an organic layer, and that's also an 11:53
19 insulating layer. 11:53

20 Q Any others? 11:53

21 A On the TFT substrate, I do not think so. 11:54

22 Q Does the gate dielectric layer 211 -- or is the 11:54
23 gate dielectric layer 211 located between two metal 11:54
24 layers, or two conductive layers? 11:54

25 A Yes. 11:54

1 Q What layers is -- what conductive layers is the 11:54
2 gate dielectric -- dielectric layer 211 between? 11:54

3 A It is between the data lines and the scanning 11:55
4 lines. It is between the gate electrode and the 11:55
5 amorphous silicone. And when the amorphous silicone 11:55
6 is turned on, the channel is considered to be 11:55
7 conductive. 11:55

8 It's also between the part of the element 11:55
9 called as the storage capacitor lines, and the portion 11:55
10 of the pixel electrodes above it were forming the 11:56
11 storage capacitor. 11:56

12 Q Is the storage capacitor you're referring to 11:56
13 indicated as CJ in Figure 4? 11:56

14 A Correct. 11:56

15 Q Is CJ one of the conductive elements of the 11:56
16 storage capacitor? 11:56

17 A It forms one plate of the storage capacitor. 11:56

18 Q What forms the other plate? 11:56

19 A In this particular embodiment, the pixel 11:57
20 electrode layer -- portions of pixel electrode layer 11:57
21 that are overlapping, and that pixel electrode layer, 11:57
22 which is Indium tin oxide, it's conductive in the 11:57
23 overlap defined in the storage capacitor area. 11:57

24 And there are two sides, so that storage 11:57
25 capacitor in one side is the element CJ, and the other 11:57

1 side is the pixel electrode material, and the overall 11:57
2 area of that storage capacitor is defined by the 11:57
3 overlap. That's where the storage capacitor exists. 11:57
4 Q Does the gate dielectric layer constitute the 11:57
5 dielectric of that storage capacitor? 11:58
6 A Correct. 11:58
7 Q Is that the only component of the dielectric 11:58
8 portion of that storage capacitor? 11:58
9 A In this particular embodiment, yes. 11:58
10 Q What is the reason for storage capacitor -- the 11:58
11 storage capacitor being there in Figure 4? 11:59
12 A The storage capacitor from -- helps to maintain 11:59
13 the voltage that is been held -- the voltage 11:59
14 difference held between the pixel electrode and the 11:59
15 counter electrode constant throughout the frame 11:59
16 period. It run... 11:59
17 Q Going back to these other layers, what is the 11:59
18 purpose of channel protective layer 215? 12:00
19 A The structure disclosed in Shiba is referred as 12:00
20 to a channel edge top structure. So this 215 is 12:00
21 referred to as channel edge top layer. Above the 12:00
22 layer 215, the source and drain electrodes, they will 12:00
23 be formed. 12:01
24 Before they will be formed, they will be 12:01
25 deposited as one continuous film. 12:01

1 Q Is that -- what kind of material is that that 12:01
2 you're referring to as the source, drain electrodes? 12:01

3 A I do not recall an explicit mention in Shiba of 12:01
4 the material. 12:01

5 Q Does the channel protective layer 215 come into 12:01
6 contact with the N-plus type amorphous silicon layer 12:02
7 217b? 12:02

8 I'm looking at Column 4, Lines 23 to 27. 12:02

9 A The N-plus amorphous silicon is interposed 12:02
10 between the drain electrode and the channel protective 12:02
11 layer. 12:03

12 Q What is on the other side of the channel 12:03
13 protective layer? 12:03

14 A Look at Line 23. It says -- starting from 12:03
15 Line 20, it reads, 12:03

16 "A source electrode 231 is formed 12:03
17 above one end portion of the channel 12:03
18 213 with a low-resistance 12:03
19 semi-conductive layer 217a made of an 12:03
20 N-plus type amorphous silicon 12:03
21 interposed there between." 12:04

22 Q Stop right there. 12:04

23 So that means the N-plus amorphous silicone is 12:04
24 between the source electrode 231 and the channel 213, 12:04
25 right?

1 Q You said it's a channel etch stop layer 215. 12:06

2 What is the function of channel etch stop layer 12:06

3 215? 12:06

4 A Well, in this structure you have the channel 12:07

5 layer, which is made of amorphous silicon form of the 12:07

6 gate dielectric. 12:07

7 Then you -- 12:07

8 Q Did you say formed of the gate dielectric? 12:07

9 A Form the gate -- 12:07

10 Q Formed on. 12:07

11 A Then you have the channel protecting layer 215. 12:07

12 That covers part of the channel -- part of the -- this 12:07

13 amorphous silicone and protect it above the gate 12:08

14 electrode. 12:08

15 After you do this -- these two layers, then 12:08

16 you -- you put down the doped amorphous silicone, and 12:08

17 then you put the metal layer that will form the source 12:08

18 and drain electrode. And both the doped amorphous 12:08

19 silicone, which is these N-plus type amorphous 12:08

20 silicone, when it comes down, is a continuous film, 12:08

21 and the metal which forms the source and drain 12:08

22 electrode, that's also continuous film. 12:09

23 And then you go into a patterning step, and 12:09

24 it -- followed by an etching step. So you etch first 12:09

25 the metal, and then you etch the N-plus amorphous 12:09

1 silicon. 12:09

2 And the channel protection layer 215 protects 12:09

3 the amorphous silicone that is used to form the 12:09

4 channel from the etchant that is used to etch the 12:09

5 N-plus amorphous silicone. 12:09

6 THE WITNESS: In the transcript it says "N-plus 12:09

7 F form." It's N-plus amorphous. 12:09

8 THE COURT REPORTER: Thank you.

9 BY MR. SCHLITTER:

10 Q Does the channel protective layer 215 overlie
11 the entire channel region?

12 A That's correct.

13 If it did overlie the channel region, the 12:10

14 channel may be damaged or -- or shorted, either 12:10

15 damaged during the etching or the N-plus amorphous 12:10

16 silicone, or may be shorted if somehow N-plus remains. 12:10

17 Actually, the last one -- strike the last one. 12:10

18 It will be damaged. 12:10

19 If the N-plus amorphous silicone somehow 12:11

20 remains, it will lead to a defect anyway. So -- 12:11

21 Q Does the -- is -- in the finished device, is 12:11

22 the channel protective layer 215 interposed between 12:11

23 the N-plus layer and the channel region? 12:11

24 A Well, part of -- part of the N-plus amorphous 12:11

25 silicone will overlap the channel protection layer, 12:11

1 and in -- in that overlap region, the -- that is true. 12:11

2 Q What -- 12:12

3 A In that -- in that overlap region, the channel 12:12

4 protection layer 215 is in between the N-plus 12:12

5 amorphous silicone and the channel. 12:12

6 Q Is there a portion of the device where the 12:12

7 N-plus does not overlap the channel protective layer? 12:12

8 A Well, on the left and right of the channel 12:12

9 protection layer 215, the N-plus amorphous silicone is 12:12

10 touching -- physically touching the -- the channel 12:12

11 layer. 12:12

12 Q You said that the channel protective layer 215 12:12

13 is used because, otherwise, the channel may be damaged 12:12

14 by the etching of the N-plus. 12:13

15 What did you mean by "damaged"? 12:13

16 A Well, there are -- there are two well 12:13

17 established amorphous silicone TFT structures. One 12:13

18 structure is the one depicted in this Figure 4 that 12:13

19 we're discussing. And in -- in this structure, N-plus 12:13

20 layer is either above the amorphous silicone or above 12:13

21 the -- the channel protecting layer. 12:13

22 Portions of the N-plus, which is above the 12:14

23 channel protecting layer -- and those portions are in 12:14

24 between the source and drain electrodes -- those 12:14

25 portions, they have to be etched away. If they will 12:14

1 remain, they will short the source and drain of the 12:14
2 device, and device will not work as a switch. That 12:14
3 will lead to a defect. 12:14

4 So there is an etching step that is performed 12:14
5 in the manufacturing that removes that material. 12:14
6 Because material is made -- is amorphous silicone, 12:14
7 that wet etching or dry etching, whatever one chooses 12:14
8 to use, will also etch the undoped amorphous silicone 12:14
9 which is used as the channel layer. 12:15

10 So in -- in -- in that regard, the presence of 12:15
11 the layer 215 will protect and prevent etching of the 12:15
12 amorphous silicone. 12:15

13 The other structure that -- so by doing that 12:15
14 one, the amorphous silicone layer 213 can be made very 12:15
15 thin. 12:15

16 Another structure, which is called a back 12:15
17 channel etch, TFT structure, is such that this channel 12:15
18 protecting layer 215 is not there. And in -- in those 12:15
19 structures, the -- the channel layer 213 is typically 12:15
20 made thicker than the channel layer used in these 12:16
21 channel etched stop structures, where the channel is 12:16
22 protected by 215. 12:16

23 Q And why is it made thicker without the channel 12:16
24 protective layer 215? 12:16

25 A Because in those structures, the -- the etching 12:16

1 process will not stop on the channel protective layer 12:16
2 215 because it's not there. So the etching may 12:16
3 continue, and portions of the undoped amorphous 12:16
4 silicone may be removed from the back side. 12:16

5 And having a thicker amorphous silicone will 12:16
6 ensure that sufficient amorphous silicone remains to 12:17
7 form the channel. 12:17

8 Q I think you said -- is the source, drain metal 12:17
9 directly on top of the N-plus layer? 12:17

10 A That is correct. That's in Figure 4. 12:17

11 Q What layer is on top of the source, drain 12:17
12 electrode metal? 12:17

13 A Layer 241, protective overcoat made of silicone 12:17
14 nitrite. 12:18

15 Q Did you say what the gate dielectric layer was 12:18
16 made of? 12:18

17 A In Column 4, Line 15, it reads, 12:18
18 "A gate dielectric 211 having a 12:18
19 laminated structure of silicon oxide 12:18
20 and silicon nitrite is formed on the 12:18
21 gate electrode." 12:18

22 Q What is the function of protective overcoat 12:19
23 layer 241? 12:19

24 A Protective overcoat layer is to oxidate and 12:19
25 protect the transistor structures and the -- the metal 12:19

1 wiring that we have on the transistor -- on 12:19
2 the -- on the substrate during the subsequent 12:19
3 processing, and also serve as a -- as an extra 12:19
4 insulating layer on -- on top of the devices and the 12:19
5 wiring. 12:20

6 Q Is it the case that the protective layer 12:20
7 overcoat 241 is not confined to the transistor 12:20
8 portion, but is used elsewhere on the display also? 12:20

9 A The protective overcoat layer, when it first 12:20
10 come down, it goes everywhere, and then portions of it 12:20
11 are removed to form openings for contact windows. 12:20
12 Within those openings or contact windows, the 12:20
13 protective overcoat layer is removed, but remains 12:20
14 everywhere else. 12:20

15 And it is shown, for example, in Figure 6 that 12:21
16 the element 241 extends all the way to the edge of the 12:21
17 glass substrate. 12:21

18 Q Does 241 -- sorry. 12:21

19 Does Figure 6 indicate any opening or window, 12:21
20 contact window in protective overcoat layer 241? 12:21

21 Withdraw the question. 12:22

22 Does Figure 4 depict any opening in protective 12:22
23 overcoat layer 241? 12:22

24 A Yes, once it's opening, its label is 243 on the 12:22
25 left of Figure 4. 12:22

1 Q What is located immediately above -- 12:23

2 A Actually, here -- 12:23

3 Q Sorry. Go ahead. 12:23

4 A There's another opening also in Figure 4. It 12:23

5 is the part over the element labeled 731, and 731 is 12:25

6 the power supply bud. 12:25

7 So above the power supply bud you have the 12:26

8 contacting medium. That's the element in 115. It 12:26

9 electrically connects the pad 731 to the counter 12:26

10 electrode. 12:26

11 Q Any other openings in 7 -- I mean, in -- in 12:26

12 protective overcoat 241 in Figure 4? 12:26

13 A In this particular embodiment, it is a crowded 12:27

14 schematic. I cannot detect other ones. Whether may 12:27

15 be, I'm not sure. But... 12:27

16 Q What is immediately above protective overcoat 12:28

17 241 in Figure 4? 12:28

18 A In what part of Figure 4 are you referring? 12:29

19 Q Are there different things over 241 depending 12:29

20 upon where you look? 12:29

21 A It appears so. It also appears that the 12:29

22 different things are above 241 in Figure 6 that we 12:29

23 referred earlier to. 12:29

24 Q What -- various things are over 241, 12:29

25 immediately above 241 in Figure 4. You said there's 12:29

1 more than one different material or component. 12:29

2 What are those components or materials? 12:29

3 A Do you want me to go from one end of the 12:30

4 Figure 4 and go all the way up to the other end of 12:30

5 Figure 4 -- 12:30

6 Q Well, let's start --

7 A -- and try to distinguish the different 12:30

8 elements? 12:30

9 Q Well, if you could, I'd like to know beginning 12:30

10 on the right side of Figure 4. 12:30

11 A "Right" means where you have the transistor? 12:30

12 Q Yes. 12:30

13 A You have some zoom-out picture. It's difficult 12:30

14 to see everything on this. 12:30

15 You prepare some sort an exhibit with -- am I 12:31

16 going to find one with better quality? 12:31

17 Q I would say better. 12:31

18 MR. SCHLITTER: I can mark this. 12:31

19 What's the next number? This will be -- I'll 12:31

20 ask the court reporter to please mark this as 12:31

21 Exhibit 2006. 12:31

22 Exhibit 2006 is an enlarged version of Figure 4 12:31

23 from the Shiba reference. 12:31

24 (Exhibit 2006 was marked for 12:31

25 identification by the court

1 reporter and is attached hereto.) 12:31

2 BY MR. SCHLITTER: 12:31

3 Q Does this help you in being able to identify 12:31

4 what things are immediately above protective overcoat 12:32

5 layer 241? 12:32

6 A Do we have a zoom-out of Figure 6 or just 12:34

7 Figure 4? 12:34

8 Q I do not. 12:34

9 Well, let me -- while you're puzzling about 12:35

10 that... 12:35

11 A Right above the TFT region, I think that's what 12:35

12 you asked me to -- 12:35

13 Q That's where we're starting this. 12:35

14 A I -- I -- I cannot detect any layer between 241 12:35

15 and the horizontal dotted line, which is the liquid 12:35

16 crystal material. I do not see an element labeled to 12:35

17 the left of Figure 4. 12:35

18 Q Do you see element 281? 12:35

19 A I see element 281 in the middle of the figure. 12:35

20 Q To save time on this point, in Column 4, 12:35

21 Lines 32 and 33, do you see that 281 is an orientation 12:35

22 film? 12:36

23 A Yes, I see that. 12:36

24 Q Where do you understand the orientation film to 12:36

25 extend in Figure 4? 12:36

1 A Where it starts and where it stops in Figure 4? 12:36

2 Q Yes.

3 A In this particular cross-section? 12:36

4 Q Yes. 12:36

5 A In this particular cross-section, start -- my 12:36

6 eyes do not play tricks on me, it's -- it's an element 12:36

7 which starts somewhere under the sealant and then -- 12:36

8 Q The sealant is 113, correct? 12:36

9 Sealant agent. 12:37

10 A Yes. 12:37

11 Somewhere below 213, so -- below 113, and then 12:37

12 it -- it is shown in Figure 4 as being terminated 12:37

13 about an inch, in this drawing, to the right of it -- 12:37

14 to the left of it. Or to the right of it. Sorry. 12:37

15 Right -- right above what is written as 12:37

16 No. 251, it shows that that has been terminated there, 12:37

17 in this schematic here. 12:37

18 And if your eyes see differently, please tell 12:37

19 me. That's why I asked you whether you have something 12:38

20 in Figure 6. 12:38

21 Q I don't, but I have something in a spec. 12:38

22 A But in -- in Figure 6, the element that you 12:38

23 refer, 281, it is -- it is shown a little more 12:38

24 clearly, and it is shown that exists on both the 12:38

25 storage capacitor, CJ -- but in Figure 4 it is not 12:38

1 shown there -- and it's shown clearly to be terminated 12:38
2 before the sealing agent, sealing material at 115. 12:38

3 Q Do you -- did you identify 281? Did we? 12:38
4 Is it the orientation film? 12:39

5 A I think we did that. 12:39

6 Q Do you agree that's the orientation film? 12:39

7 A This is what the specifications state. 12:39

8 Q In Column 4, Line 29, there is a sentence that 12:39
9 reads, 12:39
10 "A protective overcoat 241 made of 12:39
11 silicon nitrate is arranged on the TFT 12:39
12 221 and around the pixel electrode 12:39
13 251." 12:39

14 Do you understand that to mean that the 12:39
15 protective overcoat 241 does not overlie pixel 12:39
16 electrode 251 as indicated in Figure 4, which is 12:39
17 consistent with Figure 4; would you agree? 12:39

18 A You say which is consistent with Figure 4? 12:40

19 Q Let me restate the question. 12:40
20 What do you understand that sentence that I 12:40
21 just read about the protective overcoat 241 being 12:40
22 arranged around pixel electrode 251 to mean? 12:40

23 A Well, the plain English meaning of the word 12:41
24 "around" means that it is surrounding the pixel 12:41
25 electrode 251, but it could also mean that it is 12:41

1 around the region where pixel electrode 251 is. So 12:41
2 where pixel electrode 251 is, around there you also 12:41
3 have the protective overcoat 241. 12:41

4 So it is not clear whether there is an opening 12:41
5 in the pixel electrode 251 or whether there is not an 12:41
6 opening of pixel electrode 251. 12:41

7 But as I mentioned in our earlier discussion 12:41
8 previously, it was well-known that if you have a 12:42
9 protective layer above the pixel electrode, to leave 12:42
10 it. It is also well known to create an opening and 12:42
11 remove it. 12:42

12 What the authors and inventors here mean by the 12:42
13 word "around" and in -- in light of the Figures 4 that 12:42
14 I see here, where the pixel electrode is the element 12:42
15 2- -- 251 and the protective overcoat is 241, it is 12:42
16 not clear. Maybe there is an opening, but the opening 12:42
17 is not in the cross-section or the Figure 4 is -- 12:43
18 is -- is shown here because Figure 4 is a 12:43
19 cross-section in the area of the storage capacitor, 12:43
20 and -- and that's -- as I said earlier, that's where 12:43
21 you have a metal below that's formed the CJ storage 12:43
22 electrode layer. That will block the light, and 12:43
23 that's not where you're going to -- be transmissive in 12:43
24 that part. 12:43

25 There may be an -- an -- an opening in the 12:43

1 pixel electrode, but we do not have -- above the pixel 12:43
2 electrode that will -- light would be able to 12:43
3 penetrate through will be unobstructed by the presence 12:43
4 of another metal that will be opaque. 12:43

5 But the others do not provide -- let me see. 12:43

6 Well, the -- the planar section here of the 12:44
7 pixel region, Figure 2, I think lists some of the 12:44
8 elements, but not all the elements. I'm not sure. 12:44

9 Q Looking at Figure 6, would you agree that 12:44
10 orientation film 281 is shown as directly overlying 12:44
11 pixel electrode 251? 12:44

12 A In Figure 6, yes. 12:44

13 But again, this is a portion of -- of the 12:44
14 storage capacitor, but I -- I would agree that 12:44
15 probably they overlie the entire pixel electrodes. 12:44
16 It's a sensor to overlie a pixel electrode. 12:45

17 Q It is -- what did you say? 12:45

18 A "Essential." 12:45

19 Q It is "essential" that it overlie the pixel 12:45
20 electrode? 12:45

21 A Because it's at the -- or -- or -- or alignment 12:45
22 of the liquid crystal. 12:45

23 MR. SCHLITZER: Okay. I'd like to break for 12:45
24 lunch. 12:45

25 THE VIDEO OPERATOR: We are off the record. 12:45

1 The time is 12:45 p.m. on July 12, 2013. 12:45

2 This is the end of Video No. 2 of the 12:45

3 continuing deposition of Dr. Milt Hatalis. 12:45

4 (Lunch recess taken.)

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FRIDAY, JULY 12, 2013; 2:06 p.m.

1

2 THE VIDEO OPERATOR: We are on the record. 02:06

3 Time is 2:06 p.m. on July 12, 2013. 02:07

4 This is the beginning of video three of the 02:07

5 deposition of Dr. Milt Hatalis. 02:07

6 BY MR. SCHLITTER: 02:07

7 Q Do you understand that Figure 6 shows a portion 02:07

8 of the capacitor, the storage capacitor, Exhibit 6 of 02:07

9 Shiba? 02:07

10 A Among other things. 02:07

11 Q Among other things. 02:07

12 So CY refers to an electrode of the capacitor; 02:07

13 is that correct, or CJ? 02:08

14 A Yes, the lower electrode of the storage 02:08

15 capacitor. 02:08

16 Q What are the layers above that electrode CJ? 02:08

17 A I have layer 211. 02:08

18 Q And what layer is that? 02:08

19 A It's the gate dielectric. 02:08

20 Q What is immediately above the gate dielectric 02:08

21 211? 02:09

22 A 251, which is the pixel electrode layer. 02:09

23 Q What is immediately above the pixel electrode 02:09

24 layer? 02:09

25 A In Figure 6 it is labeled 281. 02:09

1 Q Is that the orientation film 281? 02:09

2 A Yes. 02:09

3 Q What is above orientation film 281? 02:09

4 A Liquid crystal. 02:10

5 Q Do you see the label 241 on the right side of 02:10

6 Figure 6 -- 02:10

7 A Yes. 02:10

8 Q -- as a protective overcoat, right? 02:10

9 A Correct. 02:10

10 Q Does protective overcoat 241 extend over in the 02:10

11 area where the capacitor is in Figure 6? 02:10

12 A I cannot distinguish it in Figure 6. I assume 02:10

13 it is not shown in Figure 6. 02:10

14 Q It's shown on the right but not shown on the 02:10

15 left, correct? 02:10

16 A It is not shown on the left which is the 02:11

17 storage capacitor. It is shown on the right under -- 02:11

18 above the wiring 127 and below the 113 -- on the left 02:11

19 of figure -- sorry, the right of Figure 6. That 02:11

20 orientation film 281 stops below the -- well before it 02:11

21 reaches the sealant. 02:11

22 Layer 241 continues past and completely covers 02:11

23 the wiring 127, and it's the one in direct contact 02:11

24 with the sealant 113, and extends also outside the 02:11

25 sealant to the right edge of the substrate 200. 02:12

1 Q Do you see the crosshatching on the layer that 02:12
2 is labeled 281 on the left? 02:12

3 A Yes. 02:12

4 Q So it's a wide crosshatch and a line crosshatch 02:12
5 alternating? 02:12

6 A I believe so. 02:12

7 Q Do you see the same crosshatching to the right 02:13
8 of the transistor? 02:13

9 A It terminates roughly in the area at the bottom 02:13
10 of the number 291. Somewhere above that numbering 291 02:13
11 the 281 terminates. 02:13

12 Q Okay. 02:13

13 A Is that what layer you're referring to? 02:13

14 Q Yes.

15 A Okay. 02:13

16 Q Referring to Figure 3 of Shiba, what do you 02:13
17 understand is designated by 127? 02:13

18 A 127 is the -- 127 is the wiring line that 02:14
19 consists of six narrow lines in this embodiment, and 02:14
20 the six narrow lines are drawn or start from the 02:14
21 element labeled 125a. 02:14

22 And then if we look at Figure 1, that wiring 02:14
23 structure continues along that edge and continues past 02:15
24 the side of the display to other edges. 02:15

25 Q Does 123 extend with reference to Figure 1 on 02:15

1 the left side of Figure 1, that is the left side of 02:15
2 the substrate that is illustrated in Figure 1? 02:16

3 A It's more clearly shown in Figure 3. 02:16

4 Do you want to look at Figure 1 or Figure 3? 02:16

5 You mentioned 123, correct? 02:16

6 Q I meant 127. 02:16

7 A Okay. Can you repeat the question? 02:16

8 Q Line 127, the wiring line marked 127 which you 02:17
9 said comprises six lines, does that extend up along 02:17
10 the left edge of the substrate in Figure 1? 02:17

11 A Yes, and the left edge is labeled 201d. 02:17

12 Q And does it also extend across the top edge of 02:17
13 the substrate? 02:17

14 A Yes, extends along the top along the side 02:17
15 labeled 201b. 02:17

16 Q Do you understand in Figure 3, 4 of the six 02:17
17 narrow lines that you referred to of the wire line 127 02:17
18 are located in a seal region that is marked 111? 02:18

19 A That is correct, in this particular embodiment. 02:18

20 Q The other two narrow lines are located in a 02:18
21 boundary region between the seal region 111 and the 02:18
22 display area 103, correct? 02:18

23 A Correct, in this particular embodiment. There 02:18
24 is another embodiment where the wiring 127 is depicted 02:18
25 having a different structure, and that structure is 02:18

1 shown in Figure 8. 02:18

2 Q We'll come back to that. 02:18

3 What is the structure of figure 127 -- I mean 02:19

4 of wiring line 127, as described in the Shiba patent? 02:19

5 MR. CORDREY: Objection. Form. 02:19

6 MR. SCHLITTER: Let me withdraw that question. 02:20

7 BY MR. SCHLITTER: 02:20

8 Q What is designated by 125a in Figure 3? 02:20

9 A In 125a refers to the interconnecting part. 02:20

10 Q What is referenced by the numbers 123/1 to 02:20

11 123/4? 02:21

12 MR. CORDREY: Just to be clear, which figure 02:21

13 are you referring to now? 02:21

14 MR. SCHLITTER: Figure 1 and Figure 3. 02:21

15 THE WITNESS: The 123/1 is shown in both 02:21

16 Figure 1 and Figure 3, and that is on the left lower 02:21

17 side -- left lower corner of the Figure 1. 02:21

18 And if we look in the zooming portion of 02:21

19 Figure 1, which is surrounded by the dotted line A, 02:22

20 and that portion is shown in magnification and more 02:22

21 detail in Figure 3, we will see that 123/1 is a second 02:22

22 wiring line which is guided across the seal region 02:22

23 111. And that second wiring line is also being 02:22

24 divided into a plurality of narrow lines as it travels 02:22

25 under the sealant. It is divided into narrow lines as 02:22

1 it exits the interconnecting part 125a and continues 02:23
2 as a plurality of narrow lines past the other edge of 02:23
3 the sealant. 02:23
4 By analogy, the 123/4, which is on the 02:23
5 right-hand side of the display, it will be a single 02:23
6 line that will go to another external pad, and they 02:23
7 will connect with part of the wiring that ultimately 02:23
8 terminates into another external connection pad. 02:23
9 Q Is there a 123/2? 02:24
10 A I do not recall if there is a 123/2 and 123/3. 02:24
11 If you have a portion to guide me it will save us 02:26
12 time. 02:26
13 Q We'll call them line 127 and 28 refers to third 02:26
14 wire lines. That is not right. 02:26
15 Line 29, second wiring lines 123/1 to 123/4, 02:26
16 does that suggest to you there are four of those lines 02:26
17 123 since it doesn't say 123/1 and 123/4? 02:26
18 A At face value it suggests that -- one, that 02:27
19 that may be a carryover from the other set of wiring 02:27
20 lines, 121/1 to 121/4 that constitute the third wiring 02:27
21 lines, and those -- there are four of those. The 02:27
22 second one -- 02:27
23 Q How do you know there are four? 02:27
24 A 121/1? 02:27
25 Q Yes, of the -- 02:27

1 A They are shown in Figure 1. There is 121/1, 02:27
2 121/2, 121/3, 121/4 on the lower along the side of the 02:27
3 display. 02:28
4 Q I see it, yes. 02:28
5 A I believe this must have been a typo because 02:28
6 there are two interconnecting parts, 122/5. There is 02:28
7 a 125a and 125b, and 123/1 are originated from 125a on 02:28
8 the left lower corner, and the 123/4 they originated 02:28
9 from the 125b on the right lower corner. 02:28
10 I think the artist may have labeled four in 02:28
11 order to coincide with the 121/4 on that side. So 02:28
12 there is 123/1, 121/1 on the left lower corner and 02:29
13 then the 123/4 and 121/4 to correspond to the right 02:29
14 lower corner. That will be my understanding. 02:29
15 Probably wanted to avoid the confusion by 02:29
16 having 123/2 which may have been confused with 121/2, 02:29
17 but then they replaced this 123 lines. So it's like 02:29
18 having the last one in both 123 and 121. They 02:29
19 probably mean they go to the same pad or same region. 02:29
20 Q What is 121/1? 02:29
21 A You could see what it is in Figure 3. The 02:30
22 121/1 is -- it reads in Column 5, line 50, 57, it 02:30
23 reads, 02:31
24 "The common pad 751 is connected to 02:31
25 the power supply pad 731 through a 02:31

1 Q What is called in the specification as the 02:35
2 second wiring line 123 is divided into five narrow 02:35
3 lines outside the seal region? 02:35

4 A Well, yes. It's not clear here that these -- 02:35
5 if I have to guess 751 is the common pad, and outside 02:35
6 of the pad region where the width of it is wider, I 02:35
7 think that becomes 123. That is why it says it's 02:35
8 drawn from the common pad, so that would be 123 and is 02:36
9 divided into five narrow lines. 02:36

10 I don't know if that is a square, a rectangle 02:36
11 which is undivided, if it's labeled 123 or if it's 02:36
12 labeled 751. 02:36

13 Q 123/1 has a lead line that goes around 02:36
14 something that loops the five narrow lines, correct, 02:36
15 in Figure 3? 02:36

16 A Where 123 terminates to 125, those five narrow 02:36
17 lines are looped and labeled 123/1. 02:36

18 On the other end they go into this rectangle 02:36
19 piece of metal which is not on -- which is not 02:37
20 labeled, and that is part of 751 and part of 123. 02:37

21 Q There is a portion of the specification 02:37
22 Column 6 of Shiba beginning on line 25, that says, "In 02:37
23 the case of TFT of bottom gate type are used as the 02:38
24 switching devices as in the above embodiment." 02:38

25 That is referring to a bottom gate structure 02:38

1 like is shown in Figure 4? 02:38

2 A Correct. 02:38

3 Q The power supply pads 731 to 738 and 731 as 02:38

4 shown in Figure 3, right? 02:38

5 A Correct. 02:38

6 Q And all four of them are shown in Figure 1? 02:38

7 A I believe, or eight are shown in Figure 1 -- 02:38

8 four of the -- along the side, along the lower end of 02:38

9 Figure 1 and 4 along the long side on the top edge of 02:38

10 Figure 1. 02:38

11 Q Correct. And the common pad 751, the third 02:38

12 wiring lines 121/1 to 121/4, the interconnecting pad 02:39

13 125a and 125b, so 125a is shown in Figure 3 and 125b 02:39

14 is shown in Figure 1, correct? 02:39

15 A Yes. 02:39

16 Q "Second wiring lines 123/1 to 123/4, and the 02:39

17 first wiring line 127 can be formed in the same step 02:39

18 by forming the data lines X." 02:40

19 Do you understand that sentence to mean that 02:40

20 all of those components are formed from the same metal 02:40

21 layer as the data lines? 02:40

22 A Well, all these different elements are made of 02:40

23 the same material. 02:40

24 Q They're formed from the same step as from the 02:40

25 data lines so they would have the same material? 02:40

1 A After patterning and performing the 18 steps 02:42
2 they overlie. How the edges would look like depends 02:42
3 upon the etching process. Sometimes you have a 02:43
4 tapered edge. Sometimes you have a vertical edge. 02:43
5 Sometimes you have like a stepwise edge. 02:43
6 So they will overlap in the middle of a line. 02:43
7 But how they overlap on the edges of the line, that 02:43
8 depends upon how the etching was performed. For 02:43
9 example, you may have the lower layer to be wider than 02:43
10 the upper layer. 02:43
11 Q But there is no intervening insulating layer 02:43
12 within that multi-layer structure, is there? 02:43
13 A In forming the data lines? 02:43
14 Q Yes.
15 A No. But one of those elements, another portion 02:44
16 below it could be made in another way. 02:44
17 Q I haven't gotten there yet though. 02:44
18 A Okay. 02:45
19 Q What is the purpose of dividing wiring line 127 02:45
20 into a plurality of narrow lines? 02:45
21 A It serves to increase the surface area, because 02:45
22 now we have the top as well as the edges that will 02:45
23 make contact with the sealant. 02:45
24 And also they serve as some sort of barrier for 02:45
25 the sealant to prevent the flow of the sealant, as the 02:46

1 sealant is like a viscous material before it is cured. 02:46
2 This prevents that from expanding into the display 02:46
3 area. 02:46
4 It is a discussion in the text on the 02:46
5 specifications by that one. We can refer to it for a 02:46
6 more accurate description. 02:46
7 Q Where would you reference? 02:46
8 A So if we look at the Column 6 -- not in 02:46
9 Column 6. Hold on a second. 02:47
10 Q How about Column 7? 02:47
11 A Yes. 02:48
12 Q Line 39, is that what you're referring to? 02:48
13 A Yes. 02:48
14 Q What is this? "The advantage of increasing the 02:48
15 effect of adhesion area can be obtained," and that is 02:48
16 as a result of the narrow lines, 127, being divided 02:48
17 into several narrow lines? 02:48
18 A Correct. It's part of the adhesion between 02:48
19 the -- between the adhesive and the ending protective 02:48
20 overcoat in the gate dielectric so that the -- in this 02:49
21 case we want to have a good adhesion to the -- to the 02:49
22 substrate. So 127 is a variety of a narrow lines. 02:49
23 Q Does that increase the surface area available 02:49
24 to interface with the sealant? 02:49
25 A One second please. 02:50

1 As you have the 127 divided into a set of 02:50
2 lines, the protective overcoat 241 in the gaps between 02:50
3 the metal wiring lines is touching and makes a better 02:50
4 bond with the gate dielectric to a level. There are 02:50
5 22 layers, maybe both oxides or maybe both nitrite, so 02:50
6 the sealant material -- so the adhesion of the 241 to 02:51
7 the gate dielectric is the one that becomes more 02:51
8 effective as we are dividing the narrow 127 into 02:51
9 plurality of lines. 02:51

10 So the one you have to remove, the sealing 02:51
11 agent we do the protective overcoat, and along that 02:51
12 are the wiring lines 127. 02:51

13 Q When do you have to remove the sealing agent? 02:51

14 A In the process of forming the display is an 02:51
15 alignment that is between the two counter substrates, 02:52
16 and one has the colored filters, the red, blue, and 02:52
17 one has the pixel electrodes. So the colored filters 02:52
18 have to be aligned with respect to the right subpixel 02:52
19 below. 02:52

20 I'm just reading whatever it says here. 02:52

21 Q Where are you reading? 02:52

22 A On Column 7, on line 49 or 50, it says, 02:52
23 "As a result the risk of removal of 02:52
24 the first wiring line 127, together 02:52
25 with the sealing agent 113, is 02:52

1 reduced. Correspondingly, the degree 02:52
2 of freedom of selecting material of 02:52
3 the sealant agent 113 depends on the 02:52
4 adhesion device that can be 02:53
5 increased." 02:53

6 Q But that doesn't say anything about having to 02:53
7 remove it, does it? Isn't that just referring to the 02:53
8 integrity of the seal? 02:53

9 A The first says, "As a result the risk of 02:53
10 removing of the first wiring line 127 together with 02:53
11 the sealing agent, 113 is reduced." 02:53

12 Here it implies the sealing agent may have to 02:53
13 be removed. 02:53

14 Q How does it imply that? The word "risk" 02:53
15 implies something that you would intentionally do? 02:53

16 Is that your opinion? 02:54

17 A The risk of removing first one in line in the 02:54
18 event of a sealing agent that has to be removed. 02:54

19 Q Where does it say that? 02:54

20 A I'm reading the same sentence as you. 02:54

21 Q I don't see "in the event." 02:54

22 A How you interpret the sentence? Maybe you can 02:54
23 provide me an alternative. 02:54

24 Q Let me ask a different question. 02:54
25 How does -- well, does the use of the plurality 02:54

1 of narrow lines for 127 allow the width of the sealant 02:55
2 region to be reduced? 02:55

3 A Well, if we look further down the same column, 02:55
4 we are on Column 7, and we look at the line 55, that 02:55
5 is the element labeled D, and it reads, 02:55

6 "Since part of the first wiring line 02:55
7 127 is arranged in the battery region 02:55
8 between the seal region 111 and the 02:55
9 display area 103, Figure 3, the 02:55
10 sealing agent 113 is prevented from 02:56
11 flowing toward the display area 103. 02:56
12 As a result the width of the bundled 02:56
13 portion between the seal region 111 02:56
14 and the display area 103 can be small, 02:56
15 thereby reducing the outside dimension 02:56
16 of the LCD panel 100." 02:56

17 Q Looking at Line 42, beginning line 42 in 02:56
18 Column 7, there is a sentence that states, 02:56
19 "However, if at least three narrow 02:56
20 lines of the first wiring line are 02:56
21 arranged in the seal region 111, the 02:56
22 advantage of increasing the effective 02:56
23 adhesion area can be obtained." 02:56
24 What does that sentence mean to you? 02:56

25 A If you divide 127 with the plurality of small 02:56

1 lines and three of those lines are in the seal region 02:57
2 in between the metal lines, the adhesive that is used 02:57
3 to provide the bonding material through substrate will 02:57
4 bond to 241. 02:57

5 And then 241 is the portion that we read a 02:57
6 moment ago indicated will be right on top of the gate 02:57
7 dielectric 211. So the area where the adhesive will 02:58
8 be bonded to the protective overcoat and the 02:58
9 protective overcoat will be bonded to the gate 02:58
10 dielectric. It will increase the surface area. Where 02:58
11 the protective overcoat is touching the gate 205 to 02:58
12 211, will increase. 02:58

13 Q You think this patent is about increasing 02:58
14 adhesion between the protective overcoat 241 and the 02:58
15 gate 205, 211? Is that your opinion? 02:58

16 A This has a relevance to my answer. The 02:58
17 strength of the adhesion is very relevant. 02:59

18 There is a very strong adhesive. You can 02:59
19 narrow down its effective width. You don't need to 02:59
20 use as much of it. If you use a weaker adhesive, then 02:59
21 you have to have a wider region to put the adhesive 02:59
22 down. 02:59

23 Is that clear? 02:59

24 Q Sure. 02:59

25 A Now, if you have a strong adhesive, and that is 02:59

1 bonded on to 241, and 241 is bonded to 127, if you 02:59
2 have to remove it, 241 is not as strongly bonded on 03:00
3 127 as it is if it is bonded in contact with the gate 03:00
4 dielectric 211. 03:00

5 Q When you have to remove the wiring 127 from the 03:00
6 protective overcoat, when does that happen? 03:00

7 A You don't have to remove the wiring 127. You 03:00
8 may have to rework the sealing process. 03:00

9 Q Where does it say that in this patent? 03:00

10 A This is the sentence that we've -- we were 03:00
11 discussing a moment ago. 03:00

12 Q How about risk of removal? Do you think that 03:00
13 is about rework? 03:00

14 A As a result the risk of removal of the first 03:00
15 wiring line 127, together with the sealing agent 113 03:00
16 is reduced according to the degree of freedom of 03:01
17 selecting the material -- capacity can be increased. 03:01
18 It means you can have a stronger sealing agent 113. 03:01
19 One has a better adhesion, and so you can make it a 03:01
20 narrow width. If you have to pull it out you don't 03:01
21 have to -- 03:01

22 Q What are you talking about? When do you have 03:01
23 to pull it out? 03:01

24 A This is what I was trying to explain earlier. 03:01
25 You have the two substrates, and the two 03:01

1 substrates are in close contact, and you have to align 03:01
2 the one substrate with respect to the other substrate 03:01
3 so the colored filters are in the right position. You 03:01
4 don't want the colored filter to be overlapping two 03:01
5 pixel electrodes. 03:02

6 So there is some fine motion that you have to 03:02
7 do to bring the two substrates, and at some point the 03:02
8 two substrates will become so close that you'll be 03:02
9 pressing against the adhesive. And if the alignment 03:02
10 is not correct then you have to pull one substrate in 03:02
11 order to reposition it, then you run into this 03:02
12 problem. 03:02

13 Q Have you seen that problem in manufacturing 03:02
14 processes firsthand? 03:02

15 A I have seen the finished products, and I have 03:02
16 took apart finished displays and I became aware of the 03:02
17 intricacies of all the important elements there, the 03:03
18 adhesive, the sealing, and I get an appreciation of 03:03
19 the complexity involved in creating these displays. 03:03

20 Did I work in manufacturing? You've seen my 03:03
21 resume'. 03:03

22 Q I didn't ask that. I asked if you'd ever 03:03
23 become aware of a situation during a manufacturing 03:03
24 setting where substrates were brought together and 03:03
25 then peeled apart and then restuck together again? 03:03

1 A In the context of another patent that we were 03:04
2 discussing, for example the Sukigawa that referred to 03:04
3 the process of attaching the external connection, it's 03:04
4 a similar situation. 03:04

5 Q That was talking about attaching a flexible 03:04
6 circuit, not the substrates. 03:04

7 A It's a similar issue. 03:04

8 Q There is nothing in Shiba about the substrates 03:04
9 being put together and then pulled apart again, is 03:05
10 there? 03:05

11 A You asked your questions about substrates. In 03:05
12 that case the flexible connectors would be substrate. 03:05
13 The glass substrate is another substrate. There are a 03:05
14 set of -- 03:05

15 Q I'll rephrase. 03:05
16 There is nothing in Shiba about the color 03:05
17 filter substrate and the thin-film transistor 03:05
18 substrate being brought together and then pulled apart 03:05
19 and repositioned together again, is there? 03:05

20 A That is not addressing the -- how the colored 03:05
21 filter and the glass substrates are bonded together. 03:05
22 It's addressing the substrate that has the flexible 03:05
23 connector that is attaching the glass substrate, and 03:05
24 the turns out that you may have to rework that 03:06
25 connection. 03:06

1 In pulling one substrate, a flexible substrate 03:06
2 that has the external wiring, you may pull the 03:06
3 metallization and you may damage the pads. So it's a 03:06
4 very similar issue here. 03:06

5 Q Except that what is described in Shiba has 03:06
6 nothing to do with the color filter substrate and a 03:06
7 thin-film transistor substrate, does it? It's about 03:06
8 the FPC. 03:06

9 A Your question earlier, it reads, "I asked if 03:06
10 you'd ever become aware of the situation during the 03:06
11 manufacturing setting where substrates were brought 03:07
12 together then peeled apart and then re-stuck together 03:07
13 again." This is what you asked me. 03:07

14 I told you I did not work in manufacturing 03:07
15 or -- and you asked me -- then I said that I became 03:07
16 familiar with this issue of bringing two substrates 03:07
17 together in the case of Shiba where you have a similar 03:07
18 issue. You have two substrates. You have to align 03:07
19 one with respect to the other, and then you have an 03:07
20 adhesive in between. 03:07

21 Only difference in Shiba is the adhesive is 03:07
22 conductive, and in this case the adhesive is not 03:07
23 conductive. 03:07

24 Q I take that as a "no". 03:07
25 Looking at Column 7, beginning at Line 21 it 03:08

1 reads, 03:08

2 "Since the first wiring line 127 is 03:08

3 arranged in the seal region 111, while

4 the other are arranged in the boundary

5 portion between the seal region 111 is 03:08

6 constituted by a plurality of neural 03:08

7 lines, the effective adhesion area 03:08

8 between the sealing agent 113 and the 03:08

9 array substrate 200 is relatively 03:08

10 large. For this reason the width of 03:08

11 the seal region 111 can be reduced 03:08

12 without a risk of removal of the 03:08

13 sealing agent 113 from the array 03:08

14 substrate 200." 03:08

15 Do you understand that to be talking about the 03:08

16 adhesion between the sealing agent and the substrate 03:08

17 200? 03:08

18 A Excuse me. Where are you reading? 03:09

19 Q Column 7 beginning at Line -- I misspoke, 31, 03:09

20 beginning at Line 31. 03:09

21 A I see that. That refers to another problem. I 03:11

22 think the substrates have to be broken and diced, 03:11

23 separated. 03:11

24 So if you make a narrow seal which is strongly 03:11

25 adhered with the array substrate 200, when you're 03:11

1 breaking the substrate. You're not removing the seal 03:11
2 when you're separating the substrate. I think that is 03:11
3 what I'm understanding from this part. If you 03:11
4 understand something different, please tell me. 03:12
5 It's all those things. If you have a narrow -- 03:12
6 the plurality of narrow lines, the area where the 03:12
7 sealing agent 113 is touching the protective overcoat 03:12
8 241 and the protective overcoat is attached with the 03:12
9 gate dielectric 211 is increased. That is where you 03:12
10 have a strong bond. 03:12
11 Q Do you think that the surface area between gate 03:12
12 dielectric 211 and protective overcoat 241 is 03:12
13 increased when there are the plurality of narrow lines 03:13
14 separating protective overcoat 241 from gate 03:13
15 dielectric 211 compared to those narrow lines being 03:13
16 absent? 03:13
17 A Well, instead of -- if you're having six narrow 03:13
18 lines, some of them are inside the sealing region and 03:13
19 some outside, we have one continuous wide line -- and 03:14
20 that is all inside the sealing area, sealing region -- 03:14
21 then the protective overcoat 241 above the wiring 127 03:14
22 is separated from the 211. They're not directly 03:14
23 connected. 03:14
24 In lines 45 to 50 this is what it states. It 03:14
25 states, 03:14

1 "Since the first wiring line 127 is 03:14
2 constituted by a plurality of narrow 03:15
3 lines as shown in Figure 6, the 03:15
4 protective overcoat 241 and the gate 03:15
5 dielectric 211 are directly connected 03:15
6 to each other through the gap between 03:15
7 the narrow lines." 03:15
8 Continuing, it reads, "As a result, 03:15
9 the risk of removal of the first 03:15
10 wiring line 127, together with the 03:15
11 sealing agent 113 is reduced. 03:15
12 Accordingly, the degree of freedom of 03:15
13 selecting material of the sealing 03:15
14 agent 113 to bonding adhesion capacity 03:15
15 can be increased." 03:15
16 Q Look at Column 2. 03:15
17 "If the width of a seal region is 03:16
18 reduced the strength of adhesion 03:16
19 between the array substrate and the 03:16
20 counter substrate is lowered." 03:16
21 Do you see that? 03:16
22 A Yes. 03:16
23 Q So it says, 03:16
24 "This causes various problems. For 03:16
25 example, removal of the sealing agent 03:16

1 be formed in the same step of forming 03:21

2 the scanning lines Y sub J." 03:21

3 Do you understand that to mean that if instead 03:21

4 of a bottom gate type TFT, top gate type TFTs were 03:21

5 used, then in that case those various lines and 03:21

6 components could be formed in the same step of forming 03:21

7 the scanning lines Y sub J? 03:21

8 A It is -- someone skilled in the art will see 03:22

9 that these wiring lines may not bend by the type of 03:23

10 the TFTs, because I don't see how even if you have a 03:23

11 bottom gate TFTs, that you cannot use that one using 03:23

12 the scanning lines, and that the wiring lines can be 03:23

13 made using the material from the scanning lines only 03:23

14 in the case of as you put it of top gate TFTs. 03:23

15 Q That's what I'm saying is just what is in the 03:23

16 patent, what it teaches, and it says, "Depending on 03:24

17 the kind of TFTs." 03:24

18 So in the first part of the paragraph it talks 03:24

19 about bottom gate type TFTs, and then describes if you 03:24

20 use those you can make all the components out of the 03:24

21 data line material. 03:24

22 Then it says, 03:24

23 "Further, depending on the kind of the 03:24

24 TFTs, the aforementioned wiring lines 03:24

25 can be formed in the same step of 03:24

1 forming the scanning lines." 03:24

2 Doesn't that mean another alternative is to 03:24

3 form all those components from the same layer as the 03:24

4 scanning lines are formed from? That is what this 03:24

5 says, would you agree? 03:24

6 A Well, what someone skilled in the art will 03:24

7 understand by this term -- depending on the kind of 03:24

8 the TFTs -- is what material is used to form the 03:24

9 scanning lines? 03:25

10 To form all those elements that we're 03:25

11 discussing above, all those wiring line elements, and 03:25

12 the supply pads, the power supply pads, common pad, 03:25

13 third wiring lines, second wiring lines and first 03:25

14 wiring lines, you need to have a high conductivity 03:25

15 material. You need to have a layer of -- made out of 03:25

16 a material that is very conductive, that will not be 03:25

17 resistive. 03:25

18 In the bottom gate TFT structure, which is used 03:25

19 here the data line material is taken as a fact that it 03:25

20 is a high conductivity material. 03:26

21 If you use a bottom gate device and the 03:26

22 material that is used to make the scanning lines also 03:26

23 is made of a high conductivity metal, that bottom 03:26

24 gate -- that -- sorry. 03:26

25 If it's a bottom gate TFT, it is implied that 03:26

1 the material used to form the data lines it will be 03:26
2 high conductivity, correct? There is no disagreement 03:26
3 with that part. 03:26

4 So this structure applies to that question if 03:26
5 you have the data line material in the bottom gate 03:27
6 TFT, that is given it is a high conductivity material. 03:27

7 The question is when one can use the scanning 03:27
8 line material to form that wiring line? You said in 03:27
9 your question that the structure bottom gate versus 03:27
10 top gate is determining factor, and I responded. 03:27

11 And I'm stating again that it's not the 03:27
12 structure top versus bottom, but it is the material 03:27
13 that is used to form the scanning line itself. If 03:27
14 that material is a high conductivity material, that 03:27
15 material can be used to make the wiring -- all these 03:27
16 wiring elements. If that material is low conductivity 03:28
17 or high resistivity, using the scanning line -- the 03:28
18 material of the scanning lines for the wiring 03:28
19 elements, it will not be effective because you will 03:28
20 add serious resistance. 03:28

21 For example, you mentioned the top gate device, 03:28
22 and one material in the top gate device is like 03:28
23 polycrystalline silicone, highly-doped silicone. That 03:28
24 will be the resistive material that will not be 03:28
25 useful. 03:28

1 If you have an aluminum gate device it doesn't 03:28
2 matter if it's a top or bottom gate, you can use it to 03:28
3 form that wiring structure. You will have a 03:28
4 refractory metal that is about enough -- about 03:28
5 activity, that will be good. 03:29

6 Q A what metal? 03:29

7 A "Refractory" metal. 03:29

8 Q "Refractory" did you say? 03:29

9 A Yes. Some of the gates used to be made with 03:29
10 aluminum, so aluminum has much higher conductivity 03:29
11 than the doped polycrystalline silicone used as the 03:29
12 gate of the top gate TFTs. 03:29

13 Q Would the polycrystalline silicone also be used 03:29
14 for the scanning lines in that situation? 03:29

15 A If it's a small-sized display. 03:29

16 Q Regardless of the kinds of transistors, this 03:29
17 sentence says, "Depending on the kind of TFT, there is 03:30
18 some kind of TFTs where the aforementioned wire lines 03:30
19 can be formed in the same step performing the scanning 03:30
20 lines," right? 03:30

21 A Okay. 03:30

22 Q Do you agree? 03:30

23 A Well, this is what the sentence says. You're 03:30
24 implying that it is the structure of the TFT that 03:30
25 dictates where you can use or cannot use the scanning 03:30

1 line, and you tried to imply that -- 03:30

2 Q I'm not implying that. 03:30

3 I said in my question, regardless of the kind 03:30

4 of transistor the sentence says there is some kind of 03:30

5 transistors depending upon the kind, it says, for you 03:30

6 to form the aforementioned wire lines all from the 03:30

7 same step of performing the scanning lines. 03:30

8 If you do that, all of the aforementioned 03:30

9 wiring lines would be formed over one layer and would 03:31

10 have the same makeup as the scanning lines, right, 03:31

11 just looking at this sentence? 03:31

12 A Okay. This sentence says it is possible to 03:31

13 form those lines out of a scanning line element. 03:31

14 Q In which case they all have the same material, 03:31

15 and they're all one layer, or if it's a multi-layer 03:32

16 scanning line they'd have the same composition as the 03:32

17 scanning line, correct? 03:32

18 A All but one segment. 03:32

19 Q What do you mean? I don't see that. 03:32

20 A Yeah. Someone skilled in the art would see. 03:32

21 With all respect, you're an attorney, not 03:32

22 skilled in the art in these matters. I'm sure, again, 03:32

23 in these proceedings you'll be very skilled. 03:32

24 But if you read the section in Column 6 03:32

25 starting from line 7, it says, 03:32

1 "As shown in Figure 1, the first 03:32
2 wiring line 127 is guided along a 03:32
3 second circuit side 201d to the second 03:32
4 longer side 201b and connected to the 03:32
5 power supply pad 735 to 738 through a 03:33
6 branch wiring line. Then the first 03:33
7 wiring line 127 is guided along the 03:33
8 first side 201c to the first longer 03:33
9 side 201a, and the narrow lines meet 03:33
10 together at the inner connecting pad 03:33
11 125b." 03:33
12 In the same column, line -- 03:33
13 Q Let's stop. Let's stop. 03:33
14 A Let me conclude this part here, because what 03:33
15 I'm going to read is the conclusion of that part. 03:33
16 In the above amount the first wiring line 127 03:33
17 is arranged the seal region. 03:33
18 Q Where are you looking? 03:34
19 A Same Column 6, line 48. 03:34
20 "The first wiring line 127 is arranged 03:34
21 along the seal region 111 on the three 03:34
22 sides, 201b, 201c and 201d of the 03:34
23 array substrate." 03:34
24 Q Do you understand that to mean the wiring line 03:34
25 127 goes along three sides of the substrate? 03:34

1 A This is what it says here. 03:34

2 Q Not four sides? 03:34

3 A But it's source with specific sides. 03:34

4 Q Right. Which sides are those that are shown? 03:34

5 A The 201b which is the top along the side, the 03:34

6 201c and 201d, those are the two short sides. 03:34

7 Q That is where the wiring 127 goes along those 03:35

8 three sides? 03:35

9 A Correct. And if you make 127 with the scanning 03:35

10 line material, the line that goes -- the second of the 03:35

11 line that goes along the side 201c, it cannot be made 03:35

12 with the scanning line material because that segment 03:35

13 will shorten all the scanning lines that will come 03:35

14 from those external connections 721, 722, 723 and 224. 03:35

15 Q 201c is the short side, on the right? 03:35

16 A Correct. 03:35

17 Q But if you had a bottom gate transistor the 03:35

18 scan lines are going to be in the gate line layer. 03:35

19 They're going to be on the bottom layer of the 03:36

20 transistor, correct? 03:36

21 A It doesn't matter if it's a bottom gate or a 03:36

22 top gate transistor. If you make a wiring that is 03:36

23 made in the same material as the scanning lines, you 03:36

24 cannot have that wiring be in the same place where 03:36

25 there is scanning lines that will be crossing. 03:36

1 You see that wiring 127 goes around, and it 03:36
2 stops at 125b. That side 201c may have like a 03:36
3 thousand scanning lines going across that segment, as 03:36
4 I said, there is -- will have to be a different 03:36
5 material. And the other material of choice, it is the 03:36
6 data line material. 03:36
7 So this embodiment says it is possible to make 03:37
8 it with the scanning line material, but in that case 03:37
9 it will be on two sides. The third side will still 03:37
10 have to be the data line material to avoid the 03:37
11 shorting with the scanning lines. That is what 03:37
12 someone skilled in the art will see. 03:37
13 MR. SCHLITTER: Okay. Let's take a break. 03:37
14 THE VIDEO OPERATOR: We are off the record. 03:37
15 The time is 3:37 p.m. on July 12, 2013. This is the 03:37
16 end of video No. 1 of the continuing deposition of 03:37
17 Dr. Milt Hatalis. 03:38
18 (Recess taken.) 03:38
19 THE VIDEO OPERATOR: We are on the record. The 03:53
20 time is 3:53 p.m. on July 12, 2013, in this is the 03:53
21 beginning of video four of the deposition of 03:53
22 Dr. Milt Hatalis. 03:54
23 BY MR. SCHLITTER: 03:54
24 Q Before the break we were talking about the two 03:54
25 cases that are described in Column 6, one where 03:54

1 various wire lines described in lines 25 through 31 03:54
2 are formed from the same step as formed from the data 03:54
3 lines, and the other case where the wiring lines are 03:54
4 formed in the same step as formed in the scanning 03:54
5 lines. 03:54

6 In the case of those wiring lines being formed 03:54
7 from the same step as the data lines, I take it all 03:54
8 three sides of wiring line 127, that is 201d, 201b, or 03:54
9 the sides along 201b, d and c, all could be at the 03:54
10 data line level, right? 03:55

11 It wouldn't interfere with the data lines 03:55
12 driven by the circuits on the bottom side of the 03:55
13 substrate shown on Figure 1, correct? 03:55

14 A Correct. 03:55

15 Q And then you were suggesting on the other hand 03:55
16 if instead of forming all the wire lines from the data 03:55
17 lines they were formed from the scanning lines, then 03:55
18 in that case you would need to make a different line 03:55
19 segment for wiring line 127 along the side 201c in 03:55
20 order to not short out the scan lines? Am I recalling 03:55
21 your testimony correctly? 03:55

22 A Correct. 03:56

23 Q Alternatively, if you just interchange the 03:56
24 driving circuits in Figure 1 so you put the data line 03:56
25 circuits alongside 201c, and the scan line circuits 03:56

1 along line or side 201a -- if I have that right -- 03:56
2 which is the bottom side, in that case you would also 03:56
3 be able to have all three sides of line 127 be on the 03:56
4 scanning line level without interfering or shorting 03:56
5 out the scan lines, correct? 03:56
6 A You could do that if one interchanges the 03:57
7 circuit. But now you are going to have the long -- 03:57
8 when you do that you will increase the length of your 03:57
9 data lines. The data lines now will run along the 03:58
10 long side of the display, not along the short side of 03:58
11 the display. 03:58
12 So you cannot just simply say it's a simple 03:58
13 change from one case to take into consideration what 03:58
14 effect will that have on the display performance. 03:58
15 But, hypothetically speaking, if one was able 03:58
16 to do that, and where are the scan lines and where are 03:58
17 the data lines, that would be correct. 03:58
18 Q Your opinion is the structure that corresponds 03:59
19 to a first internal conducting line referenced in the 03:59
20 claims of the '102 Patent, for example Claim 15? 03:59
21 A I don't understand your question. 04:00
22 Q Referencing Claim 15 of the '102 Patent, there 04:00
23 is an element that calls for, 04:00
24 "First internal conducting line 04:00
25 electrically connected to the common 04:00

1 terminal in the contact hole, wherein 04:00
2 the first internal conducting line and 04:00
3 a gate electrode of the thin-film 04:00
4 transistor are created by first 04:00
5 processing step." 04:00
6 In your -- is there a structure in the Shiba 04:00
7 reference that corresponds to this Claim element? 04:00
8 A Yes. 04:00
9 Q Where is that structure? What structure are 04:01
10 you referring to? 04:01
11 A Indicating to the first wiring line 127. And I 04:01
12 want to point out another way to get Shiba teaching. 04:01
13 Q Let me break down the question a bit more. 04:01
14 A Sure. 04:02
15 Q Where is wiring line 127, in your opinion, if 04:02
16 it is connected to a common terminal in Shiba? 04:02
17 A Well, the common terminal, according to the 04:02
18 specifications, according to the Claim, is the 04:03
19 conductive element which is located in the extractor 04:03
20 terminal. And there is a contact hole in the 04:03
21 extractor terminal, and according to the limitation 04:03
22 Claim 15 that reads, 04:03
23 "An extractor terminal including a 04:03
24 common terminal and a contact hole 04:03
25 formed over the substrate wherein the 04:03

1 common terminal is formed from the 04:03
2 same layers that pixel dielectric." 04:03
3 So in this section the description of the 04:04
4 common terminal is provided. It is a conductive 04:04
5 layer. It is located in the extractor terminal 04:04
6 region, and there is a hole in that region, and the 04:04
7 whole is space violator. 04:04
8 And in this section here it also provides 04:04
9 limitation on what is the material that the conductive 04:04
10 layer is made of, and specifically he says this is 04:04
11 formed from the same layer as the pixel electrode. 04:04
12 Now, Shiba discloses a conductive layer in the 04:04
13 extractor terminal. 04:05
14 Q Where is the extractor terminal in Shiba? 04:05
15 A The extractor terminal in Shiba is located 04:05
16 along the sides 201a and sides 201c. 04:05
17 Q Mark that as the next exhibit, 2007. 04:05
18 (Exhibit 2007 was marked for 04:05
19 identification by the court
20 reporter and is attached hereto.) 04:05
21 BY MR. SCHLITTER: 04:05
22 Q Is an extractor terminal shown in Figure 3 -- 04:06
23 I've handed you what is marked as Exhibit 2007, which 04:06
24 is an enlargement of Figure 3 from Shiba. 04:06
25 Do you recognize that? 04:06

1 And in Figure 12 in the prior art I -- 04:12

2 Q Are you looking at Column 1 from -- 04:12

3 A 102. 04:12

4 Q You said line 53? I see it. Okay. 04:12

5 A So the extractor terminal 15, and in Figure 12 04:12

6 in the prior art it shows like a dotted line labeled 04:12

7 15, and within that dotted line there are many 04:12

8 extractor terminals. 04:12

9 Q Are extractor terminals also shown in Figure 3 04:13

10 which is not prior art in the '102 Patent? We talked 04:13

11 about those this morning labeled 205. I think I'm in 04:13

12 the column I referred to. 04:13

13 A So the bottom of Column 7, line 61 reads, 04:13

14 "Extractor terminals 205 are also 04:13

15 provided to supply electric power and 04:14

16 control signals from the outside. A 04:14

17 plurality of extractor terminals are 04:14

18 shown in the dotted line that 04:14

19 surrounds them in Figure 3." 04:14

20 So by analogy I can draw a circle in one of 04:14

21 them or in many of them. You asked me to draw -- you 04:14

22 asked me as a singular, if I understand. 04:14

23 Q I will clarify the question. 04:14

24 Circle in front of you everything that you 04:14

25 think in your opinion you believe to be an extractor 04:14

1 terminal or part of the extractor terminal, or 04:14
2 terminals. 04:15

3 A Let me go one -- 04:15

4 Q Everything in Figure 3 that is an extractor 04:15
5 terminal I would like you to circle. 04:15

6 A Well, an analogy of Figure 3 and the Figure 12 04:15
7 which defines what are the extractor terminals. I 04:15
8 will draw a circle in Figure 12 -- sorry in Figure 3. 04:15

9 Is that what you asked me? 04:15

10 Q Yeah. Could you label that "extractor 04:15
11 terminals" what you just circled, please? 04:16

12 A Do you want me to write the words "extractor 04:16
13 terminals"?. 04:16

14 Q Yes, please. 04:17

15 A So I draw a rectangle around the area where the 04:17
16 extractor terminals are included within. 04:17

17 Q Is that the only part of Figure 3 that you deem 04:17
18 to be an extractor terminal? 04:17

19 A In Figure 3. 04:17

20 Q Okay. Claim element we read a moment ago 04:17
21 refers to, "First internal conducting line 04:18
22 electrically connected to the common terminal." 04:18

23 Is there a common terminal shown in Figure 3 or 04:18
24 is there structure in Figure 3 that you believe 04:18
25 corresponds to the common terminal recited in the 04:18

1 element of Claim 15? 04:18

2 A Well, the extractor terminal in the 04:18

3 specifications indicated is the region where 04:18

4 connections with the external wiring takes place, and 04:18

5 in these connections you have a conductive element in 04:18

6 the substrate. 04:19

7 And in the specifications they list different 04:19

8 materials that is used to make the pixel electrode, 04:19

9 and that material is also present in the extractor 04:19

10 terminal region, and -- 04:19

11 Q You're talking about the '102 Patent 04:19

12 specification now? 04:19

13 A Right. The Claim has a limitation in the 04:19

14 extractor terminal in which the material that can be 04:19

15 used to make the common terminal is restricted to the 04:19

16 material that is used to make the pixel electrode. 04:20

17 In Shiba what we referred to here as a common 04:20

18 terminal in the particular embodiment depicted in 04:20

19 Figure 3 and discussed in the specifications, the 04:20

20 particular embodiment is not made from the same layer 04:20

21 as the pixel electrode. There is another material 04:20

22 used in the extractor terminal to form the connection 04:20

23 with the external circuit. 04:20

24 Q So are you saying that Shiba does not disclose 04:20

25 structure that corresponds to the common terminal 04:20

1 recited in Claim 15? 04:21

2 MR. CORDREY: Objection. Form. 04:21

3 THE WITNESS: The particular embodiment 04:21

4 disclosed by Shiba meets many of the limitations 04:21

5 imposed by the Claim 15, such as the presence of an 04:21

6 extractor terminal, such as the presence of a contact 04:21

7 hole. 04:21

8 But the particular embodiment -- in this 04:21

9 particular embodiment of Shiba the common area is made 04:21

10 from a different material. There is teaching within 04:21

11 Shiba that could lead someone skilled in the art to 04:21

12 modify the -- this particular embodiment, and make 04:22

13 751 -- make the common terminal in an alternative 04:22

14 way, and in that case it will meet all the limitations 04:22

15 of Claim 15. 04:22

16 BY MR. SCHLITTER: 04:22

17 Q Are you saying that there is structure in 04:22

18 Figure 3 of Shiba that you believe corresponds to the 04:22

19 common terminal, except it's made from a different 04:22

20 material than is required by Claim 15? Is that what 04:22

21 you're saying? 04:23

22 A As we discussed earlier in the context of 1 or 04:23

23 2, the extractor terminal is a multi-layer structure, 04:23

24 has a lower level metal and an upper layer metal. The 04:23

25 upper layer metal is made of the pixel electrode 04:23

1 material, and that -- and it is the upper layer metal 04:23
2 that 102 refers as the common terminal. 04:23

3 Shiba in this particular embodiment which is 04:23
4 described in Figure 3, you have the lower level metal. 04:23
5 You have the contact hole, but this particular 04:24
6 embodiment does not show the upper layer material. 04:24

7 Q You said in your answer that the extractor 04:24
8 terminal is a multi-layer structure. 04:24

9 What exactly in the '102 Patent about the 04:24
10 extractor terminal is multi-layer? 04:24

11 A May I refer you to the discussion we had in the 04:24
12 morning? 04:24

13 Q With respect to the contact hole? Is that what 04:24
14 you were -- 04:24

15 A Well, it refers to the one we said one way to 04:24
16 implement the extractor terminal regions is to 04:24
17 indicate what you have in the -- to duplicate, 04:24
18 replicate, what is shown in the cross-section of 04:25
19 Figure 13 in the common contact portion where you 04:25
20 have -- as I said -- a lower level of metal and an 04:25
21 upper layer of metal and a contact hole, and that is 04:25
22 shown in the common contact portion. 04:25

23 And one way to make the extractor terminal in 04:25
24 102 would be to use exactly the same layers, use the 04:25
25 data line metal for the lower metal and use the pixel 04:25

1 electrode layer for the upper metal. 04:25

2 If you have -- and in this particular 04:25

3 embodiment of it it indicated where it is a specific 04:25

4 sequence of how the layers are laid down, there will 04:25

5 be a contact hole as we discussed that the pixel 04:26

6 electrode layer will go down and cover the edges of 04:26

7 the hole, and cover the bottom of the hole, and in the 04:26

8 bottom of the hole make connections to the lower level 04:26

9 metal. That is one embodiment that one can build. 04:26

10 Q Could you please take this red pen and circle 04:26

11 what you in your opinion you believe corresponds to a 04:26

12 contact hole recited in Claim 15. In other words, 04:26

13 indicate on that Exhibit 2007 which is the enlargement 04:26

14 of Figure 3 the contact hole. 04:26

15 A (Witness complies.) Well, the contact hole in 04:27

16 Claim 15 has certain limitations. There is a contact 04:31

17 hole shown in Figure 3 and is referred to -- 04:31

18 Q Figure 3 of -- 04:31

19 A -- in Shiba. And then that specification in 04:31

20 Shiba, Column 4, line 66, it reads, 04:31

21 "As shown in Figure 3 the data line 04:32

22 part 761 through 764 are exposed 04:32

23 through a slit 243 formed in the 04:32

24 protective overcoat 241." 04:32

25 It is -- slit in the protective overcoat is an 04:32

1 opening in the protective overcoat, and an opening in 04:32
2 an insulating layer is what someone skilled in the art 04:32
3 would refer to as a contact hole. You remove the 04:32
4 insulating layer, so then you allow the surface of the 04:32
5 underlying metal layer, which is below the insulating 04:32
6 layer, to be exposed. 04:32
7 So in Shiba that element 243, which is shown 04:32
8 already in Figure 3, it is labeled and it is depicted 04:33
9 with a dotted line as an opening in the protective 04:33
10 overcoat. 04:33
11 And the -- but in Claim 15 the contact hole has 04:33
12 other limitations as well. And the other limitations, 04:33
13 because Shiba does not include a common terminal made 04:33
14 from the same layer as the pixel electrode, the 04:33
15 contact hole that is shown in Shiba does not meet some 04:33
16 of the limitations such as providing a connection 04:34
17 between the common terminal and the first internal 04:34
18 contacting line, because the common terminal made from 04:34
19 the same layer as the pixel electrode is not disclosed 04:34
20 in Shiba. 04:34
21 So I can -- in your question you asked me to 04:34
22 draw a contact hole which would correspond to 04:34
23 everything recited in Claim 15, and that may not be 04:34
24 possible because Shiba is -- is not having -- is 04:35
25 lacking one element of -- and so the contact hole 04:35

1 which is disclosed in Shiba and which is an opening in 04:35
2 the passivation layer, though it is disclosed it is 04:35
3 not meeting all the limitations of the Claim 15. 04:35
4 But should one modify based on the teaching of 04:35
5 Shiba, and based on the teaching of other priority, 04:36
6 then modify the extractor terminal, they could meet 04:36
7 all the limitations of Claim 15. It would be obvious 04:36
8 how to make structure in light of the teaching of 04:36
9 Shiba, and in view of other priority make a structure 04:36
10 that will meet all the limitations of Claim 15. 04:36
11 Q Is it true also then that you cannot indicate 04:36
12 in Figure 3 of the Shiba structure that that meets the 04:36
13 limitations for the common terminal recited in 04:36
14 Claim 15? 04:36
15 A There is something wrong with the transcript. 04:36
16 Q It should be "recite." This is a rough 04:37
17 transcript. 04:37
18 It says is it true also that you cannot 04:37
19 recite -- let me restate the question. 04:37
20 Is it true that you cannot point to structure 04:37
21 in Figure 3 of Shiba that meets the limitations for 04:37
22 the common terminal recited in Claim 15? 04:37
23 A The extractor terminals in Shiba have some of 04:37
24 the elements or limitations described in Claim 15, but 04:39
25 not all. 04:40

1 Q Which ones does Shiba not show, which 04:40
2 limitations? 04:40

3 A For example, the common terminal in Shiba is 04:40
4 formed from the same layer as the pixel electrode. 04:40
5 That is an explicit limitation imposed in the Claim, 04:40
6 correct? That is what is written here. 04:40

7 Q Yes, that is in the Claim. 04:40

8 A Shiba disclosed what is the pixel electrode, 04:40
9 yet does not disclose what is the material used to 04:40
10 make all that wiring. So we cannot say if that 04:41
11 material is the same or not. 04:41

12 Q Shiba nowhere discloses where, in 127, or any 04:41
13 of those wirings that are referenced in Column 5, 04:41
14 lines 20 to -- 25 to 31, there is no discussion of 04:41
15 Shiba using a pixel electrode material for those 04:41
16 wirings, is there? 04:41

17 A Well, there is no disclosing of any material 04:41
18 that I looked for, and I trust you looked for, and I 04:41
19 could not find any reference for the data lines. 04:41

20 I know that wiring elements listed in that 04:41
21 portion, what is the material that Shiba is using to 04:42
22 make those elements. 04:42

23 Q But Shiba, I think you would agree, discloses 04:42
24 that you can make those elements all from the data 04:42
25 line material? 04:42

1 these wiring elements will be made by that material 04:43

2 because that material is not suitable for making a 04:43

3 14-inch diagonal display. 04:43

4 Q For what reason is it unsuitable? 04:43

5 A Because you need a high conductivity material. 04:43

6 Q And the pixel electrode material disclosed in 04:43

7 Shiba is not a high conductivity material? 04:44

8 A It is a conductive material, but it's 04:44

9 conductivity is much lower than aluminum or chromium 04:44

10 or other materials. 04:44

11 Q The element we've been talking with about 04:44

12 Claim 15 talks about electrically connected, that the 04:44

13 first internal conducting line which you identified as 04:44

14 wiring 127 in Shiba corresponds to 127 in Shiba, I 04:44

15 think you said, am I right? Is that your opinion? 04:44

16 Does the first internal conducting line 04:44

17 correspond to wiring 127, in your opinion? 04:44

18 A Well, I tried earlier to point to another 04:45

19 construction within Shiba 127, and you have 04:45

20 interrupted me. So if I may describe the other means 04:45

21 of creating the wiring 127 in the other means, you 04:45

22 will see the first internal conducting lines are 04:45

23 disclosed. 04:45

24 Q What are you referring to in Shiba? 04:45

25 A I'm referring in Shiba in Column 6, line 37 04:45

1 that it reads, 04:46

2 "Moreover, the first wiring lines 127 04:46

3 may be formed in the step of forming 04:46

4 the scanning lines CJ and the data 04:46

5 lines XI, respectively, thereby 04:46

6 constituting a two-layer structure. 04:46

7 In this case if the layers are 04:46

8 partially connected to each other, the 04:46

9 wiring defect can be prevented in the 04:46

10 manufacturing yield can be improved." 04:46

11 In this section Shiba discloses the first 04:46

12 wiring line in 127 can be made as a two-layer 04:46

13 structure, made of two metal layers, one metal being 04:46

14 the same as that used in the scanning lines and the 04:46

15 other metal would be the same as used in the data 04:47

16 lines. 04:47

17 As we were discussing earlier, the two lines, 04:47

18 data lines and scanning lines, have an insulating 04:47

19 layer interposed between those two and -- 04:47

20 Q Is it shown in Figure 4, the insulating layer 04:47

21 you're talking about? 04:47

22 A The insulating layer is shown. If we look at 04:47

23 Figure 6 you see that the wiring layer which is made 04:47

24 as the same as that used for the source and drain 04:47

25 electrodes, it is located above the insulating layer 04:48

1 211, in which you have identified as the gate 04:48
2 electrode, and in the scanning line CJ, which also 04:48
3 forms the gate electrode, CJ shown in Figure 6, is 04:48
4 located below that layer. 04:48

5 So someone skilled in the art, by looking at 04:48
6 that figure, reading the specifications, and looking 04:48
7 at the sequence that the layers are laid down, and 04:48
8 which comes first and which comes afterwards, it will 04:48
9 be evident that the two-layer structure formed by 04:48
10 using the scanning lines and the data line materials, 04:49
11 those two layers will have an insulating layer in 04:49
12 between. 04:49

13 And that's why Shiba says if the layers are 04:49
14 partially connected, implying that there will be a 04:49
15 contact hole that provide the partial connections, 04:49
16 even with this contact hole there will be a plurality 04:49
17 of those runs. So if there are wiring in other -- 04:49

18 Q It doesn't disclose what you're thinking would 04:49
19 be -- it doesn't exclusively talk about a plurality of 04:49
20 contact holes, does it? 04:49

21 A It talks about it partially connected to each 04:49
22 other. And in the last deposition we had a long 04:50
23 discussion about the meaning of that terminal 04:50
24 connection. If you wish, we can repeat the 04:50
25 discussion. 04:50

1 Someone skilled in the art will see that 04:50
2 partial connections can be made by having these 04:50
3 holes, and Shiba is teaching a way to any other means 04:50
4 of forming it because, as we are discussing before the 04:50
5 break in Column 7, it requires that the protective 04:50
6 overcoat in the gate electrode are directly connected 04:50
7 through each other through the gap between the narrow 04:51
8 lines that form 127. 04:51
9 So Shiba is teaching a way to completely remove 04:51
10 the protective overcoat 241. So if you have a contact 04:51
11 hole, you simply have an opening on the wiring line 04:51
12 127, and you do not affect the integrity of the 04:51
13 overcoat and how that overcoat adheres to the 04:51
14 underlying gate electrode. 04:51
15 Q Are you talking about an opening in the wiring 04:51
16 line, 127? 04:51
17 A I'll sorry. Are you asking me a question? 04:52
18 Q That is the question. 04:52
19 MR. CORDREY: That is the pending question. 04:52
20 MR. SCHLITTER: That is the pending question. 04:52
21 MR. CORDREY: He's asking the question. 04:52
22 THE WITNESS: In my previous answer I said so 04:53
23 if you have a contact hole you simply have an opening 04:53
24 on the wiring line 127. 04:53
25 BY MR. SCHLITTER: 04:53

1 Q What does that mean, an opening on the wire 04:53
2 line? 04:53

3 A That means that you remove a portion of the 04:53
4 protective overcoat in the region which is only 04:53
5 located above the wiring line 127, and you do not 04:53
6 remove the overcoat in the gap between adjacent lines. 04:53

7 Q Protective overcoating region above the wiring 04:53
8 line 127? 04:53

9 A I'm sorry. You have an opening in the -- in 04:53
10 the layer 211 -- I'm sorry -- in the layer 211, in the 04:54
11 gate dielectric layer, the one that will be on top of 04:54
12 the first layer. 04:54

13 We are talking about a double layer line, the 04:54
14 lower level being made to aid the scanning lines, the 04:54
15 upper level to be made in the data lines, and there 04:54
16 will be the layer 211 interposed in between the two 04:54
17 lines, the two metal lines as shown in the two 04:54
18 Figure 6 where you show the data line material above 04:54
19 211, and you see the scanning line material below 211. 04:54

20 So in this particular embodiment in Figure 6 it 04:54
21 shows the embodiment will figure -- the wire lines 127 04:54
22 is a single layer. 04:55

23 Q The source drain layer? 04:55

24 A The source drain layer. 04:55

25 Q 231 and 233 in Figure 6, right? 04:55

1 A I believe so. But it's on -- explicitly on the 04:55
2 sealing region where you have the wiring that is 04:55
3 labeled below as 127. So that multi-wiring structure, 04:55
4 wiring running parallel, they're all indicated above 04:55
5 211. So that will be made of the material of the 04:55
6 source and drain electrode. 04:55

7 Q When you say they're all indicated above 211, 04:55
8 but if you had the two structures you just described, 04:55
9 one of the layers would be below 211, right? 04:56

10 A Correct. So the particular embodiment is a 04:56
11 single-layer structure. The would be -- that is made 04:56
12 with the data line material one. But Shiba disclosed 04:56
13 in the embodiment a means for someone to make wiring 04:56
14 lines that have two-layer structure, and in that one 04:56
15 it disclosed specifically what are the layers, the 04:56
16 materials they use to make the two-layer structure. 04:56

17 Q And those layers are -- 04:56

18 A Made of the scanning line material, the first 04:56
19 layer, and the other one would be with the data line 04:56
20 material. 04:56

21 Because those two layers have the 211 gate 04:56
22 electrode which is formed in between them. That gate 04:56
23 electrode will be between those two layers. Those two 04:57
24 layers will not touch each other because there is an 04:57
25 insulating layer in between them. 04:57

1 So before you put down the layer 211 there will 04:57
2 be opening of contact holes. 04:57

3 Q But before you put down 211 -- 04:57

4 A Before you put down the upper layer metal, 04:57
5 before you put down the metal layer made from the 04:57
6 drain line material, contact holes will be made to 04:57
7 layer 211. 04:57

8 Those contact holes are already performed in 04:57
9 the process. These are not new contact holes. These 04:57
10 are not a new, extra step. 04:57

11 Q Extra contact holes but not extra steps? 04:57

12 A Right. They're extra contact holes, not extra 04:57
13 holes, because this is -- etching is performed to form 04:58
14 other structures. So you just simply open more holes 04:58
15 in the region where you are forming the wire in 127. 04:58

16 Q If you do that, and use the embodiment that you 04:58
17 describe so that you have a two layer wiring line 127, 04:58
18 does that wiring line meet the limitations recited in 04:58
19 Claim 15 for the first internal conducting line? 04:58

20 A Well, it meets the limitations if you modify 04:58
21 the common terminal. 04:58

22 Q Putting aside the common terminal, just the 04:59
23 wiring line? 04:59

24 A Yes. The limitation for the first internal 04:59
25 conducting line is they're created by the first 04:59

1 processing step. That limitation is the first 04:59
2 internal conducting line and the gate electrode to the 04:59
3 thin-film transistor created by the first processing 04:59
4 step. That limitation is met, and you can see that 04:59
5 clearly in Figure 6. 04:59
6 So we have the gate electrode that forms 04:59
7 element CJ, and below the existing lines shown in 04:59
8 Figure 6, 127. We have another set of lines made of 04:59
9 CJ of the material used for making CJ they will be 04:59
10 meeting that limitation made by the first processing 05:00
11 step. 05:00
12 Q If you do that, as you pointed out there is no 05:00
13 structure that corresponds to the contact hole recited 05:00
14 or shown in Figure 3 in Shiba. And there is the 05:00
15 common terminal, according to Claim 15, that needs to 05:00
16 be electrically or needs to be formed from the pixel 05:00
17 electrode, same layer as the pixel electrode, and 05:00
18 Shiba does not disclose that, correct? 05:01
19 A Yes. Shiba does not disclose a common terminal 05:01
20 made of a pixel electrode. But there is teaching 05:01
21 within Shiba that could lead someone skilled in the 05:01
22 art to form such a structure. 05:01
23 Q First of all, Shiba never discloses using the 05:01
24 same layer as the pixel electrode for either the 05:01
25 extractor terminals, the wiring, 127, or the common 05:01

1 terminal, correct? 05:01

2 A Shiba is disclosing the conductive structure 05:01

3 can be made as a two-layer structure. 05:02

4 Q Scanning line layer and data line layer, 05:02

5 correct?

6 A That is the specific combination of metals to 05:02

7 form the first wiring 127. 05:02

8 And the reason that is disclosed in that for 05:02

9 the wiring 127 is because those two metals are the 05:02

10 highest conductivity metals of the three that would be 05:02

11 needed to make the display. They are a metal used for 05:02

12 the scanning lines, a metal used for the data lines, 05:02

13 and a metal used to make the pixel electrode. 05:02

14 In making a long wiring structure where the 05:02

15 goal is to reduce the conductivity, to reduce the 05:03

16 resistance, you will pick the highest conductivity 05:03

17 materials. Those highest conductivity materials are 05:03

18 those used in making the scan lines and the data 05:03

19 lines. It's not the ones used to make the pixel 05:03

20 electrode. 05:03

21 So Shiba is teaching a two-layer structure in 05:03

22 general, and is providing guidance how to construct 05:03

23 this two-layer structure for making this particular 05:03

24 wiring. 05:03

25 If one takes that teaching of Shiba and looks 05:03

1 at the construction of the extractor terminals, 05:03
2 someone skilled in the art will be motivated -- 05:03
3 particularly in view of other prior art that teaches 05:03
4 the advantages of the pixel electrode layer being 05:04
5 present as the outer metal layers, upper conductive 05:04
6 layer that is exposed in the extractor terminal 05:04
7 region. 05:04
8 So though it is not directly mentioned, the 05:04
9 teaching that someone can follow to create such 05:04
10 structure is there, and the particular combination is 05:04
11 explicitly mentioned in other prior art that I use in 05:04
12 my declaration. 05:04
13 Q If you look at Shiba there is a pixel electrode 05:04
14 disclosed; is there not? 05:04
15 A Correct. 05:04
16 Q And that is 251 in Figure 4? 05:04
17 A That is correct. 05:05
18 Q Same in Figure 6? 05:05
19 A Yes. 05:05
20 Q I believe you said earlier the pixel electrode 05:05
21 serves as one of the electrodes of the storage 05:05
22 capacitor opposite the electrode CJ, correct? 05:05
23 A Correct. 05:05
24 Q There is no insulation between the pixel 05:05
25 electrode layer in Shiba and the source drain metal 05:05

1 layer, is there? 05:05

2 A In this particular embodiment? 05:05

3 Q In the only embodiment disclosed in Shiba there 05:05

4 is no insulation between a source drain metal and the 05:06

5 pixel electrode metal, right? 05:06

6 Let me start more easily, because you're 05:06

7 searching through the whole thing. 05:06

8 Look at Figure 4. 05:06

9 A I'm just formulating my answer. 05:06

10 In the particular embodiment there is no 05:06

11 insulating layer between the source drain metal and 05:07

12 the pixel electrode as far as we can see from the 05:07

13 schematics. 05:07

14 Q Or from the specification. 05:07

15 Do you agree the specification doesn't disclose 05:07

16 any specification between those layers either, does 05:07

17 it? 05:07

18 A Do you have a section to refer me for that one? 05:07

19 Q I haven't seen that section, if it's there, so 05:08

20 I'm asking you. 05:08

21 A Something being there cannot be taken as proof 05:08

22 it is not there. 05:08

23 Is there a section that says there is no -- 05:08

24 Q The question I asked is, is there a section 05:08

25 that says it is there? Would you agree it's not shown 05:08

1 in Figure 4, right? 05:08

2 A Well, Figure 4 shows 251, and shows the 05:08

3 protective overcoat 241. And figure -- 05:09

4 Q 241 -- 05:09

5 A -- Figure 6 does not show the protective 05:09

6 overcoat 241. 05:09

7 Q Neither shows protective overcoat 241 05:09

8 separating source draining metal from pixel electrode 05:09

9 layer, does it? 05:09

10 A Well, the question is if we look at Figure 6, 05:09

11 and we -- if you only had Figure 6 to guide us, 241 is 05:09

12 not there. 05:09

13 And then the question is is it not there 05:09

14 because it was removed before pixel electrode came 05:10

15 down or never existed? So that is why I asked you if 05:10

16 you have a guidance to show -- 05:10

17 Q Well, the guidance is this specification never 05:10

18 says there is any insulation present separating the 05:10

19 source drain metal from the pixel electrode. 05:10

20 A Is there a section that lists a specific -- I'm 05:10

21 just trying to save time. That is what I'm trying to 05:10

22 do here, what shows that explicitly. If you know it, 05:10

23 we can save time. 05:10

24 Today we are mostly addressing these terminal 05:11

25 regions and the wiring and how to provide means to 05:11

1 reduce the size of the display and improve 05:11
2 reliability, and not going into detail about how to 05:11
3 construct the pixel electrodes. 05:11
4 Let's hypothetically agree it should be -- that 05:12
5 there should be -- I guess I won't take the time for 05:12
6 this. 05:12
7 Q I don't want to hypothetically agree. 05:12
8 Would you agree that Figures 4 and 6 do not 05:12
9 show such an insulation layer? 05:12
10 A Well, I think I point out some inconsistency 05:12
11 between 4 and 6. 05:12
12 Q Where do you see insulation in either figure 05:12
13 between the pixel electrode and the source drain 05:12
14 metal? 05:12
15 A Well, in Figure 6 it shows nowhere where you 05:12
16 have the pixel electrode 251. But it does show 241 05:12
17 above the source and drain electrode. 05:12
18 Q It also shows protective overcoat 241 above the 05:13
19 pixel electrode 251 in Figure 4; does it not? 05:13
20 A That is what I point to the -- 05:13
21 Q Take that back. 05:13
22 It shows it at least to the left of pixel 05:13
23 electrode 251. 05:13
24 A We -- as far as what is above, and how the 05:13
25 pixel electrode in the source and drain electrode are 05:14

1 laid down, we may have to refer to the specifications 05:14
2 for further guidance. 05:14

3 Q Okay. But Figure 6, would you agree, shows 05:14
4 that source electrode 231 is directly in contact with 05:14
5 pixel electrode 251? 05:14

6 A Well, 251 and 231 are touching the side or the 05:14
7 edge. It's not a very clear schematic of which comes 05:14
8 first and which comes second. 05:14

9 Q They touch each other, at least? 05:15

10 A Yes, they touch each other. 05:15

11 Q The same is true in Figure 4, is it not, 231 05:15
12 and 251 are in direct contact 231 being the source 05:15
13 electrode and 251 being the pixel electrode? 05:15

14 A Right, they are in direct contact. 05:15

15 And the question is are they in direct contact 05:15
16 because there was a preservation removed or in direct 05:15
17 contact because the passivation layer would come 05:15
18 later? 05:15

19 Q How would they come into direct contact by 05:15
20 removing a passivation layer? 05:15

21 A If there was a passivation layer above the 231 05:15
22 and then it was removed, it can create an opening for 05:15
23 the other metal to come down and attach to the 231. 05:16

24 Q Do you mean if you had a protective overcoat 05:16
25 before the pixel electrode was put down? Is that what 05:16

1 for the capacitance, storage capacitors. Thinning it 05:18
2 down it would -- it is an advantage. It would 05:18
3 increase the storage capacitors. 05:18

4 But thinning it down, it creates other risks 05:18
5 that you have a weak spot, and you may completely 05:18
6 remove it. You may etch the weak spot and the second 05:18
7 layer may go down and create a short. Someone skilled 05:18
8 in the art probably will find an alternative way to do 05:19
9 that. But these are -- 05:19

10 Q What would you suggest? So how -- if you 05:19
11 wanted to do your hypothetical and put the pixel 05:19
12 electrode layer down after protective overcoat layer, 05:19
13 as 241 was put down, how would you do that? 05:19

14 A It's not a mention how I would do it. It would 05:19
15 be -- 05:19

16 Q How would a person skilled in the art do that? 05:19

17 A I think the answer is in the 102 in the prior 05:19
18 art in Figure 13, that you form a contact hole on top 05:19
19 of the drain region only. You will not do a blank 05:20
20 etching over an extended region and risk weakening the 05:20
21 integrity of the underlying layers. 05:20

22 That is why one has to look at the 05:20
23 specifications, and in the prior art, and try to 05:20
24 figure out how someone skilled in the art would be 05:20
25 motivated to do something. I do not take a figure 05:20

1 that describes some portion of the overall structure, 05:20
2 but that portion is not the main invention. So we 05:20
3 seem to focus in Figure 4 on the pixel structure, but 05:20
4 that's not the main focus of the Shiba invention. 05:21

5 We should not read too much into the pixel 05:21
6 structure disclosed in Shiba, because the only thing 05:21
7 that guides us are these two figures, and these are 05:21
8 crowded figures. We should look at the figures, and I 05:21
9 believe -- I do not find any consistencies. There are 05:21
10 no inconsistencies in the way that some of the 05:21
11 critical elements that were discussed related to the 05:21
12 wiring, where the wiring exists, how the wirings are 05:21
13 connected, and what purpose they serve, and so on. 05:21

14 Q Looking at Figure 4, if you were to use your 05:21
15 hypothetical and put the pixel electrode layer down 05:21
16 after the protective overcoat 241, then if I 05:21
17 understand your hypothetical you would have two layers 05:22
18 for the dielectric of the capacitor, correct, one 05:22
19 being the gate 205 and the other being the protective 05:22
20 overcoat 241? 05:22

21 A That is correct. That by itself is not a bad 05:22
22 idea. Again, it provides a double layer protection so 05:22
23 then there are no shorts created between the lower 05:22
24 metal and the upper metal. 05:22

25 Q The upper metal being the pixel electrode 05:22

1 layer? 05:22

2 A Correct. 05:22

3 Q Does that increase the capacitance or decrease 05:22

4 the capacitance to add another dielectric layer 05:22

5 between the two electrodes? 05:22

6 A If you increase the thickness that will 05:22

7 decrease capacitance. 05:23

8 Q Is that desirable? It's not desirable 05:23

9 generally, is it? 05:23

10 MR. CORDREY: Objection. Form. 05:23

11 THE WITNESS: Well, the amount of first 05:23

12 capacitance that you need is a function of how good 05:23

13 the transistor is, what is the leakage current of the 05:23

14 transistor, what is your frame rate, and how much your 05:23

15 voltage is going to decrease because of the leakage 05:23

16 current with the transistor, or voltage will change in 05:23

17 your pixel because the transistor may have -- may be a 05:23

18 little transistor. 05:23

19 Ideally, if you have -- in an ideal situation 05:23

20 you will not need a storage capacitance, but some 05:23

21 charge may also leak through the liquid crystal. So a 05:24

22 certain amount of charge is required. But the exact 05:24

23 size depends upon a lot of factors. In general, the 05:24

24 higher the better. 05:24

25 But you do not want to fill the pixel area with 05:24

1 the storage electrode CJ because that will take area 05:24
2 from your light, if you're thinking about a 05:24
3 transmissive display. 05:24

4 But there are other means to form the storage 05:24
5 capacitor that will not increase the thickness. For 05:25
6 example, if the protective overcoat comes after the 05:25
7 source and drain electrode, you then form the storage 05:25
8 capacitor with the extension of the drain electrode 05:25
9 itself, and there would only be the gate dielectric in 05:25
10 between. It will be the same structure as shown in 05:25
11 Figure 4, just the metal that will extend above CJ 05:25
12 will be the source electrode. In that case you 05:25
13 maintain the advantages of the thinner dielectric and, 05:25
14 thus, the higher storage capacitors. So having the 05:25
15 pixel electrode on the top may require that you change 05:25
16 some of your design, but you still have the same 05:26
17 steps. 05:26

18 BY MR. SCHLITTER: 05:26

19 Q I'm sure it absolutely would require a change 05:26
20 from what is disclosed in Shiba to put the pixel 05:26
21 electrode layer above the protective overcoat 241? 05:26

22 A I'm sorry. You said you are sure? 05:26

23 Q No. Isn't it absolutely sure -- I'll restate 05:26
24 the question. 05:26

25 Putting the pixel-like layer above the 05:26

1 protective overcoat layer 241 would require a redesign 05:26
2 of what is disclosed in Shiba; would it not? 05:26
3 A It would require a change in the order with 05:26
4 certain steps that are performed, and may require a 05:26
5 change in the mask design. But once you have the 05:27
6 mask -- and you need to have a certain number of 05:27
7 masks. You do not add anything to the masks. You do 05:27
8 not add numbers to the masks. You are simply changing 05:27
9 the design of the mask. 05:27
10 So you're going to design a set of masks. You 05:27
11 still are going to use five masks, but the design on 05:27
12 this mask in -- some of the masks will be different. 05:27
13 Once you have the mask design, the manufacturing 05:27
14 steps, the number of manufacturing steps will be the 05:27
15 same. The order with which you perform those 05:27
16 manufacturing steps will change. 05:27
17 Q If you don't change the steps, and if you use 05:27
18 what is disclosed in Shiba, isn't it true that the way 05:27
19 227 and what is called in the Shiba the common pad 751 05:28
20 would not have -- would not be made from the pixel 05:28
21 electrode layer? 05:28
22 A If you don't change the ordering of the steps 05:28
23 then you will end up with the particular embodiment 05:28
24 depicted in the figures that we're discussing, 3, 4, 1 05:28
25 and 6. 05:28

1 Q And you -- 05:29

2 A The pixel electrode layer is not present in the 05:29
3 common pad 751. 05:29

4 Q If you redesigned -- if you modified what is 05:29
5 disclosed in Shiba to put an insulating layer such as 05:29
6 protective overcoat 241 between the source drain metal 05:29
7 and the pixel electrode, you would need some 05:29
8 modification to make some connection, would you not, 05:29
9 between the pixel electrode and the source electrode 05:29
10 231? 05:29

11 A What do you mean by you need modification? 05:29

12 Q Well, the way it's disclosed in Figures 4 and 6 05:29
13 is that the source electrode 231 is directly in 05:29
14 contact with the pixel like 251. 05:29

15 If you separate them by an insulating film such 05:29
16 as protective overcoat 241, you would have to figure 05:30
17 out some way to etch them; would you not? 05:30

18 A Well, let me say that what is shown in Figure 4 05:30
19 and 6 it is not very clear. 05:30

20 What is clear is that the step that you need to 05:30
21 do to provide that X has already been performed and 05:30
22 already been disclosed in Shiba, that is the step to 05:30
23 open the -- to create the element 243. 243 is an 05:30
24 opening, is a contact hole, a large contact hole which 05:30
25 is created in the layer 241. 05:30

1 So 241 is removed, and that is the step you 05:31
2 need to do to provide the connection between the pixel 05:31
3 electrode and the drain electrode or the source 05:31
4 electrode, whatever it may be in the pixel region. 05:31
5 Is that clear? 05:31
6 Q How would you modify the structure in Shiba to 05:32
7 arrive at a structure that would meet all the 05:32
8 limitations recited in Claim 15 of the '102 Patent? 05:32
9 Let me narrow that question down -- well, 05:32
10 referring to the common terminal? 05:32
11 MR. CORDREY: Objection. Form. 05:32
12 MR. SCHLITTER: I'll restate the question. 05:32
13 BY MR. SCHLITTER: 05:32
14 Q How how would you modify the structure in Shiba 05:32
15 to arrive at a structure that would meet the 05:32
16 limitations relating to the common term recited in 05:32
17 Claim 15 of the '102 Patent? 05:32
18 A Well, I would -- someone skilled in the art -- 05:32
19 Q Would that be you? 05:33
20 A I think I'm a little bit over qualified since I 05:33
21 have more than working experience than someone skilled 05:33
22 in the art. So I am skilled in the art, but -- 05:33
23 Q More than skilled in the art? 05:33
24 A -- but I think I'm a little bit more than 05:33
25 skilled in the art because you're -- there are just 05:33

1 too many years. I think you do not need 25 years and 05:33
2 a Ph.D. to be skilled in the art. 05:33

3 Q Okay. 05:33

4 A So to someone skilled in the art, it will 05:33
5 modify the order with which the pixel electrode layer 05:33
6 will be put down. 05:34

7 We had a lengthy discussion that is a little 05:34
8 bit unclear how the pixel electrode -- and if we want 05:34
9 to have the pixel electrode to serve as a protective 05:34
10 layer in the extractor terminal, so gain the 05:34
11 advantages of the corrosion protection provided by the 05:34
12 pixel electrode layer, and in particular not the pixel 05:34
13 electrode layer disclosed in 1 or 2 which is the 05:34
14 aluminum -- because aluminum does not provide any 05:34
15 protection -- but the protection that is provided by 05:34
16 the Indium tin oxide which is a chemically stable 05:34
17 material and which does not react with oxygen and 05:34
18 moisture, it does not corrode. 05:34

19 So if one wants to gain that protection in the 05:35
20 extractor terminal region, then it will also put the 05:35
21 pixel electrode on top of the source and drain -- on 05:35
22 top of the source electrode, and the structure will be 05:35
23 as follows; you will form the scan lines. You will 05:35
24 form the transistor, or you will form the data lines. 05:35
25 You will form the source and drain electrodes. You 05:35

1 will form the wiring, the double A wiring that Shiba 05:35
2 is disclosing. Then you put the protective overcoat 05:35
3 241, and then you perform that step that opens the 05:35
4 slit 243. 05:36

5 But someone skilled in the art will not make 05:36
6 just one big opening. He will make many small holes, 05:36
7 openings such as those disclosed in Moriyama, and it 05:36
8 will have many small openings on top of each of the 05:36
9 pads labeled in the extractor terminal, which is like 05:36
10 the 751. 05:36

11 And they will place a contact hole also in each 05:36
12 eye on top of every source, as disclosed in the prior 05:36
13 art of Figure 13 of '102 Patent. And it will form, as 05:36
14 the final layer, the pixel electrode layer made out of 05:36
15 Iridium tin oxide. And that layer will be patterned 05:36
16 to form the pixel electrodes in the display area and 05:37
17 to form the second layer in the extractor terminal 05:37
18 regions, again similar to what is shown in Figure 13 05:37
19 in the prior art. 05:37

20 Q If you were to make your modification, did you 05:37
21 say there would be an opening in the protective 05:37
22 overcoat 241 down to what is called in Shiba a common 05:37
23 pad 751? 05:37

24 A And say that that person will open many small 05:37
25 holes, as disclosed in Moriyama, on top of 751. And 05:38

1 then will put down the pixel electrode material, and 05:38
2 pattern that pixel electrode material as the -- as a 05:38
3 second layer in the extractor terminals, and at the 05:38
4 same time it will form the pixel electrodes in the 05:38
5 display area. 05:38

6 Q So under your hypothetical modification there 05:38
7 would be insulation on top of common pad 751 in Shiba, 05:38
8 there would be -- which would be the protective 05:38
9 overcoat 241 -- 05:38

10 A That is already there. 05:39

11 Q But it's not over 241 as it it is right now? 05:39

12 A Sorry? 05:39

13 Q Common pad 751 -- 05:39

14 A Well, 751 during fabrication it had the 05:39
15 protective overcoat 241 above it. But then the slit 05:39
16 was formed, and that protective overcoat was removed 05:39
17 from that area. 05:39

18 In the modified structure the protective 05:39
19 overcoat will remain everywhere except the regions 05:39
20 that were formed a plurality of smaller contact holes 05:39
21 as shown in, for example, in Moriyama on top of each 05:39
22 one of the electrodes, like 751. 05:39

23 Then you will put the pixel electrode layer, 05:40
24 and you will pattern that pixel electrode layer. What 05:40
25 you will end up with is something like the common 05:40

1 contact portions on Figure 13 of prior art, but option 05:40
2 is to make one big opening as shown in this one. But 05:40
3 someone skilled in the art will be motivated to create 05:40
4 many smaller openings such as disclosed in Moriyama. 05:40
5 Q The pixel electrode layer would be separated 05:40
6 from the common pad 751 layer by the protective 05:40
7 overcoat 241, excepting in the plurality of small 05:40
8 openings you talked about? 05:41
9 A Correct. 05:41
10 Q So it would be a double layer structure? 05:41
11 A Such as the one shown in Figure 13. 05:41
12 Q And the wiring -- 05:41
13 A Of 102. 05:41
14 Q Are you proposing the wiring 127 would have 05:41
15 another ITO layer on top? 05:41
16 A Well, 127 is in a different region than 751. 05:41
17 There is no reason to modify the wiring 127 to change 05:41
18 the metals. That already is disclosed by Shiba, which 05:41
19 would be the best metals, namely, the scan line metal 05:41
20 and data line metal. 05:41
21 Someone skilled in the art would be modified to 05:41
22 only change the extractor terminal regions. 05:42
23 Q May I see this exhibit then? 05:42
24 If you made the modification you are proposing, 05:42
25 would there be a structure corresponding to the 05:42

1 contact hole recited in Claim 15 of the '102 Patent? 05:42

2 A Well, a contact hole already exists in the 05:43

3 present embodiment of Shiba that meets some but not 05:43

4 all the limitations of Claim 15. 05:43

5 The thing that the present embodiment is 05:43

6 lacking is the pixel electrode layer. By modifying 05:43

7 the structure and adding the pixel electrode layer on 05:43

8 top of 751, then the contact hole which will be formed 05:43

9 by the step which is already formed, performed in 05:44

10 Shiba, that is the step that creates slit 243. That 05:44

11 is the same step that will be used to create the 05:44

12 contact holes. That same step will result in the 05:44

13 contact holes that will meet all the limitations, 05:44

14 because we will have the ITO layer or the pixel 05:44

15 electrode layer in the extractor terminal region. 05:44

16 Q Would the first internal conducting line in 05:44

17 that case be electrically connected to the common 05:44

18 terminal in the contact hole? 05:45

19 A Yes. 05:45

20 Q I'd like to take a break. Off the record. 05:45

21 THE VIDEO OPERATOR: We are off the record. 05:45

22 The time is 5:45 p.m. on July 12, 2013. This is the 05:45

23 end of video No. 4 of the continuing deposition of 05:45

24 Dr. Milt Hatalis. 05:45

25 (Recess taken.) 05:59

1 THE VIDEO OPERATOR: We are back on the record. 06:00
2 Time is 6:00 o'clock p.m. on July 12, 2013. This is 06:00
3 the beginning of video five of the deposition of 06:00
4 Dr. Milt Hatalis. 06:00
5 BY MR. SCHLITTER: 06:00
6 Q Referring to the Exhibit 2007, which is a 06:00
7 version of Figure 3 from Shiba, if you made the 06:00
8 modification you proposed so that you would add a 06:00
9 pixel layer, a pixel electrode metal layer over common 06:00
10 pad 751 and the extractor terminal, that is what 06:00
11 you're proposing; is it not? 06:00
12 A That is the modification of the terminal, and 06:01
13 there is an associate modification that would go along 06:01
14 in the pixel region. 06:01
15 Q If you made that modification then in Figure 3 06:01
16 where will the connection be made between -- well, let 06:01
17 me back up. 06:01
18 If you made the modification what would 06:01
19 correspond to the common terminal that is called for 06:01
20 in Claim 15? What in your modified version of 06:01
21 Figure 3 in Shiba in your opinion would correspond to 06:01
22 the common terminal recited in Claim 15? 06:01
23 A It would be the pixel electrode metal layer 06:02
24 that will be added. 06:02
25 Q Where would that actually be in that Figure 3? 06:02

1 A There will be a series of such metal layers on 06:02
2 top of each one of those pads 751, 761, 762 and so on. 06:02

3 Q Could you draw with the red pen where you would 06:02
4 place the common terminal, the structure in Figure 3, 06:02
5 the modified structure in Figure 3 that would, in your 06:02
6 opinion, correspond to the common terminal in 06:02
7 Claim 15? Can you do that? 06:02

8 A Well, that would -- 06:04

9 Q Use the red pen this time. 06:04

10 A That figure is a little bit rounded figure 06:04
11 here. 06:04

12 Do you mind if I draw a structure on the side, 06:04
13 and if you wish I can do the structure as well as the 06:04
14 cross-section of it? 06:04

15 Q Well, can you not indicate on Figure 3 where 06:04
16 that would go? 06:04

17 A Well, Figure 3 has this slit 243. That opening 06:04
18 is created and surrounded by 243 would be replaced 06:04
19 by -- as we discussed earlier, someone skilled in the 06:04
20 art would change that design from one big contact hole 06:04
21 to many small contact holes, and those will be placed 06:05
22 within 751. But I can -- 06:05

23 Q Are you saying to me you would not count slit 06:05
24 243 as the contact hole under your proposed 06:05
25 modification? 06:05

1 A Well, 243 is something that is formed. It is 06:05
2 something which is formed by an etching step. 06:05

3 So the present embodiment in Shiba is 06:05
4 performing an etching step that creates the contact 06:05
5 hole 243, and that contact hole serves to connect the 06:05
6 wiring that comes externally, which is this flexible 06:05
7 connector 711 to the pad 751 to 764 on the glass 06:05
8 substrate. That is what that contact hole presently 06:06
9 is serving in this particular embodiment. 06:06

10 If we are going to modify the embodiment and 06:06
11 add the pixel electrode layer in the common terminal 06:06
12 region, we will still perform an etching step such as 06:06
13 the one created -- such as the one used to create the 06:06
14 opening 243. But instead of opening one big contact 06:06
15 hole, someone skilled in the art would be motivated to 06:06
16 open many smaller contact holes, and the level of the 06:06
17 figure is such that it is not easy to show these 06:06
18 contact holes at this level of detail. 06:07

19 Q So are you saying under your proposed 06:07
20 modification -- first of all, the slit 243 does not 06:07
21 correspond to the contact hole recited in Claim 15, I 06:07
22 think you already established earlier today? 06:07

23 A Well, we established that 243 is a contact hole 06:07
24 in the protective layer 241. 06:07

25 Q But it doesn't electrically connect to a common 06:07

1 terminal made by the pixel electrode layer, does it? 06:07

2 A Right. It does not meet all the limitations of 06:07
3 the contact hole because one layer is not present in 06:07
4 this particular embodiment of Shiba, namely, the pixel 06:07
5 electrode layer. 06:07

6 Someone, in view of the teaching in Shiba and 06:07
7 in view of other prior art, could modify and add that 06:07
8 pixel electrode layer and then all the limitations of 06:08
9 the contact hole will be met. So there is a contact 06:08
10 hole and a common hole as an opening. That opening 06:08
11 serves a purpose in the particular embodiment, but 06:08
12 because it's lacking one layer it will not make a 06:08
13 connection with that layer because that layer is not 06:08
14 present in this particular embodiment, but it will 06:08
15 modify. And without that layer the same contact hole 06:08
16 will meet all the limitations. 06:08

17 Q In Figure 4, under your modification you would 06:08
18 have a pixel electrode layer where? 06:09

19 A Well, in Figure 4, since we're modifying the 06:09
20 structure, I will first extend the source electrode 06:09
21 element 231 to overlap to the capacitor CJ, and that 06:09
22 will be the upper electrode of the storage capacitor. 06:09

23 So imagine the 231 extends past CJ, and then 06:09
24 somewhere between -- somewhere above the new 231 there 06:09
25 will be a contact hole in the protective overcoating 06:09

1 layer 241. In that contact hole will be the same 06:10
2 contact hole which is presently being used to form the 06:10
3 slit 243, and we will simply put the ITO -- we open 06:10
4 that contact hole on top of the element 231. I can 06:10
5 draw it, if you wish. 06:10
6 But it would be better if I draw it with my own 06:10
7 next to it, because this is already kind of crowded 06:10
8 and a complicated figure. 06:10
9 Q Go ahead and draw it. You have to draw fast. 06:10
10 A Okay. Stop the clock while I'm drawing. 06:10
11 You want me to draw the pixel electrode 06:10
12 structure? I will skip some of the TFT details. 06:11
13 241 or 251? 251. 06:11
14 Q You've just drawn the transistor part? 06:13
15 A The part on the source side. 06:13
16 Q Where does the wiring, 127, connect to the new 06:13
17 common pad, 751? 06:14
18 A Do you want me to draw the pixel structure? 06:14
19 Q I would like to know how to do -- how the 06:14
20 common pad 751 connects to the wiring 127. 06:14
21 MR. SCHLITTER: Should we go off the record 06:14
22 while he draws? 06:14
23 MR. CORDREY: That's fine. 06:14
24 THE VIDEO OPERATOR: We are off the record. 06:14
25 The time is 6:14 p.m. 06:14

1 with my description of it? Do you need any more 06:20
2 clarification? 06:20
3 I have no further questions about what you just 06:20
4 said. 06:20
5 A On the right? 06:20
6 Q Yes. 06:20
7 A The one on the left, it is in the extractor 06:20
8 terminal. So we see the layers made from the -- that 06:20
9 forms the element 751 which is made up of the data 06:20
10 line layer. We see 241, the protective overcoat, to 06:20
11 be above it. We see the openings formed in 241, so 06:20
12 two contact holes that are formed. As I said, it 06:21
13 would be motivated to create many small openings 06:21
14 instead of one big opening. 06:21
15 And also the ITO, that ITO is patterned at the 06:21
16 same time the pixel electrode ITO, and both ITOs -- 06:21
17 Q On the figure which is exhibit -- your copy is 06:21
18 Exhibit 2007? 06:21
19 A About -- 06:21
20 Q Yes, under your modified version of the Shiba 06:21
21 structure, where would the common terminal be? 06:21
22 A Well, as my drawing showed it will be roughly 06:22
23 where 751 is present, and it will extend -- 06:22
24 Q Just draw with a red pen indicating on Figure 3 06:22
25 where the modified common terminal would be. 06:22

1 A Can I draw a planar section view of this one? 06:22

2 Q I'd rather just see in Figure 3. 06:22

3 A Can I draw it here in Figure 3? 06:22

4 Q Can you not indicate on the drawing that is 06:22

5 Figure 3 where the common terminal would be? 06:22

6 A Well, you see, the common terminal has to be 06:22

7 positioned with respect to the metal layer and with 06:22

8 respect to the contact holes. So I need to draw 06:22

9 contact holes, and the level of magnification is -- 06:22

10 Q Just draw the extent of it and we'll understand 06:23

11 there are contact holes there. 06:23

12 A I'd rather -- if I do it here, would you mind? 06:23

13 Q I'd rather you do it on Figure 3. I won't 06:23

14 understand the modification. 06:23

15 A I'll draw my -- 06:23

16 Q Then you're not modifying Figure 3. I want to 06:23

17 see modified Figure 3. 06:23

18 A Well, Figure 3 -- 06:23

19 MR. CORDREY: Objection. Form. 06:23

20 THE WITNESS: Figure 3 is such level 06:23

21 magnification the detail I want to indicate the ITO on 06:23

22 top of the metal. 06:23

23 BY MR. SCHLITZER: 06:23

24 Q Just draw on Figure 3 the extent of the common 06:23

25 terminal, and then you can draw off to the side more 06:23

1 detail, if you would like. But I want to see where 06:23
2 the common terminal goes in Figure 3. 06:24

3 A And you want me to do it with the red pen? 06:24

4 Q Yes.

5 A And then if I go all the way up to the edge I 06:24
6 will run to the edge of the substrate and -- 06:24

7 Q Use a green pen. It is a fine point. 06:24

8 A See, I cannot draw, with my artistic skill, one 06:25
9 and then do another one, because they will just be 06:25
10 touching. 06:25

11 Q You mean because there is more than one of 06:25
12 the -- 06:25

13 A Well, if you're going to put in the ITO on top 06:25
14 of each one of them, you're not going to protect one 06:25
15 pad. 06:25

16 Q Do they all constitute the common terminal? 06:25

17 A No. The common terminal is one. But while you 06:25
18 form the common terminal you'll also be putting ITO. 06:25

19 Q I don't care about those. I just want you to 06:25
20 draw where the common terminal goes in your modified 06:25
21 version. 06:26

22 A Okay. As long as you are agreeing you're not 06:26
23 going to say ITO between the other things is going to 06:26
24 be short to my drawing. 06:26

25 Q I'll not agree to anything. 06:26

1 A You're saying I can draw a magnified version? 06:26

2 Q Yes, but may I just see what you've done. 06:26

3 Okay. 06:26

4 So the green indicates what you believe 06:26

5 corresponds to -- with the modification you've 06:26

6 proposed, the common terminal as you said in Claim 15? 06:26

7 A Well, the green will be something that overlaps 06:26

8 the present metal that constitutes 751. So green is 06:26

9 the ITO layer that will overlap the drain metal 751, 06:27

10 and I place it roughly because I couldn't draw the 06:27

11 contact holes. I asked you earlier in such a small 06:27

12 magnification, so I'm going to draw on the bottom here 06:27

13 a magnified portion of that part. 06:27

14 Q Of the green rectangle you drew? 06:27

15 A Well, the planar section view of my 06:27

16 cross-section. 06:27

17 Q Would that correspond to an enlarged view of 06:27

18 what you indicated with the green rectangle? 06:27

19 A Well, I place the green rectangle in reference 06:27

20 to existing openings in 243. And over here I'm going 06:27

21 to draw a planar section view of that one because I 06:27

22 cannot place many small holes here, but just indicate 06:27

23 that the ITO will overlap the opening. 06:28

24 I will draw you the 751 with many small 06:28

25 openings, and I will draw it in green, and I will use 06:28

1 different colors to indicate each layer. 06:28

2 Q You are going to do a cross-section? 06:28

3 A Cross-section is already here, and I'm going to 06:28

4 do a planar section. 06:28

5 Q A planar section will correspond to the green 06:28

6 rectangle? 06:28

7 A The only difference between my planar section 06:28

8 and the green rectangle is that the green rectangle in 06:28

9 the existing figure -- though you insisted I modify -- 06:28

10 I placed the green relative to the existing opening 06:28

11 because I cannot draw openings in the 751. So I 06:28

12 placed the green so it overlaps the opening, goes 06:29

13 beyond the edge of the opening. 06:29

14 And if I'm going to draw here, how should it 06:29

15 actually be done? I will modify the size of the 06:29

16 opening, and it will show it in more clarity how one 06:29

17 will modify. 06:29

18 The fabrication step will be the same. The 06:29

19 mask design is the one that is going to change. 06:29

20 Q The fabrication order changes? 06:29

21 A Right, but it does not add steps. It just 06:29

22 exchanged the order with which the steps are 06:29

23 performed. 06:29

24 Without the steps -- 06:29

25 Q I don't think we need to -- 06:29

1 is the ITO, and red are openings. 06:32

2 Q Would you no use the slit 243 then in your 06:32
3 modified version? 06:32

4 A You could use the slit, but a more effective 06:32
5 protection is provided if you have many small openings 06:32
6 instead of one large opening. 06:32

7 Q So you would -- 06:32

8 A I would change the design. 06:33

9 Q If you used your multiple small openings you 06:33
10 would not use the slit 243 to make the connection to 06:33
11 the common terminal? 06:33

12 A Well, if I'm going to modify things I would 06:33
13 adjust the design. It's the design I'm modifying, not 06:33
14 a step of forming that structure. 06:33

15 Q Would you use slit 243 if you used the multiple 06:33
16 openings that you've sketched on that Exhibit 2007? 06:33

17 A It is one approach to use existing design and 06:33
18 put ITO. In that case you put the ITO the way I have 06:33
19 drawing, if there is no Figure 3 that you insisted 06:33
20 that I modify. But you asked me how would I modify 06:33
21 it, and I would modify with a smaller opening in view 06:33
22 of Moriyama. 06:34

23 Q Instead of using one slit you would use that 06:34
24 plurality of openings? Is that what you're saying? 06:34

25 A That is what was taught by Moriyama where it 06:34

1 addresses the creation of an extractor terminal with 06:34
2 an ITO as a protective layer. 06:34

3 You could use the existing slit. You would 06:34
4 still have the same protection that if -- the slit is 06:34
5 an etching step. It forms one big opening, and you 06:34
6 can form many smaller openings. The step is the same. 06:34

7 Here the blue is a drain layer and the red is 06:35
8 the contact, or is that clear? 06:35

9 Q The red is the openings, you said? 06:35

10 A Right, so the transcript is clear. 06:35

11 Q I have what I think is a short question. It's 06:35
12 a different issue. 06:35

13 But looking at the element of Claim 39 in 06:35
14 Column 19 it begins, on line 4, it says -- I'll read 06:35
15 this, 06:35

16 "A third internal conducting line 06:35
17 formed from the same layer as the 06:36
18 source electrode and the drain 06:36
19 electrode are the thin-film 06:36
20 transistor." 06:36

21 Does Shiba disclose structure that corresponds 06:36
22 to that third internal conducting line? 06:36

23 A Yes. 06:36

24 Q Where is that disclosed in Shiba? 06:36

25 A It is not disclosed with the exact name. Its 06:36

1 inventor assigns its own terminology. That part is 06:36
2 disclosed in Shiba and corresponds to a third internal 06:37
3 conducting line formed from the same layer as the 06:37
4 source electrode and the drain electrode. 06:37
5 It is disclosed in Column 6, line 10, and it 06:37
6 reads, 06:37
7 "Then the first wiring line 127 is 06:37
8 guided along the first shorter side 06:37
9 201c to the first longer side 201a, 06:37
10 and the narrow lines meet together at 06:38
11 the interconnecting part 125." 06:38
12 So the part of the first wiring line 127 which 06:38
13 is guided along the first shorter side 201c and which, 06:38
14 as we discussed earlier, is made with the data line 06:38
15 material which is the same material that is used to 06:38
16 form the source and drain electrodes in the 06:38
17 corresponding third internal -- 06:38
18 Q That would be the one on the right side in 06:38
19 Figure 1 on Shiba? 06:38
20 A The right side is the 201c. 06:38
21 Q That would be what corresponds, in your 06:38
22 opinion, to the third internal conducting line 06:38
23 referenced in that portion of Claim 39 we just read? 06:38
24 A Correct. 06:39
25 Q Moriyama discloses in the internal portion 06:39

1 three metal layers, correct? 06:39

2 A Can you give me the Moriyama exhibit? I cannot 06:39

3 form my own objections. 06:39

4 Q I hand you what was previously marked as CMI 06:39

5 Exhibit 1004. 06:39

6 (Exhibit 1004 was previously marked

7 for identification and is attached

8 hereto.)

9 BY MR. SCHLITTER:

10 Q Do you see the question? Is it correct that 06:40

11 Moriyama discloses three metal layers in terminal 06:40

12 portion, layers 1, 3 and 4; is that correct? 06:40

13 A Well, depending upon what embodiment in 06:40

14 Moriyama you're referring to. 06:40

15 Q There are only three conductive layers in any 06:40

16 of the embodiments in Moriyama, are there not, 13 and 06:40

17 4? 06:40

18 A Not in the prior art of Moriyama depicted in 06:40

19 Figure 9. 06:41

20 Q Let me take a look. 06:41

21 What layers are depicted in Figure 9? 06:41

22 A There are two layers depicted in Figure 9. 06:41

23 Q Okay. 06:41

24 A A lower level element one and an insulating 06:41

25 layer, openings in the insulating layer that is the 06:41

1 element two, and an upper layer, element four, which 06:41
2 is made of ITO. 06:41

3 What I have drawn in my schematic that I have 06:41
4 annotated, and in both these exhibits in Figure 3 and 06:42
5 4 are duplicating the structure that is shown in 06:42
6 Figure 9 and -- 06:42

7 Q Figure 7 of Moriyama discloses three metal 06:42
8 layers instead of two, correct? 06:42

9 A That's Moriyama's changes to the prior art. 06:42

10 Q Seven is prior art? 06:42

11 A No, nine is prior art. Seven is the embodiment 06:42
12 that I invented. 06:42

13 Q The question is in seven, does Figure 7 in 06:42
14 Moriyama disclose three conductive layers? 06:42

15 A Figure 7 disclosed three conductive layers. 06:42

16 Q And those layers are 1, 3 and 4? 06:43

17 A That is correct. 06:43

18 Q And layers 3 and 4 directly contact each other; 06:43
19 is that correct?

20 A In that embodiment, that is correct. 06:43

21 Q There is not an insulating film separating 06:43
22 layers 3 and 4 disclosed in Moriyama, is there? 06:43

23 A In that embodiment, no. 06:43

24 Q In any embodiment is there anything in Moriyama 06:43
25 where layers 3 and 4 are separated by an insulating 06:43

1 film? 06:43

2 A You focus in the embodiment that uses three 06:43

3 metal layers, and I point out that someone skilled in 06:43

4 the art may motivate you to change the Shiba 06:43

5 structures and implement something as a figure shown 06:43

6 for Figure 9a. 06:43

7 Q But that is not the question. 06:43

8 The question is, isn't it true that metal does 06:43

9 not disclose an insulating film separating layers 3 06:44

10 and 4? 06:44

11 A In the embodiment that employ 3 and 4 is not. 06:44

12 But as I see there is one embodiment that -- in which 06:44

13 is using two layers such as the one that someone 06:44

14 skilled in the art would be motivated to modify Shiba 06:44

15 terminal region. 06:44

16 Q In Figure 7 there is an insulating film five 06:44

17 that separates one from layers 3 and 4. Do you see 06:44

18 that? 06:44

19 A The insulating layers is the same insulating 06:44

20 layers used in embodiment 9. 06:45

21 Q That is the same as 9a, and seven are the same 06:45

22 insulating layer five, correct? 06:45

23 A That is correct. But someone skilled in the 06:45

24 art will take the teaching, which is -- maybe is 06:45

25 expressed in the embodiment 9a, and what is the 06:45

1 teaching? How to provide a protection to a metal 06:45
2 layer that will be exposed in the external -- in the 06:45
3 extractor terminal. 06:45

4 So in Figure 9a I have the metal layer one, I 06:45
5 have a passivation layer on top of it. I create 06:45
6 openings in the passivation layer and I cover the 06:45
7 one -- and the openings with the ITO layer. That 06:45
8 teaching is directly as you see in all my drawings of 06:45
9 Moriyama. 06:46

10 So the element one, shown in Moriyama, is made 06:46
11 of certain materials that the cross-section -- if you 06:46
12 put it side-by-side in 9a and the cross-section I 06:46
13 drew, they're identical. In Moriyama the sequence of 06:46
14 the layers is different. 06:46

15 But what is the essence here to someone skilled 06:46
16 in the art is the means to create an extractor 06:46
17 terminal that will be resistant to corrosion, and that 06:46
18 is something that someone skilled in the art will be 06:46
19 able to construct. 06:46

20 Q Does Shiba talk about as an objective 06:46
21 preventing corrosion? 06:46

22 A Shiba is not addressing the issue and corrosion 06:46
23 the extractor terminals region. 06:47

24 MR. SCHLITTER: We have to go off the record. 06:47

25 THE VIDEO OPERATOR: We are off the record. 06:47

1 The time is 6:47 p.m. 06:47

2 (Recess taken.) 06:47

3 THE VIDEO OPERATOR: We are back on the record. 06:52

4 The time is 6:53 p.m. 06:53

5 MR. SCHLITTER: In view of the hour I don't 06:53

6 have any further questions. 06:53

7 MR. CORDREY: I don't have any questions. 06:53

8 THE VIDEO OPERATOR: We are off the record. 06:53

9 The time is 6:53 p.m. on July 12, 2013. 06:53

10 This concludes today's testimony given by 06:53

11 Dr. Milt Hatalis. Total number of media used was five 06:54

12 and will be retained by Veritext Legal Solutions. 06:54

13 06:54

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I, MILTIADIS HATALIS, Ph.D., do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made such corrections as appear noted herein, in ink, initialed by me, or attached hereto; that my testimony as contained herein, as corrected, is true and correct.

EXECUTED this _____ day of _____,
2013, at _____, _____.
(City) (State)

MILTIADIS HATALIS, Ph.D.

1 STATE OF CALIFORNIA)
) ss

2 COUNTY OF ORANGE)

3 I, the undersigned, a Certified Shorthand
4 Reporter of the State of California, do hereby
5 certify:

6 That the foregoing proceedings were taken
7 before me at the time and place herein set forth; that
8 any witnesses in the foregoing proceedings, prior to
9 testifying, were placed under oath; that a verbatim
10 record of the proceedings was made by me using machine
11 shorthand which was thereafter transcribed under my
12 direction; further, that the foregoing is an accurate
13 transcription thereof.

14 I further certify that I am neither financially
15 interested in the action nor a relative or employee of
16 any attorney of any of the parties.

17 IN WITNESS WHEREOF, I have this date subscribed
18 my name.

19
20 Dated: 16 July, 2013

21
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23
24
25

Sherry A. Case

SHERRY A. CASE
RFR, CLR, CLR, CSR No. 2989

06:54

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