

SEL EXHIBIT 2013

INNOLUX CORPORATION v. PATENT OF SEMICONDUCTOR ENERGY
LABORATORY CO., LTD.

IPR2013-00068

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
3

4)
 4 INNOLUX CORPORATION,)
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 5)
 5 Petitioner,)
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 6)
 6 vs.) No. IPR2013-00068
) Patent 8,068,204
 7)
 7 PATENT OF SEMICONDUCTOR)
 ENERGY LABORATORY CO., LTD.,)
 8)
 8)
 8 Patent Owner.)
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14 VIDEOTAPED DEPOSITION OF MILTIADIS HATALIS, PH.D.
15 Irvine, California
16 Tuesday, July 2, 2013
17 Volume I
18
19
20

21 Reported by:
DENISE BARDSLEY
22 CSR No. 11241
23 Job No. 1683385
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25 PAGES 1 - 153

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4 INNOLUX CORPORATION,)
5 Petitioner,)
6 vs.) No. IPR2013-00068
) Patent 8,068,204
7 PATENT OF SEMICONDUCTOR)
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Videotaped deposition of MILTIADIS HATALIS, PH.D., Volume I, taken on behalf of Patent Owner, at 3 Park Plaza, Suite 1100, Irvine, California, beginning at 9:14 a.m. and ending at 5:44 p.m. on Tuesday, July 2, 2013, before DENISE BARDSLEY, Certified Shorthand Reporter No. 11241.

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INDEX

WITNESS EXAMINATION
MILTIADIS HATALIS, PH.D.
VOLUME I

BY MR. MANZO 7

EXHIBITS
(NONE)

1 Irvine, California, Tuesday, July 2, 2013

2 9:14 a.m.

3
4 THE VIDEOGRAPHER: Good morning.

5 We are on the record at 9:14 a.m. on July 09:14:45

6 2nd, 2013. This is the video-recorded deposition of

7 Dr. Milt Hatalis. My name is Scott Slater, here

8 with our court reporter, Denise Bardsley.

9 We are here from Veritext Legal Solutions

10 at the request of counsel for the patent owner. 09:15:07

11 This deposition is being held at 3 Park Plaza, Suite

12 1100, in Irvine, California 92614. The caption of

13 this case is Innolux Corporation versus Patent of

14 Semiconductor Energy Laboratory Co., Ltd., Case

15 No. IPR2013-00068, Patent 8,068,204. 09:15:34

16 Please note that audio and video recording

17 will take place unless all parties agree to go off

18 the record. The microphones are sensitive and may

19 pick up whispers, private conversations or cellular

20 interference. I am not authorized to administer an 09:15:57

21 oath, I am not related to any party in this action,

22 nor am I financially interested in the outcome in

23 any way.

24 May I please have an agreement from all

25 parties that we may proceed? 09:16:08

1 MR. MANZO: So agreed.

2 MR. GIBSON: I agree.

3 THE VIDEOGRAPHER: Thank you.

4 At this time will Counsel and all present
5 please identify themselves for the record. 09:16:17

6 MR. MANZO: I'm Edward Manzo for the patent
7 owner, from the firm -- law firm of Husch Blackwell,
8 LLP. With me is my partner, Mark Murphy, from the
9 same firm, and also with us is --

10 MR. SCHLITTER: Stan Schlitter from Steptoe 09:16:38
11 & Johnson, also for the patent owner.

12 MR. GIBSON: Stan Gibson on behalf of the
13 petitioner.

14 THE VIDEOGRAPHER: Thank you very much.
15 Will the court reporter please administer the oath. 09:16:47

16
17 MILTIADIS HATALIS, PH.D.,
18 having been administered an oath, was examined and
19 testified as follows:

20
21 EXAMINATION

22 BY MR. MANZO:

23 Q Good morning, Professor.

24 A Good morning.

25 Q I am placing before you a copy of the Shiba 09:17:11

1 reference, which was marked as Exhibit 1003
2 previously, and it bears Patent No. 5,684,555.

3 Is it okay with you if we just refer to
4 that as Shiba in these proceedings?

5 A That will be fine. 09:17:40

6 Q Now, before we dig into the examination, we
7 asked you a lot of questions yesterday morning about
8 your background, and we're hoping that we don't need
9 to repeat all those today and that we can rely on
10 yesterday's testimony with regard to your background 09:18:29
11 and other examination on technical issues.

12 Is that agreeable, Counsel?

13 MR. GIBSON: His background is fine; I
14 don't believe it's changed from yesterday to today.
15 I'm not sure what you mean by rely on other 09:18:44
16 examination on technical issues. Certainly we don't
17 need to cover his background again.

18 MR. SCHLITTER: We intend to use both the
19 transcripts, probably, from yesterday and today and
20 both the '413 IPR and '204 IPR if that turns out to 09:19:04
21 be appropriate. There are a lot of questions that
22 relate to the same exhibits in both --

23 MR. GIBSON: I don't disagree with that. I
24 just don't know what it means to use the same
25 technical understanding, so it is just too broad of 09:19:20

1 a term.

2 If we have an objection to using something
3 in a different one, then I don't know what that
4 would be. At this point I'd have to see how we are
5 using it. I don't think we need to repeat questions 09:19:32
6 from yesterday.

7 MR. SCHLITTER: Okay.

8 MR. MANZO: Thank you.

9 Q Professor --

10 A Before we proceed, since you're not going 09:19:41
11 to be asking me any more questions about my
12 background, may I make a comment related to some of
13 the questions you asked me yesterday, for the
14 record?

15 Q That's somewhat unusual. 09:19:59

16 What are they? Technical issues?

17 A No, no. They are related to my experience
18 in patent litigation. You asked me a lot of
19 questions in those areas and you asked me,
20 percentagewise, about the income I received from 09:20:16
21 patent litigations and so on.

22 Q Sure. Why don't you go ahead.

23 A So --

24 Q Let me ask you a question.

25 Could you please clarify some of the issues 09:20:27

1 that were raised yesterday that you thought about
2 further overnight regarding your background.

3 A Sure. Thank you.

4 You asked me a lot of questions about my
5 litigation experience against -- a series of case 09:20:40
6 against SEL, and you also asked me a lot of
7 questions related to, percentagewise, the income I
8 received from patent litigation work. And I was
9 going to make a comment that compared to the experts
10 that wrote the two response -- the two expert 09:21:03
11 reports for the last two patents that I was
12 involved, I find out that I have less litigation
13 cases than them and that their rates are
14 significantly higher than mine.

15 So I just want to clarify, that case, that 09:21:24
16 some of them also work for more than one case,
17 several cases on behalf of SEL.

18 You comment that I worked against SEL,
19 that's because some of my clients were being sued --
20 not my clients, but some of the law firms were being 09:21:42
21 sued by SEL, so I represented defendants in this
22 case, or in some case. And the other experts
23 represented SEL against some of the same clients.

24 So my litigation experience and my income
25 is less than what it is, than the other experts. 09:22:03

1 Q I see.

2 A Thank you.

3 Q Thank you.

4 Professor, I'm placing before you a copy,
5 also, of Exhibit 1001, which is the patent involved 09:22:26
6 in this inter partes review, Hirakata U.S. Patent
7 8,068,204.

8 Are you familiar with that patent?

9 A Yes.

10 Q And I'm also placing before you a copy of 09:22:49
11 the declaration that was filed as Exhibit 1007 in
12 this case.

13 Could you look at that Exhibit 1007 and see
14 if that's the declaration that you signed?

15 A Yes, it is. 09:23:41

16 Q Could you please tell me if -- I'd like to
17 know how this declaration was prepared. And so my
18 first question is: Did you do the search for prior
19 art that you applied in this patent -- in this
20 declaration? 09:24:11

21 A No, I did not.

22 Q How did you come to cite these particular
23 references?

24 A I was provided, by the counsel, some prior
25 art references, and I selected the most relevant for 09:24:27

1 this particular content.

2 Q Did you begin by reading the patent in
3 question, Hirakata, Exhibit 1001?

4 A Of course. I read '204, I tried to
5 understand what '204 -- what is the subject matter 09:24:53
6 of '204, what is the objective of '204, what are the
7 specifications and the claims of '204, and then I
8 reviewed the pieces of prior art that I was provided
9 and selected the ones I thought was the most
10 relevant from that pool. 09:25:16

11 Q And your selection was based on the claims
12 at issue; is that right?

13 A Correct.

14 Q How did you prepare for today's deposition?

15 A I reviewed my declaration, I reviewed the 09:25:51
16 petition for the inter partes review, I reviewed the
17 board decision, I reviewed the initial response of
18 the patent owner, I also reviewed the request for
19 rehearing by the patent owners, the decision of the
20 board on the rehearing request and, of course, I 09:26:21
21 review the '204 patent and the three patents that
22 are cited in my declaration and which were accepted
23 by the board as a basis for these hearings and the
24 patent by Shiba, the patent by Sukegawa and the
25 patent by Watanabe. 09:26:48

1 I don't remember the exact patent numbers.

2 If you want, I can refer to.

3 Q No.

4 A It is referred to in my declaration.

5 Q That's fine. 09:26:59

6 And you met with your counsel for four
7 days -- I'm sorry. You met with counsel for
8 petitioner for four days in preparing for these two
9 days of depositions?

10 A Correct. 09:27:15

11 Q In those four days did you cover both
12 patents or did you have four days for each patent?
13 Four days for the one and four more days for the
14 other one?

15 A No, we covered both, and we did not work 09:27:27
16 full time because two of those days were the
17 weekend.

18 Q Let me start with the Shiba reference,
19 which I think is the one you relied on primarily; is
20 that correct? 09:28:00

21 A Correct. The Shiba, Sukegawa and Watanabe.

22 Q Does Shiba have an objective or desire to
23 maximize the display area relative to the outside
24 dimensions of the panel?

25 A Yes, it does. 09:28:49

1 Q Can you explain how Shiba goes about
2 achieving that objective, briefly?

3 A One of the issues in making a panel -- one
4 of the steps in making a panel is the part that
5 assembles and seals the two counter substrates in an 09:29:20
6 area which is referred to as the seal area, and that
7 area occupies -- is all around the display and has a
8 certain width along the transverse direction of the
9 seal that is a distance that a lot of people tried
10 to minimize because the whole seal area is kind of a 09:29:52
11 wasted area. It is needed in order to seal the
12 liquid crystal within, but it doesn't serve any
13 other purpose.

14 If one tried to make a seal very narrow,
15 there are problems that the seal is not very 09:30:15
16 effective. If you make it very wide, you waste more
17 area for that one.

18 So the wiring that Shiba is proposing
19 enables the user from a narrower sealant. That's
20 one of the objectives in Sukegawa -- sorry -- in 09:30:46
21 Shiba, and that's one of the approaches that he's
22 taking.

23 And another approach that he's taking, to
24 reduce the dimensions of the panel.

25 And here I like to make a comment, since 09:31:10

1 you were combining the proceedings from yesterday
2 and today, that yesterday I was making a lot of
3 statements about the -- that someone skilled in the
4 art would know that minimizing the waste area and
5 trying to make as much as possible of the display 09:31:28
6 area relative to the size of the glass is very
7 relevant.

8 As you see here, it was an issue that was
9 well known and a lot of researches attempted to
10 maximize the size of the display relative to the 09:31:50
11 size of the glass that's used to make that display.

12 So the other -- continuing for Shiba is the
13 other approach that Shiba is introducing is means to
14 provide signals to the display only from two sides
15 and relative to prior art that were providing 09:32:24
16 signals from four sides or three sides, and that
17 would require more bonding area for pads and so on
18 in these other sides. So by having two sides,
19 that's an improvement.

20 And in order to access the pads, which are 09:32:40
21 away from the areas, from the terminal regions from
22 the pad areas that receive the signals and the power
23 from the outside circuit board, Shiba is proposing a
24 specific wiring that will have benefits of reduced
25 resistance and improved manufacturing yield by 09:33:15

1 eliminating manufacturing defects, in essence by
2 having a two-layer wiring structure.

3 And there may be other things. If you
4 want, I can read more to Shiba and give you a bit of
5 a summary. From the top of my head, I can refer to 09:33:36
6 Shiba and give you more detail if I missed
7 something, but --

8 Q Let me ask some more specific questions.

9 Does Shiba aim to reduce the width of the
10 seal region without lowering the strength of 09:33:51
11 adhesion between the two substrates?

12 A That is correct, by creating a wiring in a
13 specific way that will have more surface contact
14 area with the sealant, one can reduce the width of
15 the sealant, while still maintain the strength of 09:34:14
16 adhesion between the two substrates.

17 Q And, finally, does Shiba also declare that
18 his or her invention does not increase the number of
19 manufacturing steps?

20 A That is correct. 09:34:42

21 Q Let me invite your attention to Figure 3.

22 And, as I see it, Figure 3 has a lower
23 portion and an upper portion. Does that
24 characterization seem reasonable to you?

25 A I can follow you. 09:35:19

1 Q Okay. So what, generally, is the lower
2 portion of Figure 3?

3 A The lower portion is the external flexible
4 wiring that comes and attaches to the glass, and the
5 two pieces make contact in the terminal regions 09:35:38
6 where you have the pads via anisotropic conducting
7 field.

8 Q So you referred to two pieces. Is the
9 first piece the lower part and the second piece the
10 upper part? 09:36:35

11 A The upper part is the glass substrate that
12 contains the display area, the wiring, the seal, the
13 counter substrates.

14 Of course, not everything is shown at this
15 level of details, but I can refer to the exact 09:36:55
16 Watanabe is calling the elements.

17 Q I don't need that.

18 A Okay. It isn't called the array substrate,
19 it's the glass substrate.

20 Q Okay. So where is the display region of 09:37:16
21 this LCD depicted in Figure 3?

22 A The display region is within the seal area.
23 The seal area is element 111, 111.

24 Q Do you mean that the display area is within
25 the region circumscribed by the seal area 111? 09:37:56

1 A No, I mean it is inside.

2 111 is two lines. It's run parallel like a
3 band. And within that band, over here, the upper
4 left corner is the start of the display. It is the
5 display surrounded by the 111 band. 09:38:23

6 Q Yes.

7 A So it is inside.

8 It extends beyond the inside line of 111.

9 Q And relative to what's been marked as X1,
10 X2, X3, X4 and X5, where is the display area? 09:38:41

11 A X1 is the first signal lines, data signal
12 lines, also referred to as data lines. So X1, X2,
13 X3, X4 is the first data lines of the array. And
14 there may be hundreds of such lines, which it starts
15 from the X1, and then you put one next to each other 09:39:25
16 at specific interval, which is determined by the
17 spacing between pixels. And depending upon the form
18 of the display and how many lines you have, you have
19 640 of such lines if it's a VGA, monochrome, 640
20 times three if it is VGA color, and so on. 09:39:50

21 Q And so --

22 A And then these are the data signal lines.
23 And you also have the scanning lines. The scanning
24 lines are orthogonal to the data lines. They start
25 from the opposing side of the display. The 201d is 09:40:20

1 one of the short sides of the display. The opposing
2 side of that one is at 201c, so the scanning lines
3 start from that side and they propagate orthogonal
4 to the X lines, which are the data lines. And
5 either the first or the last is the one that
6 terminates right past X1.

09:40:57

7 And the first one -- the first one,
8 probably, it goes up to where that square label
9 125a.

10 Q Okay.

09:41:20

11 A Stops short of that one.

12 Q Okay. Thank you.

13 So if you looked at Figure 1, for example,
14 together with Figure 3, it is fair to say that
15 Figure 3 is the bottom left corner of Figure 1 in a
16 blowup view?

09:41:32

17 A In Figure 1 there is a rectangle drawn
18 called A. So Figure 3 is a magnification of the
19 content within that rectangle labeled A.

20 Q Good. So the display area is up and to the
21 right of Figure 3, generally speaking, yes?

09:41:53

22 A Yes. It starts from this corner and
23 propagates --

24 Q Okay.

25 A -- up and to the right.

09:42:14

1 Q Now, in Figure 3 is area 731 a power supply
2 pad? That's that box off to the corner of the
3 sealant region.

4 Do you see it?

5 A Yes, I see it. 09:42:34

6 Q Is that a power supply pad?

7 A It is the pad that provides the power to
8 the counter substrate. It is referred in column 5,
9 line 51, as the power supply pad 731.

10 And what it does is it receive a signal 09:43:24
11 from the common pad 751. And the common pad 751
12 receives the power or the signal from the external
13 wiring 711.

14 And then that through wiring, that signal
15 goes to 731, and then through a conductive means, 09:43:55
16 like an epoxy that contains conductive particles,
17 731 is making contact to the counter substrate that
18 will be bonded to the substrate that is shown to the
19 glass substrate 201.

20 The two substrates will be bonded through 09:44:34
21 the seal, but the seal is not conductive. The
22 seal -- or the epoxy that will be placed on the pad
23 731 is a conductive one, and that will provide the
24 connection to the ITO layer that it covers the
25 entire surface of the counter glass substrate, which 09:44:55

1 is the counter electrode for the pixels.

2 Q Thank you.

3 Just generally speaking, in Figure 4, just
4 below Figure 3, is the display region to the right
5 and the terminal region to the left? 09:45:43

6 A In that cross section?

7 Q In that cross section, yes.

8 A Correct. The right, the left with respect
9 what -- with respect to the seal, yes.

10 Q I was talking about left and right with 09:46:07
11 respect to the page that's on, but that's also with
12 respect to the seal.

13 So to the left of the seal, somewhat to the
14 left of the seal, is a terminal region, correct?

15 A Outside, correct. 09:46:23

16 Q All right. That's outside. And to the
17 right of the seal you can call inside, and that's
18 where the display region is?

19 A Correct. That's where you have a specific
20 gap between the two substrates, and the liquid 09:46:34
21 crystal is contained within.

22 Q And the pad 731 that you testified about a
23 little while ago is shown in Figure 4 about -- near
24 the bottom about 1 inch from the left side.

25 Do you see it? 09:46:58

1 A I see it.

2 Q And then above that there is a substance or
3 a part 115. Is that the -- what the patent refers
4 to as transfer material? I think you called it an
5 epoxy that's conductive. 09:47:16

6 A Correct.

7 Q So that transfers electrical potential to
8 the counter substrate, which is part, it looks like,
9 501; is that correct? Well, the counter substrate,
10 whatever number it is. 09:47:46

11 A The whole concept is 500. 501 is the glass
12 substrate. On the counter substrate -- on the
13 counter substrate you have the ITO layer.

14 Q Okay. Now, going back to Figure 3, just to
15 confirm a few small things, is pad 731 electrically 09:48:31
16 in common with the line 121 dash what looks like a 1
17 or an I?

18 A I think it is a 1.

19 Q You think. Okay. Yes or no?

20 MR. GIBSON: Objection; form. 09:48:54

21 THE WITNESS: What do you mean
22 "electrically in common"? It is formed by the
23 extent -- it is the same metal. It's form is a big
24 rectangle in the pad 731, and then the metal
25 continues and forms that wiring 121. They are all 09:49:16

1 pre-made by the same material. And that material is
2 the material of the data lines.

3 BY MR. MANZO:

4 Q Okay.

5 A Could be made with other material, but the 09:49:29
6 preferred embodiment, it is from the data lines, it
7 is listed.

8 Q I'm sorry. You are looking for something?

9 A Looking at the material that is made, like
10 in column 6, line 25, "In the case where TFTs of 09:50:07
11 bottom gate type are used as switching devices as in
12 the above embodiment, the power supply pads 731 to
13 738, the common pad 751, the third wiring lines,
14 121-1 to 121-4, the inter-connecting pad 125a, and
15 125b the second wiring lines 123-1 to 123-4, and the 09:50:43
16 first wiring line 127 can be formed in the same step
17 of forming the data lines Xi."

18 So it is the same material. And the mask
19 that is used has a big rectangle where it is labeled
20 731, it has a narrow wiring line 121, and so on. 09:51:14

21 So they are not different pieces, they are
22 formed all from the same initial metal layer that
23 was put and covered the entire substrate, at least
24 the remaining metal that's left.

25 Q Okay. So I think that all I'm trying to 09:51:38

1 say is that they are electrically in common. They
2 could be part of the same layer, but not be
3 connected, right, because of masking -- strike that.
4 That's unclear.

5 When a person puts down a layer of metal, 09:52:05
6 it is governed by the mask; is that right?

7 MR. GIBSON: Objection; form.

8 THE WITNESS: Well, you put the metal and
9 cover the entire substrate, and then you use a
10 masking step followed by an etching step to the 09:52:24
11 regions of the metal to form the different elements.

12 Some of those regions, such as the lines
13 X1, X2, X3, X4, they are long continuous lines
14 starting from the pad 761 and continue to the other
15 end of the display and stopping short of the other 09:52:53
16 sealant, of the opposing side of the sealant.

17 Other regions, such as the ones that I just
18 quoted from the patent, namely, 731, 121, 751, 123,
19 125 and 127, they are all continuous metals and just
20 say different ways, but all part of one continuing 09:53:29
21 pattern that is connected.

22 BY MR. MANZO:

23 Q Fine.

24 A It's -- there is no any discontinuity.

25 From 751 you can go to all those regions and still 09:53:52

1 be on the same metal.

2 And -- so, for example, if 751 you put like
3 5 volts in 751, you give it the potential of 5
4 volts, then all that wiring in that pad will be held
5 at 5 volts. 09:54:30

6 Q Okay. So if you put 5 volts on 751,
7 there's also going to be 5 volts on 121-1 and 731
8 and 123-1 and 127 and 125 -- well, I'm not sure
9 about 125a -- strike 125a -- is that correct?

10 A 125a is also part of it. It is a square 09:54:54
11 piece of metal.

12 Q Okay.

13 A From Figure 3. And then there are other
14 elements from Figure 1 that also will be at 5 volts.
15 It will be the 732 -- well, the 732 receives -- but 09:55:08
16 from 751 it will be 731, 735, 736, 737, 738, so it
17 will be multiple pads that will receive that signal.
18 And it continues, also, on the other side.

19 Q Professor, where is 732 -- sorry?

20 A You see that in Figure 1. 09:55:43

21 But I said strike that one because 732
22 receives a signal from another pad, not the 751.

23 Q Okay.

24 A But the one from 751 goes to 731 and then
25 through the wiring 127 goes to 735, -36, -37, -38, 09:55:59

1 and it continues and gets connected up to 734.

2 Q Pardon me. Where is 734?

3 A You can see that in Figure 1.

4 Q I see.

5 A It's the lower right corner. 09:56:30

6 Q Thank you.

7 A The wiring 727 forms almost like a pi, a
8 Greek pi letter and kind of surrounds the display
9 starting from 751 back.

10 Q I'm not sure how it resembles the Greek 09:57:12
11 letter pi.

12 A It is like a P, it is like this, that and
13 then that.

14 Q Oh, with regard to the -- I -- what you're
15 saying is that looking at Figure 1, which is a plan 09:57:34
16 view, the lines 127, if they start at the bottom
17 left, rise upward and then traverse across to the
18 right and then traverse downward?

19 A Correct.

20 Q And that's what the Greek letter pi 09:57:52
21 somewhat looks like?

22 A Yes.

23 Q Now, is it correct that lines 127 are not
24 electrically in common with the data line pads shown
25 in Figure 3 as 761, 762, 763 and 764? 09:58:19

1 MR. GIBSON: Objection; form.

2 THE WITNESS: You are using -- you
3 introduced new terminology, "electrically in
4 common," which is not -- I'm not familiar with this
5 term.

09:58:40

6 BY MR. MANZO:

7 Q All right. Let me --

8 A Electrically connected or same potential?
9 What do you mean? Touching?

10 Q Let me ask you a broad, open-ended
11 question, then.

09:58:49

12 A Okay.

13 Q Is there a relationship between the power
14 supply pad 731 and the data line pad 761, 2, 3 and
15 4?

09:59:04

16 A The common pad 751, that is connected, and,
17 as we said earlier, the 5 volt in 751, it will be
18 5 volt in 731. That is controlled by the external
19 wiring, which is labeled 821a, which is the first
20 external wiring from the element 711 from the lower
21 part of -- the lower part -- not the Figure 4, say
22 Figure 3, the wirings 821a, that's the wiring that
23 provides the signal to common pad 751.

09:59:32

24 Q Okay. And to the right of 821a there are
25 further lines?

10:00:00

1 A Right. Other pads. Each one connected to
2 a data line, and they receive signal from the
3 external wirings, other external wirings. If those
4 external wirings happen to be the same voltage as
5 the 751, then there may be -- one of the data wiring 10:00:30
6 may also be in the same voltage, but that's because
7 the signal is received and happens to be in the same
8 voltage.

9 So if, for example, they all get 5 volts,
10 5 volts will appear to all of them. Maybe the 10:00:44
11 5 volts only go to 751, and 761 get 1 volt, and 762
12 get 2 volts, 3 volts or 4 volts, they can all be
13 separate, separate potentials, independently
14 determined by the outside circuit.

15 Q Okay. So it's fair to say that pad 751, 10:01:02
16 761 through 764 are five independent pads?

17 A Correct.

18 Q Now --

19 A There are four -- as we said, there will be
20 hundreds of these pads. There will be four pads 10:01:32
21 that will have the same voltage as 751, and you will
22 be able to see that in Figure 1.

23 Q I think you described those --

24 A Okay.

25 Q -- a little while ago. 10:01:48

1 A But all the other pads, they will be
2 independent.

3 Q Okay. Is the sealant marked as region 113
4 in Figure 4?

5 A The sealant material -- 10:02:11

6 Q I just want to know the part number of the
7 sealant.

8 A Yeah, 113 is the sealing material.

9 Q And you mentioned that in your declaration
10 at paragraph 48, I think. 10:02:35

11 Could you confirm that on page 15?

12 A Yes. So 113 is the sealant material and
13 111 is the seal region; in other words, what is the
14 projection or the regions on Figure 3 where the
15 sealant will be applied. 10:03:04

16 Just clarify, the 111 and 113.

17 Q Going back to 111, then, in Figure 3, some
18 of the -- well, looking at the reference number
19 111 -- do you see it?

20 A Yes, the seal region. 10:03:30

21 Q And just to the right of the number 111
22 there are these lines marked in a bracket as 127?

23 A Correct.

24 Q Now, some of those are in solid lines and
25 some of those are in broken lines. 10:03:43

1 Why is that?

2 A The ones that are in broken lines, they are
3 considered to be under the sealant -- under the
4 sealant. So they will be covered by the sealant
5 material. So, in a way, if the sealant material is 10:04:03
6 opaque, you wouldn't be able to see them. So the
7 artist kind of do them with broken lines to say that
8 they will be there. Even if you look from the top
9 of the glass, you won't be able to see them. If you
10 look from the bottom side of the glass, you will be 10:04:17
11 able to see them.

12 Q And the unbroken lines?

13 A And the unbroken lines, the continuous
14 lines, those are the lines outside the sealant.

15 Q Now, is there anything in Figure 3 that you 10:04:35
16 regard as an external connection line?

17 A Well, as we discussed, 751, 121, 731, 123,
18 125 and 127, they are all made by the same metal
19 film, and that metal film is continuous.

20 So that metal that goes all the way out to 10:05:07
21 751, or starting from 751, and that metal continues
22 and provides a signal to all those elements. Those
23 elements are labeled differently in order to
24 illustrate the purpose of those things, but it's the
25 same metal line which is continuous. So that's 10:05:35

1 metal, which is all those things are the same
2 potential because all part of the same metal, which
3 is continuous, is the external connection line.

4 Q Is there anything in Figure 3 that you
5 regard as an auxiliary line within the meaning of 10:06:03
6 the claims of the '204 patent?

7 A The purpose of the line that the patent
8 labels 127 -- 127, column 6, line 5, it reads,
9 "refers to wiring line 127 is drawn from the
10 interconnect in pad 125a," and so on, and then it 10:06:55
11 says, "as shown in Figure 1, the first wiring line
12 127 has got a longer segment, shorter side, 201d, to
13 the second longer side, 201b and connected to the
14 power supply pad 735 to 738 through the branch wired
15 line. Then the first wiring line 127 is guided 10:07:25
16 along the first shorter side to 201c to the first
17 longer side 201a."

18 So the wiring 127, the first wiring 127,
19 runs a very long distance.

20 And if we look further down column 6 in the 10:07:51
21 line 37, it reads, "The first wiring lines 127 may
22 be formed in the step of forming scanning lines Yj
23 and the data lines Xi, respectively, thereby
24 constituting a two-layer structure. In this case,
25 if the layers are constantly connected to each 10:08:23

1 other, the wiring defect can be prevented and the
2 manufacturing yield can be improved."

3 In that section it reads that the 127 is --
4 it has two layers, and one layer made by the data
5 wiring metal, that's the upper layer, that's the 10:08:46
6 auxiliary line -- sorry -- that's the external
7 connection line that we have identified a moment
8 ago, and the lower metal is low -- lower layer is
9 made by the material of the scanning lines, and
10 that's the auxiliary line. 10:09:04

11 Q Okay. So is it your testimony that the
12 external connection line and the auxiliary line have
13 the same number in Figure 3?

14 A They are overlapping one on top of the
15 other, and they occupy the same area. 10:09:36

16 Now, the auxiliary line is indicated in
17 this wiring element 127. So both auxiliary lines
18 and external connection lines are within the element
19 127.

20 Q Okay. Professor, I'd like to spend a 10:10:09
21 moment trying to understand the relationship between
22 Figure 3 and Figure 4.

23 Do you have an understanding of any such
24 relationship?

25 A I don't know what you mean. I do 10:10:50

1 understand what's in Figure 3 and 4 and all the
2 other figures, and Shiba, as I studied as well.

3 Q Well, what is Figure 4?

4 A Figure 4 is a cross section along the line
5 that in Figure 3 it shows a-a prime. 10:11:16

6 Q That's what the patent says, isn't it?

7 A I believe so.

8 Q Okay. So if we were to look and slice
9 through this structure at the line a-a prime, we
10 would theoretically see what is shown in Figure 4; 10:11:50
11 is that right?

12 A Correct.

13 Q Professor, I had some problems verifying
14 that because, for example, the pad 731 in Figure 3
15 is not along that slice or that line from a-a prime, 10:12:24
16 and yet it's shown in Figure 4.

17 Do you see that?

18 A Yeah, I see that. But it is not uncommon
19 for the artist to try to depict essential elements,
20 that occasionally I've seen in other works that the 10:13:08
21 lines -- typically when you see a cross section is
22 like a slice through one continuous straight line,
23 but I've seen in other that the line can actually be
24 like almost like some arbitrary shaped line in which
25 the elements that will be along that arbitrary 10:13:33

1 shaped line for the purpose of the teachings are
2 illustrating in the cross section.

3 That's done in order to save space so the
4 author will not have to draw two or three or more
5 cross sections to illustrate the relative location 10:13:57
6 of the different elements to try to include them in
7 the same figure for illustration purposes.

8 Q In your experience, don't draftsmen usually
9 indicate that they are doing that on the plan view
10 so you can avoid having to wonder where the cross 10:14:25
11 section is taken?

12 A Well --

13 MR. GIBSON: Objection; form.

14 THE WITNESS: These documents are meant to
15 be read by people with ordinary skill within the 10:14:42
16 art. And the people use them to learn and be
17 educated, and they already have a certain background
18 and a certain experience that thinks that may not be
19 clear to someone who is not skilled in the art, it
20 is clear for them. So you point out some 10:15:09
21 differences in the artwork. I don't think that
22 would be a big issue for someone skilled in the art.

23 BY MR. MANZO:

24 Q Okay. Looking at Figure 4, can you trace a
25 signal path from the terminal region into the 10:15:42

1 display region?

2 A Well, in this particular cross section,
3 the -- as you point out, it doesn't -- the terminal
4 pads, it doesn't go to the display regions, it
5 provides a connection to the element 731. So it 10:16:23
6 terminates there.

7 Outside the seal region, it shows the cross
8 section along 751 to 123, and inside the seal region
9 it shows transistors and different elements,
10 everything, the pixel. 10:17:01

11 Q Now, before you were talking about the
12 person skilled in the art who would understand these
13 drawings.

14 What would such a person have been or how
15 do you describe such a person as of 1997? 10:17:18

16 A Well, in general terms, it would be a
17 person who has enough experience to be able to read
18 those documents and be able to understand their
19 meaning and be able to understand the teachings and
20 be able to take the teaching and implement 10:17:43
21 structures and be able to combine different piece of
22 arts to create new structures that contain elements
23 from different pieces of prior art.

24 Q Can you describe their education and their
25 experience in terms of degrees and whether they are 10:18:35

1 a circuit designer or a process design engineer?

2 A Well, this is an interdisciplinary field,
3 so you have people with different backgrounds coming
4 from different fields. You can have people with a
5 science background, like physics and chemistry, but 10:19:01
6 you can also be from material science or you can be
7 from an engineering field, such as electrical
8 engineering, chemical engineering.

9 And those people, they have some courses as
10 part of their education, which is relevant to this 10:19:34
11 technology. They also receive further training at
12 the workplace, and we discussed about that
13 yesterday, whether they are process engineers or
14 circuit designers.

15 I believe after a few years in the field, 10:19:56
16 all these peoples from different background, they
17 will be able to understand these prior art pieces
18 such as Shiba.

19 Q Does Figure 4 show an external connection
20 line and an auxiliary line? 10:20:36

21 A No. It shows -- you asked me if it shows
22 an external connection line and an auxiliary line.
23 It shows an external connection line.

24 Q Which one is the external connection line?

25 A It is 751. It is connected to 731, which 10:21:12

1 continually is labeled 751 -- same line, different
2 portion is labeled 121-1 and another portion, same
3 setting, is label 731.

4 This is only a segment of the line, the
5 metal wiring that is formed starting from 751. We 10:21:58
6 discussed earlier about the other pieces that are
7 formed from the same material, they are
8 continuously -- that go under the seal, like 123 and
9 127, which are not shown in Figure 4 but are shown
10 in Figure 3. 10:22:26

11 Someone skilled in the art -- 751 is shown
12 as a single layer in this.

13 Q Do you see a storage capacitor in Figure 4?

14 A Yes.

15 Q Is it formed of these three layers, a 10:23:20
16 electrode Cj, or C subscript j, an insulator 211 and
17 an electrode 251?

18 A In column 4, line 7, it reads, "The storage
19 capacitor is constituted by the pixel electrode 251
20 and the storage capacitor lines Cj." 10:24:31

21 Q Why is a storage capacitor formed or shown
22 in Figure 4?

23 A Well, the artist, as we discussed earlier,
24 is trying to depict some critical elements outside
25 the sealant and critical elements inside the 10:25:08

1 sealant. So the critical elements inside the
2 sealant is a pixel structure, and the elements --
3 and the storage capacitor is one element within the
4 pixel. So the artist try to show how that storage
5 capacitor is formed. 10:25:37

6 Q What factors would impact the size of the
7 storage capacitor?

8 A What do you mean by that?

9 Q Well, for example, does the thickness of
10 insulator 211 impact the size of the storage 10:26:07
11 capacitor?

12 A The capacitance depends on the thickness of
13 the dielectric, which is in between the two
14 electrodes, it is actually inversely proportional to
15 the thickness of the insulating layer between them. 10:26:31
16 211 is the gate dielectric and is in between the two
17 electrodes.

18 So as you increase the thickness, the
19 capacitance will decrease, the storage capacitance
20 will decrease. 10:26:57

21 Q Professor, if two insulators are stacked
22 one on top of the other, is it technically possible
23 to remove only the upper insulator by etching
24 without causing any damage to the lower insulator?

25 MR. GIBSON: Objection; form. 10:27:57

1 THE WITNESS: Is this part of these
2 proceedings?

3 BY MR. MANZO:

4 Q I don't think that that's a responsive
5 answer. 10:28:23

6 A No, I tried to put it within the context
7 whether I missed something here, and I want to say
8 something in Shiba is referring to it, and I want to
9 put in the context of the '413 patent and the prior
10 art that I review and try to give you a response. 10:28:38

11 I don't recall that something that came out
12 as a part of the '413 and the three patents that we
13 are referring to today and we need to provide
14 deposition -- testimony of those three.

15 Q Well, with regard to the knowledge of the 10:29:01
16 person ordinarily skilled in the art in 1997, if
17 there are two stacked insulators and you needed to
18 etch through one of them, can it be done without
19 causing damage to the lower of the two insulators?

20 MR. GIBSON: Objection; form. 10:29:28

21 THE WITNESS: And can I ask you can you
22 please point out where that question is related to
23 the proceedings to the material that I have been
24 called to testify here so I can put my answer in a
25 context? 10:29:43

1 But I don't think the material -- that's
2 something I have studied to give you a thorough
3 answer today.

4 BY MR. MANZO:

5 Q So are you saying that, technically, you're 10:30:25
6 not aware of that?

7 MR. GIBSON: Objection; relevance.

8 THE WITNESS: I'm saying that the question
9 that you are asking is in a subject matter that I
10 have not review and I'm not prepared to give you a 10:30:44
11 response today because I don't think that question
12 deal with any of the material that I have studied.

13 And I have been informed that you can ask anything
14 you wish, but I'm prepared to discuss the prior art
15 that I have in front of me and not to give you 10:31:05
16 answers -- I'll try -- but you asked me something
17 and I asked for guidance so I can place my answer in
18 proper context. But I do not recall this question
19 come, that it was something that I had to deal with.

20 BY MR. MANZO: 10:31:25

21 Q Well, you're experienced with etching; is
22 that right?

23 A Yes.

24 Q Have you tried to etch stacked insulators
25 and just etch your way to the top level of two 10:31:45

1 stacked insulators without any over etching of the
2 lower insulator?

3 MR. GIBSON: Objection; relevance.

4 THE WITNESS: I have worked with many
5 insulators and different substrates, and I have to 10:32:12
6 review my notes. If you guide me to some specifics,
7 I may be able to give you a response, but this is a
8 very big open-ended question that you are asking.

9 MR. MANZO: Why don't we take a short
10 recess. 10:32:36

11 THE VIDEOGRAPHER: We are off the record.
12 The time is 10:32 a.m. on July 2nd, 2013. This is
13 the end of video number 1 of the continuing
14 deposition of Dr. Milt Hatalis.

15 (Recess.) 10:32:52

16 (Whereupon Conrad Szuladzinski
17 replaced Scott Slater as the.)

18 THE VIDEOGRAPHER: This is the continuation
19 of the deposition of Milt Hatalis. My name is
20 Conrad Szuladzinski, and I am the videographer. And 11:13:38
21 we are back on the record at 11:13 a.m.

22 BY MR. MANZO:

23 Q Professor, in paragraph 48 of your
24 declaration, which is Exhibit 1007, you referred to
25 wiring lines with a two-layer structure. And you've 11:14:39

1 referred to the passage, I think, at column 6,
2 earlier this morning about the two layers; is that
3 right?

4 A Yes.

5 Let me add, two-layer structure that are 11:15:06
6 overlapping, but there is an insulating layer in
7 between and which is partially connected.

8 Q Can you describe how the two layers are
9 created and form the line that you're talking about,
10 please, and include -- if you would, explain why you 11:15:35
11 conclude that there is insulation there.

12 A Okay. Column 6, line 36, is our section
13 where it reads, "Moreover, the first wiring lines
14 127 may be formed in the step of forming the
15 scanning lines Yj, and the data lines Xi." 11:16:22

16 So if we go to different sections of the
17 patent trying to understand what are those two
18 layers are formed and what occurs in between them,
19 you go to column 4 at line 1, it reads, "Each
20 scanning line Yj is used as the gate dielectric of a 11:17:07
21 TFT 221."

22 Then you go further down in column 4, line
23 12, it says, "As shown in Figure 4, this scanning
24 lining Yj and the storage capacitor line Cj are
25 formed on the glass substrate 201. The scanning 11:17:31

1 line Yj itself is used as the gate dielectric of the
2 TFT 121. A gate dielectric 211, having a laminated
3 structure of silicon oxide and silicon nitride, is
4 formed on the gate dielectric Yj."

5 So in these sections it talks about right 11:17:55
6 on top of the glass substrate, you are forming the
7 scanning lines so you leave portions of the film
8 that was deposited onto the glass substrate to form
9 the different wirings and the scanning lines, and
10 capacity lines is a set of lines, and the portion of 11:18:19
11 the wiring on 127, as we read earlier, is formed at
12 that time. And this is the lower layer.

13 Q Made of?

14 A The material which is used to make this
15 scanning lines. And the sentence at column 4, line 11:18:42
16 15, which reads, "Gate dielectric having a laminated
17 structure of silicon oxide and silicon nitride is
18 formed the gate dielectric."

19 It shows that after the scanning line is
20 put down and is patterned to form different elements 11:19:02
21 that remain, then the dielectric is formed and the
22 dielectric is deposited by, typically, some sort of
23 a CPT technique that it covers the entire substrate.

24 And then the -- then, based on the sections
25 of column 6, line 31 that reads, "If the layers are 11:19:36

1 proximately connected to each other" -- that section
2 means that after the gate dielectric has been
3 formed, some step is occurring to open contact holes
4 on top of the gate material, the scanning line
5 material. And then we put down the material of the 11:20:09
6 data lines.

7 And then that material has been patterned
8 to form the data lines and the upper layer of the
9 wiring 127.

10 So what you have is the lower layers, made 11:20:31
11 of the scanning line material, you have the gate
12 dielectric 211 in between, you have openings in the
13 gate dielectric, and then you put down the data line
14 material and you pattern that one and it forms the
15 upper layer. 11:20:58

16 Q In creating the gate dielectric that you
17 read about, the gate dielectric 211, and the
18 specification at column 4 says, at line 16, "silicon
19 oxide and silicon nitride," is there control over
20 where those regions -- where those dielectrics end 11:21:29
21 up?

22 MR. GIBSON: Objection; form.

23 THE WITNESS: Well, what do you mean by
24 "control"?

25 BY MR. MANZO: 11:21:37

1 Q Is there a masking step or patterning?

2 A During the deposition or after the
3 deposition?

4 Q Yes.

5 MR. GIBSON: Objection; form. 11:21:51

6 THE WITNESS: These are two different
7 things. During deposition, there is no masking
8 step. Deposition is a high-temperature step so the
9 material goes everywhere and covers the entire
10 substrate. It is a masking step and an etching step 11:22:07
11 that will follow the deposition process.

12 And if one wants to create the -- what is
13 referred to in column 6, the -- if one is to enable
14 the layers to be partially connected, so someone
15 skilled in the art says if the layers are constantly 11:22:30
16 connected, if so, if someone wants to build a
17 double-layer structure, then you have -- you need to
18 create an opening in the gate dielectric to -- at
19 least one opening to enable the partial connection.

20 BY MR. MANZO: 11:22:49

21 Q How do you know that the dielectric is not
22 etched away from the lower layer? What is the
23 teaching?

24 A What do you mean "lower layer"?

25 Q From the lower layer of lines 127. 11:23:06

1 A Well, you have a masking step, right? And
2 the masking step protects the great majority of the
3 surface area where the dielectric layer will remain
4 and only leaves exposed the portions of the area
5 where you want that oxide and nitride film to be 11:23:32
6 removed so it will expose the underlying layer of
7 127 so that the upper layer of 127 will come down
8 the hole and touch the lower layer. And, by doing
9 that, will create the partial connection that's
10 referred to in column 6. 11:24:02

11 In that etching process you need to remove
12 the entire gate dielectric, so you need to remove
13 both the silicon oxide and the silicon nitride so
14 the lower metal layer that were made by the scanning
15 line metal is exposed. So then the upper layer 11:24:23
16 metal when it is deposited, it will touch it, it
17 will make direct contact with it.

18 Q Are you -- forgive me, Professor, but now
19 I'm even more confused.

20 You put down the scanning line layer and 11:24:53
21 then you define lines?

22 A Correct.

23 Q And then you put down nitride and oxide as
24 dielectrics, and then you etch, correct?

25 A Then you do a photo step and you pattern 11:25:12

1 the regions that you want to etch.

2 Q Okay.

3 A Define the regions that you want to etch.

4 Q Now, does this reference, Exhibit 1003,
5 tell you whether you want to etch or not -- whether 11:25:26
6 you want to mask or not mask the nitride and oxide
7 over line 127?

8 A Well, it refers to a means to make a
9 partial connection. That means the upper layer is
10 touching some points, but not in all points, of the 11:25:52
11 underlying layer.

12 Q Okay. Is there any other support for that,
13 other than the word "partial" or "partially"?

14 A Well, someone skilled in the art, as we
15 were discussing yesterday, will know if there are 11:26:17
16 two layers and there is an insulating layer in
17 between. We spent quite a bit of time yesterday to
18 discuss that connection is done, someone skilled in
19 the art will know that you have two layers, two
20 metal layers and an insulating layer in between, 11:26:34
21 like an insulator has been sandwiched by the two
22 metal layers, then you open contact holes; in other
23 words, depicted in the prior art.

24 Q But --

25 A That was something was well known in the 11:26:57

1 art.

2 Q Well, Professor, how do we know that,
3 according to this patent, the dielectric should be
4 left on top of the first formed part of lines 127
5 and not stripped away during the etching step? 11:27:16

6 There are two choices. Let me pause.
7 Aren't there two choices, you can put the dielectric
8 down and either leave it there or you can take it
9 away, right?

10 And you've chosen one way, and I'm saying 11:27:40
11 why is it that way instead of the other way?

12 A I mean, what do you mean by leave it there
13 or take it away?

14 Q Okay. So the question is, you're citing
15 this paragraph in the middle of column 6 to say that 11:27:54
16 there is a two-layer structure, two conductors?

17 A Right, separated by an insulating layer,
18 because in the sequence there is that layer that
19 comes in between them. There is a specific order
20 with which the layers are laid down. 11:28:08

21 Q Okay. And there will be insulator on top
22 of the bottom layer --

23 A Correct.

24 Q -- during the process of forming this?

25 Now, you advise that there is also a 11:28:23

1 masking and etching step. And it seems to me that
2 you are presuming that these lines 127 will be
3 masked so that the nitride and oxide will remain
4 there, or so that you'll just mask and etch contact
5 holes instead of striping them away completely. 11:28:44

6 And my question to you is, where does that
7 come from out of this reference?

8 MR. GIBSON: Objection; form.

9 THE WITNESS: What do you mean by striping
10 completely? 11:29:03

11 BY MR. MANZO:

12 Q Well, you said that --

13 A There's no masking step?

14 Q Well, you said that there is a masking
15 step. 11:29:11

16 A Right.

17 Q And you leave -- you put a mask over the
18 parts you want to remain before you etch. And then
19 you etch, and then you remove the mask and you have,
20 still intact, the parts that you wanted to have 11:29:22
21 remaining; is that correct?

22 A I tried to visualize a structure that -- or
23 the steps that need to occur to create what the
24 inventor here is trying to teach. And the inventor
25 is trying to teach a structure in which the two 11:29:42

1 layers are partially connected to each other.

2 The inventor does not teach that you form
3 127 where the two layers are in direct contact and
4 overlapping over the entire length of the line. So
5 I'm trying to see how one will create a structure
6 which are constantly connected.

11:30:07

7 If I understand your reasoning, you tried
8 to somehow create both the partial connection and,
9 at the same time, remove the entire dielectric. And
10 if you remove the dielectric, then the lines will
11 not be constantly connected.

11:30:29

12 Q How will they be connected, hypothetically?

13 A Well, I'm trying to understand your
14 structure. You say you remove the gate dielectric
15 completely.

11:30:46

16 So in your response that I studied it was a
17 drawing where the two metals were overlapping a
18 hundred percent over that distance of the drawing
19 that you had indicated there, and that drawing does
20 not show that the layers are constantly connected.
21 They show that they are connected over the entire
22 length of the line.

11:31:08

23 I'm trying to understand how you can remove
24 the entire dielectric and still be able to get the
25 partial connection.

11:31:27

1 Q All right. So I understand your answer to
2 mean that if you remove the entire dielectric, you
3 would not have partial connection, which the patent
4 refers to, the Shiba patent refers to at column 6,
5 lines 39 or 40, and, instead, you would have a 11:31:49
6 complete full connection between the two conductive
7 layers of lines 127; is that right?

8 MR. GIBSON: Objection; form.

9 THE WITNESS: Well, you start discussing
10 another hypothetical way of making it, and I'm 11:32:37
11 trying to understand your hypothetical way, and I
12 was asking you questions.

13 And now you're telling me I give you
14 answers, I was meaning mostly within the context of
15 a question that was asking you, what do you mean by 11:32:57
16 removing the dielectric and how that removal will
17 then satisfy the partial connection.

18 So I'm still trying to understand your --
19 what is the structures you are proposing is an
20 alternative to the structures that I have proposed 11:33:18
21 and which was well known in the art of how to
22 connect two layers separated by an insulating layer,
23 and the connection typically involves formation of
24 contact holes and establishing a contact where the
25 metal -- the upper layer will go down the hole and 11:33:44

1 touch the lower metal.

2 BY MR. MANZO:

3 Q Well, thank you for your explanation, but
4 your explanation presumes that there is insulation
5 between the two layers. And the part of the Shiba 11:34:05
6 reference that you've cited for that is not in this
7 discussion in the middle of column 6, lines 36 to
8 42, it is somewhere else, and it is talking about
9 other parts of the structure.

10 And since there is a masking and etching 11:34:30
11 step, you are presuming that the masking and etching
12 step is such that as to leave the insulator on top
13 of 17 between the two layers, and I'm suggesting
14 that maybe it doesn't work that way.

15 And all I'm asking you is what is the 11:34:50
16 support for you saying that there is insulation
17 between those two conductive layers? Because I
18 don't see it between lines 36 or -7 and 42.

19 A You make a long statement, so let me start
20 from the first aspect or first topic of your 11:35:14
21 statement. And you state, "Your explanation
22 presumes that there is insulation between the two
23 layers," so let's focus just on that part.

24 Q Okay.

25 A I read sections in -- from Shiba that list 11:35:34

1 the order with which the layers are put down, and I
2 said that following those steps, it will lead to an
3 insulating layer between the wiring formed from the
4 scanning line material and any wiring formed between
5 the data line material. And you seem to even 11:36:07
6 question that par.

7 Why you say presume? You're reading
8 differently in the specifications that I do? You're
9 questioning even the presence of the dielectric.
10 When the dielectric goes down, it goes everywhere. 11:36:28
11 It's not that it's put selectively in some regions,
12 it is not put putting everywhere. So the dielectric
13 is everywhere, on top of anything that is formed
14 from the scanning line material.

15 Q I understand that. 11:36:52

16 Now, according to what I think you said,
17 there will be a masking and etching step --

18 A Okay.

19 Q -- is that right?

20 A Yeah, so we agree that on top of the 11:37:06
21 scanning line material there is dielectric.

22 And I think we are agreeing that now there
23 will be a masking step and an etching step.

24 Are we on the same page, wavelengths?

25 Q Let's say I follow you. And my question is 11:37:24

1 really this, now we're getting to the heart of the
2 question --

3 A Okay.

4 Q -- the question is, where does the mask go?

5 I appreciate that there is masking. And 11:37:38
6 here's my point. If I want to mask over there
7 someplace to my left, it doesn't mean that I'm also
8 going to mask over here, someplace to my right.

9 And -- can we agree with that?

10 MR. GIBSON: Objection; form. 11:37:57

11 THE WITNESS: Masking step means that you
12 leave what's known as the photoresist layer, which
13 is an organic material that is photosensitive and
14 which is patterned by exposure and followed by a
15 developing step. So through that whole process, 11:38:17
16 part of the organic material, the photoresist,
17 remains and protects anything which is underlying
18 it.

19 And the region that did not contain the
20 photoresist, that will be exposed, whether it be the 11:38:33
21 chemical -- whether it be wet chemical means or dry
22 chemical means -- those regions that will not be
23 protected by the photoresist will be exposed to the
24 etching.

25 BY MR. MANZO: 11:38:47

1 Q Good. Now, what part of Shiba tells you
2 that photoresist should cover the dielectric on top
3 of the scan line material being used to make the
4 lower layer of lines 127?

5 A Well, you need to create a connection that 11:39:18
6 will -- at the end will be a partial connection.
7 That 127 -- the lower layer of 127 will be partially
8 connected to the upper layer of 127; that in the two
9 regions where the two layers overlap, the connection
10 will be a partial one. 11:39:39

11 Isn't that what is reading on column 6,
12 line 40? "The layers are partially connected to
13 each other."

14 Q Okay. So you are relying on the word
15 "partially"? 11:39:58

16 A I'm relying on the word "partially," and
17 also relying on whatever we talk yesterday from,
18 say, Sukegawa, which was another piece of prior art
19 which also been used in these proceedings to show
20 that someone skilled in the art will know that you 11:40:12
21 have two layers separated by dielectric and you want
22 to establish a connection between the two layers,
23 you -- the means to do so is to open contact holes.

24 And when doing so, you establish two
25 parallel lines that are separated by a dielectric. 11:40:39

1 Every now and then the two lines are attaching each
2 other, so the two lines have the same potential,
3 they form a lower resistance line than if you just
4 have one or the two. And Shiba says that,
5 furthermore, you also gain additional advantage, if 11:41:02
6 you say that one of the layers has a wiring defect,
7 let's say there is a particle that it creates an
8 opening, creates a discontinuity in that portion,
9 the other layer, it is at a different level, it will
10 continue carrying the signal and will bypass the 11:41:24
11 defect portion.

12 Q May I ask you also about other
13 possibilities?

14 Does the passage -- the paragraph at column
15 6, beginning at line 35 -- sorry -- 37 that you've 11:41:46
16 cited, the moreover paragraph --

17 A Yes.

18 Q -- is it possible that that means that
19 there are lines 127 formed of two different layers
20 and that they are side by side, running in parallel, 11:42:02
21 except occasionally crossing over one another?

22 MR. GIBSON: Objection; form.

23 THE WITNESS: Well, if we look at the
24 Figure 3, I don't think your statement is supported
25 by the drawings in Figure 3. 11:42:42

1 We see that all the lines of 127 originate
2 from the pad 125a, I think 125a is referred to --
3 pad 125 is referred to as inter-connecting pad.

4 And at column 6 it reads, line 5, "A first
5 wiring line 127 is drawn from the inter-connecting 11:43:28
6 pad 125a."

7 And we discussed earlier that some of those
8 lines are in dotted lines and some of the lines are
9 continuous lines. So 127, as you pointed out, it
10 refers to those lines as -- with an element which 11:43:50
11 characterizes 127, that wiring is characterized by
12 one number, 127.

13 And the process that we read on column 6,
14 line 127, the moreover passage, it says that 127 can
15 be made as a two-layer lines where the two layers 11:44:15
16 will be partially connected.

17 I cannot see any support in the drawing or
18 in the package to say that some lines are made with
19 one material and some other lines made with another
20 material. 11:44:36

21 BY MR. MANZO:

22 Q When is a --

23 A Go ahead.

24 Q May I ask a question?

25 A Yes. Go ahead. 11:44:49

1 Q When is the pixel electrode 251 made in
2 this sequence?

3 A Whatever is formed after the formation of
4 the gate dielectric, because we have information of
5 the storage capacitor element, which was described, 11:45:55
6 and I read that section earlier, and we have that
7 Figure 4 -- if you are referring to the -- to other
8 layers, can you be a little bit more specific as to
9 what layers you're referring to?

10 My answer is it is after the gate 11:46:34
11 dielectric.

12 Q Can you --

13 A After the gate dielectric, it's not quite
14 clear.

15 Q Can you tell whether it's before or after 11:46:49
16 the lower layer of 127 is established?

17 A It definitely is after the lower level of
18 127, because we see, in Figure 4, the lower level of
19 127 being -- which is made with the same material
20 and the scanning lines Yj, which are already laid 11:47:18
21 down, above that layer, the scanning line, you have
22 the gate dielectric element 211. And Figure 4 shows
23 the pixel electrode to be above the 211.

24 So, clearly, it is made after the lower
25 level of 127 has already been formed. 11:47:44

1 Q Can you tell whether it's before or after
2 the second level of 127 is formed?

3 A I cannot find any passage in the
4 specifications in the text to list the order. And
5 if you do have such passages, please point it out to 11:49:15
6 me so I will not be wasting your time.

7 Q I'll ask my colleagues to jump into that --

8 A Sure.

9 Q -- if there is a citation in Shiba that
10 they are aware of. I don't think that they are, but 11:49:34
11 we'll see.

12 Meanwhile --

13 A While your colleague is looking for that,
14 if I might make a comment in your previous question?

15 Q Yes. Which previous question? 11:50:04

16 A You, hypothetically, discussed that the
17 wirings can be formed as separate lines that run in
18 parallel, and each line may be formed in different
19 layers; is that what --

20 Q That is a hypothesis. 11:50:19

21 A Hypothesis.

22 And I said the record does not support
23 that.

24 Q Okay.

25 A And I want to point out another piece of 11:50:28

1 evidence in the record that does not support it.

2 Q Please.

3 A Sure. So if we look at Figure 6, it is one
4 we have not referred to so far.

5 Q Yes, Figure 6. 11:50:43

6 A In Figure 6 you see on the right-hand side
7 a set of parallel lines which are grouped as a
8 bracket that says "127."

9 Q I see several side-by-side lines 127.

10 A Right. And some of them are under the 11:51:08
11 sealant and some are inside of the sealant, to the
12 left of the sealant.

13 And those lines are made -- a single-layer
14 line made from the data line material, because those
15 lines are above the insulating layer 211. And they 11:51:31
16 are all grouped together.

17 If you were to have a structure where some
18 of the lines will be made by the data line material
19 and some of the structures will be made from the
20 scan line material, then the mask step, it will have 11:51:54
21 some data line -- lines and it will be -- but not
22 all of them.

23 So if we count the lines of 1 to the 7 in
24 Figure 3, and if we count the lines in Figure 6, I
25 think they are the same. 11:52:28

1 So it shows that as many lines as you have
2 in the planar section view, you have in the
3 cross-sectional view, which means that the masking
4 step for when you pattern the data line material, it
5 includes all lines.

11:52:55

6 And, likewise, if you pattern the scanning
7 line material, you pattern all lines, so then the
8 wiring 127, as shown in Figure 3 and in Figure 6,
9 they all constitute one -- cannot be referred with
10 one numeral, 127.

11:53:15

11 Q Okay. So in Figure 6 you pointed out that
12 all the lines 127 sit on top of the gate dielectric
13 or the insulator 211; is that right?

14 A That is what is shown.

15 Q Okay. And you don't see a lower layer
16 there, do you, of conductor 127?

11:53:39

17 MR. GIBSON: Objection; form.

18 THE WITNESS: Well, Shiba talks about
19 multiple embodiments and, particularly, this line
20 127, it says -- line 30 -- column 6, line 31, "the
21 first wiring line 127 can be formed in the same step
22 for forming the data lines Xi."

11:54:04

23 So that particular embodiment in Figure 6
24 depicts the embodiment that is made with first --
25 with the material of the data lines.

11:54:49

1 But further down in column 6, in line 34 it
2 says that, "further, depending on the kind of TFTs,
3 the aforementioned wiring lines can be formed in the
4 same step performing the scanning lines Yj." That's
5 another embodiment. 11:55:16

6 And continuing the same column 6, line 37,
7 we'll go into the passage that reads, "Moreover, the
8 first wiring lines 127 may be formed in the step of
9 forming the scanning lines and the data lines."

10 So someone skilled in the art will see 11:55:36
11 there are three different embodiments that are
12 disclosed by Shiba that you can make them with the
13 scan line material, the data line material or as a
14 two-layer structure that you use both materials.

15 BY MR. MANZO: 11:55:49

16 Q The wirings 127 are part of the same layer
17 or layers as 125a, I think you testified, and
18 those -- that connects to lines 123-1 in Figure 3?
19 And those, I think you said, are also a part of the
20 same layer as 751 and 731 and 121-1. 11:56:59

21 Do you recall that testimony?

22 A Well, I read you from Shiba. This is what
23 Shiba is teaching --

24 Q Okay.

25 A -- that all these elements are made from 11:57:22

1 the same metal layer.

2 Q So pad 751 will be made at the same time in
3 the same way as what you've described; is that
4 correct?

5 MR. GIBSON: Objection; form. 11:57:34

6 BY MR. MANZO:

7 Q Or put it a different way, would pad 751 be
8 made differently?

9 A Well, the pad is -- we refer to the pad as
10 a region. And in that region, like in 127 region, 11:57:56
11 you may have one layer or multiple layers; for
12 example, we see 127 have multiple layers.

13 Now, the 751 will include, as a minimum,
14 the material made by the data lines as shown here in
15 the preferred embodiment of Shiba. 11:58:31

16 Q Are you referring to a figure there or --
17 when you say "here," what do you mean?

18 A I'm looking at the passage that we read
19 earlier.

20 Q Okay. The column 6 "Moreover" passage? 11:58:48

21 A No. A little bit above that one in column
22 6, line 27 reads, "The power supply pads 731 to 738,
23 the common pad 751, the third wiring lines 121-1 to
24 121-4, the inter-connecting pad 125a, and 125b the
25 second wiring lines 123-1 to 123-4, and the first 11:59:26

1 wiring line 127 can be formed in the same step of
2 forming the data lines Xi."

3 So all those regions are formed in the same
4 step as forming the data lines.

5 Now, the "moreover" passage below in the 11:59:47
6 same column 6, it shows that the 127 can be made as
7 a two-layer structure.

8 So the thing in Shiba is that all these
9 regions are made from the data line materials, that
10 some regions, some elements, can you made as a 12:00:19
11 two-layer structure.

12 Q And in the paragraph from which you were
13 reading in column 6, do you see a reference at line
14 37 to "not increasing the number of manufacturing
15 steps"? 12:01:11

16 A I see that.

17 Q Is that important, in general, to
18 semiconductor manufacturing?

19 A Do not increase the number of manufacturing
20 steps keeps cost down. 12:01:29

21 Q So more manufacturing steps means more
22 cost; is that right?

23 MR. GIBSON: Objection; form.

24 THE WITNESS: In general, unless your
25 additional manufacturing steps improve yield or 12:01:48

1 improve performance, and they may be worth the
2 additional thing because you may make a better
3 product which you sell it at the premium, so it
4 doesn't mean that you -- ideally, if you can get
5 advantages in yield and in performance without
6 increasing the manufacturing steps, you get the best
7 of both worlds.

12:02:06

8 So, for example, the wiring structure 127
9 being a double-layer structure, it reduces the
10 defects and also increases the resistance -- sorry,
11 decreases the resistance. Excuse me. Decreases the
12 resistance.

12:02:51

13 Shiba teaches giving the signal to the
14 counter electrode is very critical, and those points
15 are looked at very -- at distances far away from the
16 terminal parts.

12:03:20

17 So having a wiring that will distribute the
18 signal to the counter electrode in such a way that
19 it will be able to modulate the potential of the
20 counter electrode fast is essential for
21 high-performance displays.

12:03:40

22 And he lists examples of different driving
23 things that can be implemented because the wiring
24 structure that he has is a low-resistance structure.

25 BY MR. MANZO:

12:04:05

1 Q Just to be clear, does this two-layer
2 structure for wiring lines, or line 127, according
3 to Shiba, result in additional manufacturing steps
4 or not?

5 A It says, "If the layers are partially 12:04:19
6 connected to each other, the wiring defect can be
7 prevented and the manufacturing yield can be
8 improved" -- are you referring to that part?

9 Q No.

10 A "The structure of the present invention, 12:04:40
11 therefore, does not increase the number of
12 manufacturing steps"?

13 Q That's the part.

14 That's at column 6, line 32, approximately.

15 A I don't believe it increases the 12:05:03
16 manufacturing steps.

17 Do you have evidence that it does?

18 Q I just wanted to see if you have that
19 understanding, Professor.

20 A It is my understanding, based on the 12:05:19
21 teaching of Shiba, the drawings and the
22 specifications and what I thought, was someone
23 skilled in the art will also understood at the time
24 of the invention that the double-layer structure can
25 be implemented without increasing complexity, 12:05:36

1 without adding additional manufacturing stems.

2 I do not see evidence in the record that
3 shows the opposite will be true.

4 Q Very well.

5 A little while ago you referred to 12:07:01
6 Figure 6.

7 A Yes.

8 Q Does Figure 6 show that the protective
9 overcoat 241 is above the lines 127?

10 A This is what is depicted in Figure 6. And 12:07:27
11 241, column 4, line 29, it specify what it is and,
12 quote, protective overcoat 241 made of silicon
13 nitride is arranged in the TFT 221 and around the
14 pixel electrode 251.

15 And that's the second insulating film. 211 12:08:23
16 is the first insulating film in the sequence of
17 fabricating this structure.

18 Q Professor, could you turn to paragraph 69
19 of your declaration.

20 Does paragraph 69 indicate that a person of 12:09:30
21 ordinary skill would modify Shiba in some way?

22 A The paragraph 61 says the person with
23 ordinary person with skill in the art can modify
24 Shiba to form pads that will include a transparent
25 conducting film, such as indium tin oxide, because 12:10:39

1 that material is well known to resist oxidation and,
2 thus, will result in reliable connection.

3 Two-layer structure has already been taught
4 by Shiba --

5 Q Yes. Go ahead. 12:11:10

6 A -- within the context of forming the wiring
7 lines 127.

8 So two-layer structures have been shown in
9 some portions of display to be advantageous.

10 Extending the teaching of Shiba, one can view the 12:11:34
11 pad 751 as a two-layer pad and use different layers
12 to gain the advantages of improved reliability.

13 Q I just want to try to understand that
14 better. Does the pad 751 have already the two
15 layers formed from the scan line material used to 12:12:16
16 make the lines Y and the data line material used to
17 make the lines X? And are you now changing one of
18 those or putting something on top of that?

19 MR. GIBSON: Objection; form.

20 THE WITNESS: Well, Shiba is teaching that 12:12:39
21 751 is a single layer and that element 127 is a
22 double layer.

23 Shiba does not say that the 751 has a lower
24 layer made of the scanning line and an upper layer
25 made of the data lines. That's something that 12:13:06

1 someone skilled in the art can implement based on
2 the teaching, but Shiba does not disclose that part.

3 BY MR. MANZO:

4 Q Okay. So how would you form the two-layer
5 pad structure, according to paragraph 69 of your 12:13:26
6 declaration? How would a person of ordinary skill
7 in the art do that?

8 A Someone ordinarily skilled in the art will
9 have a two-layer structure in 751 where the lower
10 layer is made -- still is made with the data line 12:13:54
11 material, but the upper layer is made by the indium
12 tin oxide layer.

13 Q Now, would there be dielectric on top of
14 the data line material?

15 A Yes, there is this dielectric of 241, I 12:14:15
16 believe -- yes, 241. So there will be openings in
17 that layer 241. So the pad -- so the indium tin
18 oxide can make a contact to the metal layer or, as
19 we discussed several times, there is the data line
20 material and then there is the insulating layer 241 12:15:13
21 and there is the indium tin oxide layer. So you can
22 put the 751 down, you put the 241 down, you have
23 openings, and then you put the ITO layer.

24 Alternatively, you -- so that's one way to
25 make the structure. 12:15:44

1 Q Would this require an additional step of
2 adding indium tin oxide at that location on pad 751?

3 A There is already indium tin oxide used as
4 the pixel electrodes.

5 Q Are you saying no additional step would be 12:16:12
6 needed?

7 A You asked me earlier about the order of the
8 pixel electrode, and I did not find evidence in the
9 specifications, and I asked for your help to point
10 me in that direction, at least where the ITO is 12:16:40
11 relevant to- -- to the data line material.

12 There is a layer- -- there is a pixel
13 electrode layer and there is openings in 241 that
14 are created and there is a data line material. And
15 so you have all the steps there in making the 12:17:11
16 structure.

17 Q I don't think that answers my question.
18 Are you saying that this modification to
19 Shiba to include ITO on top of the pad 751 can be
20 done without adding additional steps? 12:17:53

21 A Someone skilled in the art will conclude
22 that those steps can be made without adding steps.

23 Shiba is not clear how the pixel electrode
24 layer -- when the pixel electrode layer is formed.
25 So depending upon where the pixel electrode is 12:18:22

1 formed, you don't even -- you change nothing in the
2 process, or depending on where the pixel electrode
3 layer is formed, you change the ordering with some
4 of the -- the order with which some of the steps are
5 formed. But you not add in additional manufacturing 12:18:40
6 steps, you just simply change the order.

7 And I did not see evidence in the
8 specification. I asked for your help, and I did not
9 see whether you have a clear answer where is the
10 pixel electrode base in the teaching of Shiba in the 12:18:58
11 specifications.

12 Q Just so I understand your testimony of the
13 declaration, in paragraph 48, you said that the
14 wiring lines 127 can include a two-layer structure
15 of an auxiliary bottom line that's conductive and 12:20:35
16 you've testified that there would be dielectric on
17 top of it with openings, and then an upper
18 conductive layer formed by the data line material
19 that is partially connected through these openings
20 to the scan line material forming the lines 127. 12:21:01
21 That's what I understand from your testimony so far.

22 Is that correct -- is that understanding
23 correct?

24 A Well, the auxiliary lines at the bottom
25 will be made by the scan line material. They will 12:21:54

1 be insulating layer on top of that with openings.

2 In the second upper conductive layer they
3 will form the external connection lines that will be
4 made by the data line material.

5 Q Okay. So that's your testimony. And I 12:22:22
6 think that --

7 A This is what I described in paragraph 48.

8 Q Okay. And I think I understand your
9 testimony.

10 And then I asked you here a little while 12:22:32
11 ago whether that structure also applies to the pad
12 751, and you indicated, I thought, that it does not,
13 and you referred to the bit in column 6, I think,
14 where the patent says that the pad is made of the
15 same material in the data line material X; is that 12:23:03
16 correct?

17 A Well, paragraph 48, and the portions we
18 discussed earlier from the specifications, refers to
19 wiring lines 127 being double-layer lines. So
20 within that context there are two points I want to 12:23:33
21 make. One is that the patent is saying that it is
22 double-layer structures, consisting of the scan line
23 material and data line materials applies to 127, at
24 least this is what is disclosed in the preferred
25 embodiment of Shiba. 12:23:59

1 And the other elements, 751, 121, 125, are
2 referred to as a single-layer structure.

3 The paragraph 38 and the context in the
4 teaching of Shiba, there is something -- there is a
5 general teaching that emerges out of the 12:24:26
6 construction of 127.

7 And the general teaching of the
8 construction of 127 is that two-layer structures are
9 advantages. If you can form them without adding
10 steps and if you gain advantages, that will improve 12:24:43
11 the manufacturing yield, will reduce defects.

12 So there is a specific teaching for a
13 specific wiring, but there is also a general
14 teaching that someone skilled in the art will see
15 that can apply to maybe other structures. 12:25:05

16 The general teaching is that the structure
17 can be made, in general, with two layers. And the
18 specific teaching for making the wiring 127 applies
19 to wiring lines 127.

20 One can do that exact sequence of layers to 12:25:29
21 other parts or it can change and use different
22 layers to make other parts and use other materials
23 which already used in the manufacturing process and
24 mix and match the layers in order to gain
25 advantages. 12:25:53

1 After all, there are three layers that are
2 reported in Shiba, the three conductive layers.
3 There is the conductive layer made of the scanning
4 line material, there is the conductive layer made of
5 the data line material and there is a conductive 12:26:12
6 layer made with the transparent indium tin oxide.

7 So you can mix and match which layers you
8 want to use to make a two-layer structure in order
9 to gain some advantages in that particular region
10 that you want to implement that two-layer structure. 12:26:31

11 In forming a long wiring line, just as in
12 127, to provide signals to these counter electrode
13 pads, which are distributed along the periphery, far
14 away from the common pad 751, it makes sense, as
15 Shiba specifically disclosed, that that wiring has 12:26:55
16 been made with the data line and the scanning line
17 materials. But the general teaching of making
18 two-layer structure is there.

19 So in the common pad region, someone
20 skilled in the art will see that you can maintain 12:27:17
21 the data line material from Shiba and introduce the
22 pixel electrode above it in order to gain advantages
23 in corrosion protection.

24 Q Would a person ordinarily skilled in the
25 art want to consider and weigh the disadvantages, if 12:28:25

1 there are any, of a process sequence in which the
2 indium tin oxide is added on top of pad 751 after
3 the formation of the protective overcoat 241?

4 MR. GIBSON: Objection; form.

5 THE WITNESS: And what are these 12:29:29
6 disadvantages?

7 BY MR. MANZO:

8 Q Well, if there are any, would they have to
9 be weighed?

10 MR. GIBSON: Objection; form. 12:29:52

11 THE WITNESS: I did not see any
12 disadvantages. If you have see something, if you
13 have evidence of -- that there is a disadvantage,
14 can you elaborate so I can answer your question?

15 BY MR. MANZO: 12:30:02

16 Q Well, Professor, I'm not the expert here
17 testifying. You're the expert at this, and I'm just
18 trying to understand and explore the testimony
19 you've given and the consequences of it.

20 So if I ask some dumb questions, I'll hope 12:31:03
21 that you'll forgive my ignorance. Maybe my
22 questions are not sensible and maybe they are, but
23 together we are trying to arrive at the truth, so
24 let me press on.

25 A Let me comment that, first, your questions 12:31:44

1 are not, what you say, dumb questions, I do not find
2 your questions to be dumb. And I agree with you
3 that we need to derive to the truth of the matter
4 and I understand that you may also have experts that
5 help you in understanding those structures that may 12:32:10
6 have more knowledge and skill than you, as an
7 attorney, may have on the subject matter. So I
8 think some of your questions may be guided by
9 information you receive by the experts, so I am --
10 in some of my questions towards you, I'm looking for 12:32:34
11 things that you or your colleagues or your experts
12 see and read in the specifications so then I can
13 respond and provide comments to those evidence that
14 they maybe see.

15 And it was my testimony earlier that I do 12:32:57
16 not see any disadvantages. If you have any
17 information for such disadvantages that you have
18 formulated yourself or your colleagues or your
19 experts, please point it out to me so we can discuss
20 them and then we'll derive to the truth, as you 12:33:13
21 said.

22 Q Well, let me try.

23 Looking at Figure 4 of Shiba, we have a
24 gate dielectric layer 211 that you've pointed out,
25 right? 12:33:49

1 A Yes.

2 Q Now, I see number 211 at the right-hand
3 side of Figure 4. Let me just ask one question for
4 now before we break. Can you tell how far to the
5 left in Figure 4 that layer 211 extends? 12:35:26

6 A From the drawing?

7 Q Yes. Or, if you want to consult any other
8 part of the specification, that's fine also.

9 A Well, if you have evidence that will help
10 me, we'll save time. If you want to direct me to 12:36:00
11 something, to some point you would like to make --

12 Q Well, frankly, you know, I almost need a
13 microscope or magnifying glass to tell this.

14 I just wonder if, in your expertise, maybe
15 you know the answer and can help me with that. 12:36:18

16 A Well, Figure 4 is kind of crowded picture,
17 and 211 is labeled on the right. And you asked me
18 how far it extends to the left, if I understand your
19 question?

20 Q Right. Yes. 12:36:41

21 A In my analysis I use Figure 6 where it is a
22 bit more clear where 211 is on -- with respect to
23 the sealant. I presume you would like to find out
24 where 211 is relevant to the sealant, because the
25 sealant is towards the left. Is that what you're 12:37:13

1 trying to --

2 Q Yes.

3 A And I can see it clearly in Figure 6. And
4 I would assume that apply to the other side.

5 Q In Figure 6, just to be clear, the display 12:37:32
6 region is on the left-hand side of Figure 6 and the
7 terminal portion is on the right-hand side? Do I
8 have that correct?

9 A Figure 6 is one of those sides that does
10 not have a terminal portion. 12:37:48

11 Q Oh.

12 A As you see from Figure 1, the terminal
13 portions are on two sides, and there are two other
14 sides that did not have terminal portions. I
15 believe that applies to the side that does not have 12:38:02
16 a terminal portion.

17 Q Okay. So to rephrase, in Figure 6 does the
18 left-hand side of the sealant represent the
19 display -- part of the display area and -- let's
20 just end the question there. 12:38:26

21 Perhaps that's a little unartful. Let me
22 rephrase it.

23 In Figure 6, is the display area generally
24 to the left of the sealant 113?

25 A By "display area," I presume you are 12:38:42

1 referring to the array where you have the pixel and
2 the electrodes, and the answer is, yes, it is to the
3 left of 113, and you can see where the two
4 substrates, 200 and 500, because the sealant 113
5 that contains and seals the liquid crystal that is 12:39:06
6 the -- within the display area.

7 Q Okay. So based on that, you've indicated
8 that Figure 6 shows the dielectric 211 extending
9 from the array area of the display area beyond the
10 sealant to a region outside the sealant, yes? 12:39:43

11 A That's correct.

12 Q And would that tell you that in Figure 4 of
13 the same orientation or configuration for that
14 region 211, dielectric 211 persists or exists?

15 A I think it is shown in Figure 4. 12:40:15

16 Q I'm sorry. Did you say, "I think it is
17 shown in Figure 4" or did you say "I think it is so
18 in Figure 4"?

19 A "It is shown."

20 Q Okay. 12:40:58

21 A Earlier in this questioning you said that
22 you had trouble seeing 211 to the left, and then I
23 refer you to the Figure 6, which I said would
24 equally apply to Figure 4. And then we agree that
25 it is shown clearly in Figure 6. And I'm looking at 12:41:16

1 Figure 4. Without the help of magnifying lens, I
2 believe it is shown that it is there and extends all
3 the way out to the edge.

4 Q Okay. Well --

5 A And it is below element 751. 12:41:40

6 MR. MANZO: Maybe we can stop here for
7 lunch.

8 THE VIDEOGRAPHER: This is the end of tape

9 1. We are off the record at 12:41 p.m.

10 (Recess.) 01:29:32

11 THE VIDEOGRAPHER: This is the beginning of
12 tape 2. We are back on the record at 1:30 p.m.

13 BY MR. MANZO:

14 Q Professor, did you discuss your testimony
15 with anybody over the lunch hour? 01:30:21

16 A No.

17 Q Okay. We were talking, before the recess,
18 about including a transparent conductive film, such
19 as ITO, for the top layer of pad 751.

20 Do you remember that? 01:31:00

21 A Yes.

22 Q And I believe you rely on Sukegawa for that
23 motivation; is that correct?

24 A Yes.

25 Q I just want to make clear that we're in 01:31:17

1 agreement that Shiba does not refer to using a
2 transparent conductive layer for this specific
3 purpose; is that right?

4 A Shiba is teaching wirings that can be made
5 or structures that can be made as two layers, where 01:31:42
6 each layer has been formed from a different
7 material. The particular embodiment discussed in
8 Shiba in the common pad region, 751, it depicts only
9 a single layer, which is made of the material of the
10 data lines. 01:32:15

11 Q Are the data lines and the scanning lines
12 made of different materials or are they the same
13 material?

14 A Made at two different times. It is two
15 different deposition process, and they are separated 01:32:38
16 by a dielectric layer 211, as we discussed earlier.

17 I do not recall, and please help me if you
18 recall, where the materials of the data lines and
19 scanning lines are referred explicitly what they are
20 in Shiba. 01:33:43

21 Q Maybe I can rephrase, whether you recall
22 any indication in the Shiba patent of whether the
23 data lines and the scanning lines are different in
24 material.

25 A My recollection and a brief scan, they are 01:35:47

1 referring them as scanning line and a data line, but
2 do not go into detail what material constitutes each
3 line.

4 If you are asking me in general --

5 Q Let me ask you in general. 01:36:04

6 A -- what material are used, they can be the
7 same or they can be different.

8 For example, in Sukegawa that I'm using
9 there is specific mentioning of what material they
10 can be used, and they also provide a list of 01:36:36
11 additional materials of -- and the list includes
12 chromium, molybdenum, aluminum, tantalum, to name a
13 few.

14 Q I understand your answer, but focusing
15 specifically on Shiba, then you're not aware of any 01:37:21
16 specific teaching in Shiba, are you, of using
17 different materials for the X lines and the Y lines?

18 A My recollection, and I cannot find -- I
19 cannot find any mentioning right now what are the
20 materials for the scanning lines and data lines. 01:37:48

21 I see a reference to another component, the
22 light shielded matrix layer, which is used to
23 make -- which is made from chromium on the other
24 substrate, the 500 substrate, but I do not see a
25 reference on material for the scanning lines and 01:38:16

1 data lines.

2 So I cannot tell you if they are the same
3 or different or what is the material based on Shiba,
4 unless you have portions that you want to guide me.

5 Q I don't have an indication myself. 01:38:34

6 Is there any suggestion that the data lines
7 or the scanning lines are made of ITO in Shiba?

8 A No. They are not -- they are not referred
9 as made of ITO. ITO, it refers -- specifically for
10 the use of the pixel electrode and the counter 01:39:02
11 electrode.

12 In general, you will not form scanning
13 lines and data lines for a large display. And I
14 believe this is a 14-inch diagonal display. You
15 will not form long lines, such as the scanning lines 01:39:35
16 or data lines, using ITO. Those long lines will be
17 resisted.

18 Q Okay.

19 A In Shiba it mentions somewhere that ITO is
20 a high-resistance material and only use it for the 01:40:06
21 counter electrode and the pixel electrode.

22 So you not form long lines with ITO, but
23 you can certainly form a second layer, because in
24 that case you only have to transverse the thickness
25 of the layer. You do not -- actually, the length 01:40:37

1 that you're transversing through that layer is very,
2 very small.

3 And the cross section of that area will be
4 large, because it will be the cross section of the
5 sum of all the openings in that area. 01:40:58

6 Q All right. So do you agree that the only
7 mention of transparent conductive layer in Shiba is
8 as pixel electrodes 251?

9 A And as a counter electrode 541, column 4,
10 line 42. 01:41:47

11 Q Anything else?

12 A Not in this preferred embodiment, not in
13 this embodiment.

14 Q Well, I don't mean just in this embodiment.
15 I'm talking about in the whole patent. 01:42:14

16 A I mean, in the embodiment described in the
17 specifications. The patent provides a description
18 of certain embodiments. And out of that examples,
19 there is a teaching that is conveyed to the persons
20 of ordinary skill in the art, and that teaching go 01:42:45
21 beyond the specific details and specific structures
22 used in the specific -- in the particular
23 embodiments used to illustrate.

24 Q Okay. So you don't find any such teaching
25 in the description of embodiments or anywhere else 01:43:12

1 in this patent?

2 A What teaching?

3 Q Of using a transparent conductive layer for
4 anything other than a pixel electrode or the
5 electrode 541, the counter electrode; is that right? 01:43:37

6 A Well, what I found is that in -- there are
7 three conductive layers. One conductive layer is
8 the transparent pixel electrode that is mentioning
9 to be used as the pixel electrodes and the counter
10 electrodes. But I also found -- find, and someone 01:44:19
11 skilled in the art also finds, the teaching that you
12 can use multiple layers out of these three layers,
13 and there is a specific example between two such
14 layers that you can make a double-layer structure
15 using the existing conductive layers. 01:44:50

16 So though a specific embodiment -- there is
17 no specific embodiment that utilizes the pixel
18 electrode -- sorry -- utilizes the transparent
19 conductive layer specifically for other purposes,
20 the general teaching of combining existing layers to 01:45:12
21 form conductive structures is there.

22 And in light of other prior art, such a
23 combination of layers will be obvious.

24 Q Excuse me for a second.

25 There is so much that we covered yesterday 01:47:59

1 about Sukegawa, that it would be just covering the
2 same ground over and over again, which I don't think
3 we want to do.

4 If we can use yesterday's testimony on this
5 topic, it will shorten this deposition a lot. 01:48:18

6 MR. GIBSON: I don't think you need to ask
7 the same questions again. I don't have any issue
8 with that. I assume that we'll have the same
9 ability when we take your experts on these too.

10 MR. MANZO: Right. 01:48:36

11 MR. GIBSON: With that understanding, I
12 think you can use any of the questions from
13 yesterday relating to Sukegawa in this petition as
14 well, with the understanding we'll have the same
15 ability to do that. 01:48:48

16 MR. SCHLITTER: We'll be accommodating.

17 MR. MANZO: Okay. Thank you.

18 Q Now, do you remember Sukegawa, Professor?

19 A I do.

20 Q And just to refresh, Sukegawa, in Figure 01:49:24
21 1B, for example, shows that the transparent
22 conductive layer 8 is directly on top of the upper
23 metal layer wiring 7, right?

24 A Yes. May I have Sukegawa reference?

25 Q There is the figure. 01:49:56

1 A Are you planning to cover that --

2 Q Here is a copy of Sukegawa patent that was
3 marked as Exhibit 1005 in this proceeding.

4 MR. GIBSON: Thank you.

5 BY MR. MANZO: 01:50:12

6 Q And my question was just to refresh your
7 recollection, I think, that 8 is directly on top of
8 7, as shown in Figure 1B.

9 A 8 is laid over 7.

10 Q Okay. Now, if a person of ordinary skill 01:50:47
11 in the art were to modify Shiba, in light of
12 Sukegawa, to provide a transparent conductive layer
13 over the common pad 751 of Shiba, would the ITO be
14 provided -- or would the transparent conductive
15 layer be provided directly on the common pad 751? 01:51:19

16 A Well, as we discussed quite extensively
17 yesterday, on top of the layer 7 there are two
18 layers, 8 and 9. One is the transparent conductive
19 layer and the other is the insulating layer 9.

20 There are two and only two possible ways 01:51:49
21 that one can lay down those films on top of 7.

22 You can put 8 to touch 7 and 9 over 8 or
23 you can put 9 above 7 and 8 above 9.

24 So if one wants to take those two
25 processing options and import those in Shiba to 01:52:22

1 modify Shiba terminal pads, common pads, 751, they
2 can be modified in any one of those two ways. I
3 don't think it's been limited to one or the other
4 because the goal is to have the ITO layer be the
5 layer that will be in between the flexible printed 01:52:57
6 circuit board and the external connection line.

7 Whether you put 8 on top of the external
8 connection line and then you have the passivation
9 layer and then form the opening or vice versa, you
10 have the passivation layer, form the opening and 01:53:24
11 then put the transparent conductive layer, to
12 someone skilled in the art, both options will be
13 obvious and whichever they choose to do, they will
14 be equally valid for the particular embodiments that
15 they wish to -- particular products that they wish 01:53:42
16 to make.

17 Maybe there are some specific reasons for
18 that particular product to choose one or the other,
19 but they are equally valid -- they are equally sound
20 approaches, and they are both obvious. 01:54:01

21 Q Okay. I understand. Is there anything in
22 Sukegawa that suggests flipping the order of layers
23 as between 8 and 9 with respect to layer 7?

24 MR. GIBSON: Objection; form.

25 BY MR. MANZO: 01:54:38

1 Q I'll rephrase the question.

2 Is there anything in Sukegawa that suggests
3 that the person ordinarily skilled in the art could
4 deposit layer 9 directly on top of layer 7 and then
5 put transparent conductive film 8 on top of 9, 01:55:16
6 presumably after 9 were etched? Is that actually
7 taught in Sukegawa?

8 A Well, you see that teaching when you have
9 to connect 2 to 7 and you have 3, which is
10 insulating layer in between. 01:55:46

11 So in connecting 2 and 7, and you have an
12 insulating layer in between, you opening the contact
13 holes and you establish regions where the upper
14 layer will touch the lower layer.

15 So if you have, again, two layers, an 01:56:20
16 insulating and a conducting, that you want to lay
17 over another conducting layer, isn't that obvious in
18 light of the underlying structure, namely, between
19 2, 3 and 7, isn't that structure similar to 7, 8, 9,
20 flipping the sequence of the orders and putting the 01:56:49
21 opening -- and doing the etching to form the opening
22 first versus last?

23 They are teaching in Sukegawa -- how to
24 connect lines, two conducting lines, with an
25 insulating layer in between is within Sukegawa, and 01:57:13

1 that's no different connecting 7, 8 -- combining 7,
2 8 and 9.

3 I did not recall if the claims in Sukegawa
4 are broad enough that it can cover both embodiments.

5 Q In Sukegawa, are layers 2 and 7 made of the 01:59:16
6 same material?

7 A In the detailed description of the
8 preferred embodiment, it reads -- on column 4, line
9 10, it reads, "a chromium film is an opaque
10 conductive film that is deposited to a film 01:59:59
11 thickness of 149 nanometer on the entire subsurface
12 of the glass substrate 1 by spattering process
13 followed by being patterned to form a lower layer
14 metal wiring 2."

15 So there is a specific disclosure that the 02:00:18
16 lower wiring is chrome. And then further down in
17 column 4 on line 46 it reads that another chromium
18 film is opaque conductive film, is deposited to a
19 film thickness of 140 nanometers so as to cover the
20 inter-layer insulation film 3. 02:00:51

21 So in this preferred embodiment, they are
22 both described to be as chromium. That is another
23 section on column 8, at line 55 that it reads,
24 "While the present invention has been explained with
25 reference to the preferred embodiment, the invention 02:01:25

1 is not restricted only to such embodiments, but
2 various modifications are possible within a range
3 not departing the purpose of the present invention.
4 For instance, the lower layer metal wiring and the
5 upper layer metal wiring are made of chrome, but, 02:01:52
6 instead, a single layer or a composite layer, such
7 as made of aluminum, tantalum, molybdenum and
8 tungsten may be used. Further, the materials for
9 the lower layer metal wiring and the upper layer
10 wiring may not always be identical." 02:02:18

11 So this paragraph in this section in the
12 first sentence it says that multiple -- that
13 variations and modifications can be implemented, and
14 switching the order with which 8 and 9 falls within
15 the scope of Sukegawa will result in the same 02:02:57
16 benefits.

17 And the second sentence gives an example
18 that is referring to switching the materials used
19 for the wirings 2 and 7, or changing the materials
20 or -- referring to the selection of materials that 02:03:31
21 could be used to form wirings 2 and 7.

22 Q Thank you. Just to make sure that I
23 understand you, it is your testimony that switching
24 8 and 9 relative to 7 is suggested by the first
25 sentence in column 8 beginning at line 55? Is that 02:04:05

1 what you said?

2 A I said the invention is not restricted only
3 to such embodiments.

4 So there are several embodiments described
5 in Sukegawa, and this sentence say that the 02:04:25
6 invention is not restricted only to such
7 embodiments, but various modifications are possible.

8 So it is my testimony that someone skilled
9 in the art, switching the order of 8 and 9, it will
10 have been obvious, particularly because making a 02:04:49
11 connection between 8 and 7 with the layer 9 in
12 between 8 and 7, you simply replicate the process
13 sequence that is used in connecting 2 and 7 where 3
14 is in between.

15 Q Forgive me if I'm taking a bit of time to 02:06:50
16 formulate my next question, but I'm skipping a lot
17 in light of yesterday's testimony.

18 MR. GIBSON: That's always appreciated.

19 THE WITNESS: Let me take a one-minute
20 break. 02:07:09

21 MR. MANZO: Sure.

22 THE VIDEOGRAPHER: Off the record at 2:07
23 p.m.

24 (Recess.)

25 THE VIDEOGRAPHER: Back on the record at 02:14:36

1 2:14 p.m.

2 BY MR. MANZO:

3 Q Professor, I invite your attention to the
4 '204 patent.

5 I may have asked you similar questions 02:15:11
6 yesterday, but if you look at Figures 4A and 4B, do
7 you see that the ITO 114 is not covered anywhere by
8 the resin inter-layer film 113?

9 A I see that in Figure 4A and 4B.

10 Q Is there any advantage to that that you 02:15:56
11 recognize?

12 A Such as?

13 Q Well, I'm just trying to understand what
14 you recognize.

15 A As I said, there are two layers that need 02:16:38
16 to be placed over 403. One way is to put the resin
17 inter-layer film first, then create -- form the
18 openings, and then put 114, as shown here.

19 Q Would a person ordinarily skilled in the
20 art in 1997 have recognized an advantage to doing it 02:17:19
21 one way or the other way?

22 A Figure 4A shows us one way and Figure 1B in
23 Sukegawa they are referring shows a different way.
24 These are the two possible ways to implement them.

25 It is my opinion, and reading the 02:17:51

1 specifications of both patents, neither inventor
2 wanted to limit to one or the other. They described
3 a particular embodiment.

4 Now, what someone skilled in the art
5 chooses to do will depend upon a lot of details that 02:18:13
6 will be applicable to the selection, to the flow in
7 manufacturing lines that they have.

8 As I said a number of times, there are only
9 two options, and inventors of one do it one way in
10 their preferred embodiments, and perhaps inventors 02:18:41
11 of a later patent choose to do different from the
12 earlier patent, maybe perhaps to show it is
13 different, but I tried to explain that someone
14 skilled in the art, both ways are obvious.

15 So even before the '204, both ways were 02:19:08
16 obvious. And the '204, as I said -- within the
17 context of '413 yesterday, the '204 does not claim
18 any advantages for that part. '204 is not
19 describing the advantages of having the ITO on top
20 of the inter-layer resin film, it doesn't try to 02:19:36
21 make that as a claim invention.

22 If you read the specifications, and I'm
23 sure you have read it a number of times, over many,
24 many columns, the inventors discuss these adjustment
25 layers, what materials, what shape, what to extend, 02:20:00

1 how to connect them, or to form one continuous, so
2 there are a lot of discussion about the adjustment
3 layers. So -- and as far as this terminal
4 connection, there is only a very brief reference to
5 it, and that is in example 3 in column 8 in line 53 02:20:24
6 to 55 that reads, "Referring to Figure 4A, the
7 external connection lines 403 are electrically
8 connected to an FPC (flexible printed circuit) 107
9 through contact holes provided in the resin
10 inter-layer film 113 through ITO (indium tin oxide) 02:21:00
11 film 114," period. That's the only reference I have
12 found. And guide me if there are others that refer
13 to this connection.

14 And in these four brief sentences here --
15 four brief lines, in this entire sentence, I do not 02:21:25
16 see any claim advantages. And even the level of
17 details is -- of how to form it is not explained.
18 There is no order with what the layers are put down,
19 it doesn't list that you have to list -- put down
20 the resin inter-layer film first and the indium tin 02:21:53
21 oxide on top of it.

22 That description, that language, as I said
23 yesterday and I'm saying it again now, it is broad
24 enough that covers both implementations of
25 connecting ITO and the layer 403. 02:22:19

1 Perhaps the inventors wanted to have it
2 broad enough so it would cover both embodiments, but
3 to someone skilled in the art, that is broad and
4 covers many embodiments.

5 Similar to Sukegawa does not disclose the 02:22:52
6 other embodiments, that the inventors of '204 didn't
7 choose to create an embodiment like the one in
8 Figure -- like the one in Figure 1B of Sukegawa.
9 Choose to have one, but then have enough -- have a
10 language which is broad enough that cover both. 02:23:17

11 I'm not expert in writing patents. I don't
12 know what the advantage or disadvantage of broad
13 language, but that's the only reference I found for
14 that particular connection.

15 Q Thank you. 02:23:36

16 Looking a little more at Sukegawa and the
17 Figure 3 pages, Figures 3A through E, in Figure 3D
18 would you agree that the -- I think you agreed
19 yesterday that the sealant is between structure 100
20 and structure 200. 02:24:38

21 A The edge of 200.

22 Q Okay. And that would be to the left of the
23 left edge of the tape carrier package 300, correct?

24 A Correct.

25 Q Would you agree that the tape carrier 02:25:02

1 package 300 could not extend between structures 100
2 and 200, for at least the reason that it's much too
3 thick?

4 A I do not know what you mean by the reason
5 at least it is too much thick. 02:25:29

6 Q That the tape carrier package 300 is much
7 too thick and it would introduce a very large gap
8 between 100 and 200.

9 A The tape carrier package 300 comes down
10 onto 100 after 200 already has been formed. So the 02:25:54
11 sequence of which comes first is very specific. You
12 fabricate the wirings and the transistors on 100,
13 you bring 200, you seal it, you fill it with liquid
14 crystal, and then you build 300.

15 By the time 300 comes to -- and applied 02:26:22
16 onto 100, 200 has already been formed.

17 Q Okay. Now, looking at Figure 3E, I invite
18 your attention to the space marked 14 between the
19 tape carrier package parts 31 on the right side of
20 14 and the structure on the left side of 14. 02:26:55

21 And do you see that the upper layer wiring
22 7 has been removed in the region 14?

23 A That is another embodiment in Sukegawa, and
24 I did not rely on that embodiment for my analysis.
25 But I see in this embodiment that you are referring 02:27:20

1 in Figure 3 what you just described.

2 Q Would that normally be done by an etching
3 step before layer 8 is deposited?

4 A You're asking me the details of fabricating
5 the embodiment shown in Figure 3? 02:27:57

6 Q Yes. Just with regard to removing that bit
7 of the upper metal layer 7 in that particular spot.

8 A For building that particular embodiment, it
9 is obvious that if you want to add a layer and
10 remove portions of it, you do that before you cover 02:28:39
11 it by another layer, so the answer is yes.

12 Q Okay. Now, as between Figure 2C, about
13 which you did testify in your declaration, comparing
14 Figure 2C and Figure 3E, assuming that all the
15 dimensions are the same and all the materials are 02:29:09
16 the same, please make those assumptions, does
17 Figure 3E present the higher resistance between the
18 copper foil 31B and the left side of layer 2?

19 MR. GIBSON: Objection; form.

20 THE WITNESS: What are you referring to? 02:29:50
21 Left side of layer 2?

22 BY MR. MANZO:

23 Q The part on the left side of the drawing,
24 the left side of 2.

25 A Okay, the end -- the far left of the 02:30:03

1 drawing?

2 Q Yes.

3 A At the end.

4 Q At the metallic layer or the wiring layer

5 2. 02:30:13

6 MR. GIBSON: Objection; form.

7 BY MR. MANZO:

8 Q Well, Professor, do you understand what I'm
9 asking?

10 A No, I think I understand. Don't worry, I 02:30:41
11 think I understand what you're asking.

12 Q Okay.

13 A I just want to make sure I didn't
14 misunderstood anything.

15 If one compares Figure 2C and Figure 3E, 02:30:55

16 and assuming all the dimensions are identical, as
17 you highlighted, and we measure the resistance
18 between the flexible printed circuit board and the
19 far left of wiring 2 in Figure 3 and compare that to
20 the far left of Figure 2C, Figure 2C will have a 02:31:43
21 lower resistance.

22 Q Is that because part of the upper metal
23 wiring has been removed?

24 MR. GIBSON: Objection; form.

25 THE WITNESS: The two wirings in Figure 2C 02:32:00

1 are forming a parallel path for the signal to go, so
2 you have element 7, what is continuing to the left
3 without any gaps, and that will have a lower
4 resistance compared to the Figure 3E where a portion
5 of the 7 has been removed and you only have 8, which 02:32:37
6 is known to have a lower resistance than 7.

7 BY MR. MANZO:

8 Q Thank you.

9 A But, as I said, I did not use Figure 3 in
10 my analysis, I used Figure 2C in my analysis. 02:33:05

11 Q Yes. Thank you.

12 A And what you just described, as you
13 admitted, a double layer structure to the left of
14 the flexible printed circuit board, it creates a
15 lower resistance structure, because I think there 02:33:33
16 was a discussion in one of the responses that said
17 that that part does not create any -- does not have
18 any effect from the resistance.

19 And these discussions that we have, it is
20 good to clarify that we both agree that the 02:33:50
21 resistance to the left of the flexible printed
22 circuit board is lower by having the two wires
23 running parallel.

24 Q Well, thank you. I thought that my
25 questions were just questions rather than testimony 02:34:48

1 on my part.

2 But that's something that counsel for the
3 petitioner can talk to you about, after the
4 deposition.

5 MR. GIBSON: Not during the deposition. 02:35:08

6 THE WITNESS: I think we are all here to
7 clarify the records.

8 BY MR. MANZO:

9 Q Professor, in making a liquid crystal
10 display device, are there technical reasons why a 02:36:34
11 person ordinarily skilled in the art would want to
12 avoid covering indium tin oxide with a protective
13 layer?

14 A What do you mean by "technical reasons"? I
15 mean process compatibility reasons or performance of 02:37:35
16 the system reasons, or you group them all into one
17 broad category?

18 Q I don't want to restrain your answer in any
19 way by narrowing the scope of your answer.

20 A I'm trying to understand the scope of your 02:38:01
21 questions.

22 I'm not aware of technical reasons of
23 covering ITO with an insulating layer, will that
24 create problems as far as compatibility with the
25 processing steps. 02:38:25

1 You can coat an ITO layer with a
2 passivation layer.

3 In the pixel electrode region, that what
4 used to be the case, it used to be that the ITO
5 electrode was covered by a passivation layer. 02:38:43

6 I believe in some of the earlier
7 implementation of the active matrix liquid crystal
8 displays, that in those displays, the voltage you
9 had to apply on the pixel electrode to create a
10 certain twist of the liquid crystal was high because 02:39:16
11 the twist of the liquid crystal was a function of
12 the strength of the electric field. And by having
13 the pixel electrode lower than the passivation
14 layer, increase the -- increase the layers between
15 the ITO and the counter electrode. You have the gap 02:39:46
16 and then you also have the passivation layer, so the
17 electric field was lower.

18 To reduce the voltage and, hence, to
19 increase the electric field people either start
20 removing the passivation layer by creating an 02:40:11
21 opening on the pixel electrode or by flipping the
22 order and putting the pixel electrode on top of the
23 passivation layer.

24 That what comes in my mind at the end of
25 these two long days is technical reasons and 02:40:32

1 advantage/disadvantage, putting them on top of each
2 other, it refers to the electric field on top of a
3 pixel electrode in the array and how that's related
4 to the voltage of the -- that it is -- the electric
5 field, how the electric field is related to the 02:40:58
6 voltage you put to the pixel electrode, and I
7 believe that is mentioned in one of the patents that
8 are used in some of the other inter partes that have
9 used. I don't recall exact which one now, but I
10 think that's what it was referred to. 02:41:20

11 Q Okay.

12 A If you have something else in particularly
13 that you want to do, please relate more specific and
14 I will remember.

15 Q I think you already answered this, but you 02:41:39
16 said that the protective layer can be placed over
17 the ITO?

18 A In the pixel electrode region, there could
19 be a protective layer on top of the ITO. That
20 protective layer will reduce the electric field that 02:42:01
21 will go. So either one has -- if you want to
22 operate the lower voltages, lower power, you either
23 have to create an opening on top of the pixel
24 electrode and remove that dielectric or put the ITO
25 on top of the dielectric. 02:42:28

1 Q What about the strength of the composite in
2 terms of one material adhering sufficiently well to
3 the material below it?

4 MR. GIBSON: Objection; form.

5 THE WITNESS: Are you talking about the 02:42:56
6 passivation layer, like passivation layer, say, 9 in
7 Sukegawa?

8 BY MR. MANZO:

9 Q Yes.

10 A Well, like depending on like 9 adhering 02:43:09
11 better to ITO or ITO adhering better to 9? I don't
12 quite understand your question.

13 Q That's fine. We'll just move on.

14 In Sukegawa is it true that to avoid a risk
15 of corrosion, Sukegawa uses double coverage over the 02:43:38
16 upper level wiring 7, where the double coverage is
17 the transparent conductive film 8, together with the
18 protective insulation film 9?

19 A In the parts of 7 that are not exposed in
20 order to make a contact to the flexible printed 02:44:25
21 circuit or be used for testing, are you referring to
22 that portion, the portion which is to the left of
23 the left opening or the vertical edge of the left
24 opening?

25 Q Yes. 02:44:47

1 A Yeah, both layers are used for protection.

2 Q Yes, okay. Thank you.

3 A But reversing the order will equally
4 provide both layers in that region.

5 Q Well, do you agree that Sukegawa discloses 02:45:51
6 that the transparent conductive film 8 needs to be
7 formed directly on top of the upper metal layer
8 wiring 7 in order to avoid corrosion?

9 MR. GIBSON: Objection; form.

10 THE WITNESS: 8 needs to be formed above 7, 02:46:25
11 but whether 8 is directly above 7 or you have 9 in
12 between 7, I do not find any evidence in Sukegawa to
13 say that one is better than the other one and that
14 one should be avoided in favor of the other.

15 If you do have that, please guide me to 02:46:50
16 that part and I will remember it.

17 BY MR. MANZO:

18 Q I'm not aware of Sukegawa discussing the
19 option of putting 9 directly on top of 7, and that
20 the only disclosure I'm aware of in Sukegawa is that 02:47:18
21 the ITO 8 is on top of the wiring 7.

22 Are you aware of any other specific
23 affirmative teaching in Sukegawa otherwise?

24 A I think I read the part in column 8, line
25 starting at 55, that "while the present invention 02:47:57

1 has been explained with reference to the preferred
2 embodiments, the invention is not restricted to such
3 embodiments, but various modifications are possible
4 within the range not departing the purpose of the
5 present invention." 02:48:17

6 So that would have been one set of choice
7 that one could form.

8 Q Where does that sentence say that you can
9 put 9 on top of 7?

10 A It says, "various modifications are 02:48:49
11 possible."

12 Q But it doesn't say what they are.

13 A It lists one example as far as the
14 visualization, so rely on what someone skilled in
15 the art will consider whether certain modifications 02:49:12
16 will become obvious in light of the teachings in
17 Sukegawa.

18 For example, Sukegawa teaches that layers 8
19 may have pinholes and layers -- and pinholes in
20 layer 8 may lead into corrosion of the underlying 02:49:40
21 layer 7.

22 So if we put 9 directly above 7, and 8
23 above 9 and create the openings, that will be one
24 way to remove the effect of the pinholes in 8 from
25 the effect of 7. 02:50:17

1 Q Well, that may be one possibility, but
2 Sukegawa actually does something different, doesn't
3 he or they, if you know?

4 A Again, in the particular embodiments -- in
5 the particular embodiments that he lists, but to 02:50:34
6 someone skilled in the art, other modifications may
7 also be obvious.

8 And I discussed earlier that having 9 above
9 7 and 8 above 9, it will simply duplicate the
10 structure that is listed below, namely the 02:51:03
11 connections between 2 and 7.

12 Q Okay. But just to make perfectly clear, do
13 you agree with me that there is no figure that shows
14 that in Sukegawa?

15 A The figures list specific embodiments in 02:51:18
16 the paragraph I read --

17 Q We'll get to the text next. I just want to
18 ask you about the picture first.

19 So do you agree that there is no picture
20 showing this change in order? 02:51:39

21 A No, the pictures list specific embodiments,
22 and that's a different embodiment.

23 Q All right. Now, turning to the text of
24 Sukegawa, do you find a specific suggestion beyond
25 column 8 saying you can make modifications where it 02:52:01

1 says one of the modifications you can make is to put
2 9 on top of -- sorry, you can put 8 on top of 9? Is
3 that anywhere in here specifically?

4 A It has been two long days, so if you give
5 me time, I will read it again to find out supporting 02:52:29
6 evidence. And I have to reframe my mind again to
7 the claims if they suggest that part.

8 If you want me to look at it again, I will
9 take the time to look at it again. I --

10 Q Sure. That's fine. How long would you 02:52:57
11 like?

12 A I don't know what is my mental capability
13 right now, but, I don't know.

14 Q Should we take a recess while you do this
15 review and come back in a few minutes? 02:53:27

16 A Sure.

17 Q Okay.

18 THE VIDEOGRAPHER: Off the record at 2:53
19 p.m.

20 (Recess.) 02:53:34

21 THE VIDEOGRAPHER: Back on the record at
22 3:13 p.m.

23 BY MR. MANZO:

24 Q So, Professor, have you found that specific
25 citation, if there is one? 03:13:33

1 A I found several sections in which Sukegawa
2 is teaching the advantages of placing ITO directly
3 on insulating layer. And by doing the placement of
4 the ITO directly on the insulating layer, pinholes
5 within the indium tin oxide layers will not affect 03:14:44
6 the reliability of any underlying metal layer,
7 because below the indium tin oxide layer there will
8 be an insulating layer.

9 Those portions are discussed with reference
10 to the different embodiments of Sukegawa, so the 03:15:14
11 teaching in Sukegawa -- so within Sukegawa there is
12 a teaching that it is advantageous to place the
13 transparent conductive film 8 that will be exposed
14 directly on the surface of an insulating layer.

15 So it will take someone with ordinary skill 03:15:46
16 in the art to place 8 on top of 9, given the
17 teachings within Sukegawa that such a placement will
18 create a more robust structure because it will solve
19 the problem of the pinholes.

20 Q Okay. So where are those citations, 03:16:15
21 please?

22 A So in column 6, lines 23 to 38, starting
23 from the part that reads, "Accordingly, even if the
24 transparent conductive film 8 in the terminal
25 portion contains a defect or even if it is used in a 03:18:57

1 high humidity atmosphere, the upper layer metal
2 wirings, 7-1 and 7-2 are not exposed to the external
3 air and protected against corrosion," and continues,
4 "in that embodiment, the transparent conductive film
5 8 is shown to be formed directly on insulating 03:19:24
6 layer."

7 That insulating layer is not subject to any
8 corrosion because it does not react. It is already
9 an oxide or nitride.

10 So it shows that if I place the transparent 03:19:46
11 conducting film on an insulating film, and even if
12 there are pinholes, those pinholes will not cause
13 any corrosion.

14 Q Professor, isn't that discussing Figure 3E,
15 and they are talking about the part of layer 8 where 03:20:16
16 there is no layer 7 underneath it to be corroded by
17 pinholes?

18 A I think that's the essence of the teaching,
19 you place the transparent conductive layer that will
20 be exposed not directly on top of a metal, so if 03:20:39
21 there are pinholes, you will not expose the
22 underlying metal into it.

23 So you it will take ordinary skill in the
24 art that if you reverse the order with which 8 and 9
25 are laid down, you will gain that advantage by 03:21:06

1 having the 8 on top of an insulating layer
2 throughout the surface. And the same thing has also
3 been taught in another embodiment where, again, the
4 placement of the transparent conductive layer
5 directly on top of an insulating layer and not above 03:21:32
6 the metal, it results in this improved reliability.

7 Q Okay. Is there a further citation that you
8 located?

9 A Yes, let me -- so it is column 7, line 48,
10 and I'm quoting, "Also in this embodiment, the 03:22:44
11 transparent conductive film 8 exposed through the
12 aperture portion of the protective insulating film 9
13 is formed directly on the surface of the inter-layer
14 insulating film 3 under which the upper layer metal
15 wire 7 is not present in the same manner as in the 03:23:05
16 first embodiment. Accordingly, if the transparent
17 conductive film 8 in the terminal portion contains
18 defect or it is used in a high humidity atmosphere,
19 the metal wiring 7 is not exposed to the external
20 atmospheric and can be protected against corrosion." 03:23:21

21 So in both these embodiments, Sukegawa
22 teaches the advantages of placing the transparent
23 conductive layer directly onto an insulating layer,
24 which, by itself, would be resistant to corrosion
25 and will not be affected if there are any pinholes 03:23:46

1 in the transparent conductive layer.

2 So it will take somebody with ordinary
3 skill in the art to see that reversing the order 8
4 and 9, that will result in such advantages because 8
5 will be on top of an insulating layer and any 03:24:13
6 pinholes will not affect the underlying layers.

7 Q Anything else? Are those all the ones you
8 found?

9 A And there is another embodiment it is
10 placing the ITO on top of the glass where it is an 03:24:34
11 insulating layer. So there are three embodiments
12 within Sukegawa that discuss the advantages of
13 placing the ITO on an insulating layer. It gives
14 two examples of what are those insulating layers.
15 One is the insulating layer 3, another is the glass 03:25:00
16 substrate.

17 So I will take ordinary skill in the art to
18 reverse the order of 8 and 9 and place 8 above 9 to
19 get the benefits of placing the transparent
20 conductive layer on to an insulating substrate. 03:25:23

21 Q Thank you.

22 A If I may, outside of Sukegawa, that has
23 also been disclosed in other prior art references
24 that I have reviewed as part of this proceeding. It
25 was well known at the time of the invention that the 03:25:48

1 placement of the ITO on the upper surface of the
2 passivation film would result in some advantages as
3 far as the corrosion concerns.

4 Placing the IT on top of 9, particularly
5 the time that the '204 was filed was certainly not 03:26:23
6 an innovation. I'm not sure what was the priority
7 day, but even by Sukegawa is better than the '204
8 and Sukegawa is listed as a reference in '204 so I'm
9 sure that the artist have to put a reference --
10 sorry, a drawing that will not be exactly the same 03:27:09
11 as the one depicted by Sukegawa.

12 But, as we discussed and I testified a
13 number of times already, the language in '204 is
14 broad that covers both structures.

15 Q If there are advantages to putting the ITO 03:27:40
16 layer 8 above layer 9, can you think of any reasons
17 why Sukegawa did not illustrate that in Figure 3E,
18 for example, or even in Figure 2C?

19 A Perhaps Sukegawa wanted to avoid having an
20 embodiment that would look like other prior art 03:28:14
21 pieces that had ITO above the layer 9.

22 Q You don't have those references here today,
23 do you?

24 A No. You may have it.

25 If you look at the prior art, Moriyama, you 03:28:55

1 will see that the ITO layer is the upper layer and
2 it has been placed on top of an insulating film.

3 Do you happen to have Moriyama with you?

4 Q No.

5 A I'm sure my counsel can try to generate it. 03:30:04

6 Q Is it correct that in the column 7 citation
7 you gave us, Sukegawa --

8 A Which line?

9 Q At line -- well, I think you cited 48 to
10 57. 03:31:37

11 Is the transparent conductive layer on top
12 of the oxide layer 3 or, rather, the nitride layer
13 9?

14 A Well, in the particular embodiment
15 discussed in this section, it is form the 03:32:18
16 inter-layer insulating film 3, but the benefit of
17 placing at here on top of an insulating film will
18 apply independently of what is that insulating film,
19 whether that will be the 3 or the 9. Because they
20 are -- both 3 and 9 will not be affected if there 03:32:56
21 will be a pinhole in the transparent conductive
22 layer, none of them will be reacting and corroding.

23 Q I understand.

24 In your citation at column 6, lines 23 to
25 38, is that also talking about placing the ITO film 03:33:23

1 on top of the oxide 3, rather than on top of the
2 nitride 9?

3 A Inter-layer insulating film 3 is a
4 composite film that includes an oxide, silicon oxide
5 film and silicon nitride film. It is column 4, line 03:34:12
6 22. It reads, "a composite film of a silicon oxide
7 film and a silicon nitride film to form an
8 inter-layer insulating film 3 is formed."

9 So both 3 and 9 contain silicon nitride, so
10 it's not that one is better than the other one. 03:34:38

11 Q But is it the case that in the Figure --
12 sorry -- in the column 6 passage you mentioned,
13 Sukegawa is talking about the transparent conductive
14 layer over the insulator 3?

15 A In this particular embodiment. But the 03:35:42
16 advantages of having 8 on top of 9 will be the same
17 as having on top of 3.

18 Q I understand what you're saying.

19 Do you agree that there is no embodiment in
20 Sukegawa where 8 is over or on top of 9, 03:36:19
21 specifically?

22 A There is no drawing, but the teaching for
23 creating and modifying the embodiment discussed, the
24 preferred embodiment we discussed, is there. And
25 Sukegawa teaches that various modifications are 03:36:56

1 possible. And placing 8 above 9 is one such obvious
2 modification or possible modification.

3 It would be better to say obvious and
4 possible. Even better, an obvious possible
5 modification.

03:38:18

6 Q The passage that you're citing does not
7 say, specifically, to have an embodiment with layer
8 8 over layer 9, does it?

9 A The passages I described teach the benefits
10 of having ITO on top of an insulating layer. They
11 use an example. They have two examples, two
12 different insulating layers, and those are two
13 different insulating layers. 9 would have been an
14 obvious modification.

03:39:04

15 Q I understand what you're saying. That
16 doesn't mean I agree with you, but I understand what
17 you're saying.

03:39:35

18 I want to ask you some questions about the
19 '204 patent. I believe you have a copy in front of
20 you.

03:40:01

21 I think that the first claim that is
22 challenged is claim 31; is that right?

23 A I have to refer to my declaration.

24 That's correct.

25 Q Okay. Well, let's look at claim 31, then.

03:41:31

1 That appears at column 17, lines 35 through
2 63, or 62.

3 Do you have that before you?

4 A I do.

5 Q Good. 03:41:56

6 Actually, let's, instead, turn to claim 54.
7 That starts at column 19, line 62 and extends down
8 through column 20, line 31.

9 Do you have that before you now?

10 A I do. 03:43:10

11 Q Okay. Good.

12 And if you read through this claim, I think
13 that you'll find the use of the word "over," for
14 example, at column 20, line 3 --

15 A Okay. 03:43:37

16 Q -- which calls for a first conductive line
17 over the substrate.

18 And these questions are much like the ones
19 I asked you yesterday about the sequence.

20 So does the word "over" imply a sequence 03:43:46
21 here as between the substrate and the first
22 conductive line?

23 A It means that the first conductive line is
24 formed over the substrate, that the substrate
25 preexists the first conductive line. 03:44:08

1 Q Okay.

2 A You cannot form the substrate over the
3 first conductive line.

4 Q Does the next claim element, a first
5 insulating film over the conductive line, call for 03:44:25
6 the first conductive line to be in existence first
7 with respect to the first insulating film?

8 A That's correct.

9 Q And, correspondingly, or similarly, does
10 the next claim element at column 20, line 5, which 03:44:46
11 recites, "a second conductive line over the first
12 insulating film," does that require the existence of
13 the first insulating film to be in existence prior
14 to the second conductive line?

15 A Yes. 03:45:09

16 Q Does the next paragraph of the claim
17 similarly have a sequence implicit in it? That one
18 calls for a, quote, transparent conductive layer
19 over a first region of the second conductive line,
20 closed quote. 03:45:37

21 Does that mean that the transparent
22 conductive layer is placed after the second
23 conductive layer -- sorry, the second conductive
24 line is established?

25 A The transparent conductive layer is formed 03:45:58

1 after the first region of the second conductive line
2 is formed.

3 Q And the next claim element, must the
4 flexible printed circuit be placed over the first
5 region of the second conductive line, does that mean 03:46:18
6 that the second conductive line must be formed first
7 before the flexible printed circuit is put there?

8 A That's correct.

9 Q And next, where it says that a sealant --
10 strike that. 03:46:38

11 It says, quote, a sealant over a second
12 region of the second conductive line, closed quote.

13 Does that language imply that the second
14 conductive line must have a second region which is
15 established before the sealant is placed there? 03:46:55

16 A That is correct.

17 In all these cases, we relay the sequence
18 of two elements. And the only thing we can say from
19 each individual sentence is which comes first and
20 which comes second. 03:47:24

21 If we take certain of these sentences as a
22 group to relay the sequence of more than two
23 elements, then in some sections an explicit order of
24 which comes first, second and third also appears.

25 The fact that there is a sequence between 03:47:58

1 two different elements, it does not imply inherently
2 the sequence of more than one -- more than two
3 elements. I don't know if I'm making myself clear.

4 Q Okay.

5 A But please continue. 03:48:24

6 Q Okay. The next one is on line 14 and that
7 calls for a conductive layer over the substrate.

8 Does that mean the substrate must exist
9 before the conductive layer is placed over it?

10 A Yes. But, for example, in this particular 03:48:38

11 sentence, a conductive layer over the substrate, we
12 can only say the relationship, the order, between
13 those two elements; for example, that sentence by
14 itself, it does not, for example, relate the
15 conductive layer with any of the previous elements 03:49:05
16 that were discussed, for example, to know how the
17 conductive layer -- maybe start again.

18 That sentence, "a conductive layer over the
19 substrate," it only implies an order that the
20 conductive layer is formed after you have the 03:49:41
21 substrate. But that sentence alone does not relay
22 the conductive layer, it does not relay the order
23 with which the conductive layer was placed over the
24 substrate in relationship to any of the other
25 elements that we are already discussed. And we 03:50:05

1 discussed a number of elements that are over the
2 substrate. For example, we had the first conductive
3 line over the substrate, we had the first insulating
4 film over the first conductive line, hence the first
5 insulating film is also over the substrate. The 03:50:24
6 second conductive line over the first insulating
7 film also, which means that the second conductive
8 line is also over the substrate.

9 So this is three other elements, first
10 conductive line, first insulating film, second 03:50:38
11 conductive line, that are also over the substrate.
12 And here we have, in this line 14, another element
13 over the substrate.

14 So I'm just trying to clarify that the
15 order, in using the word "over," is implied only 03:50:56
16 between those two elements that are used in that
17 sentence.

18 If we want to derive the relationship or
19 the order among multiple layers, we have to look in
20 more than one of those statements and see if that 03:51:17
21 such relationship can be established in a unique way
22 or there are multiple ways that can be established.

23 Q Looking at the subparagraph beginning at
24 line 21, which reads, "Wherein the second conductive
25 line and the flexible printed circuit are in 03:52:13

1 electrical contact through the transparent
2 conductive layer."

3 Is there an implied sequence there that
4 tells us that the contact -- that tells us anything
5 about the contact? 03:52:38

6 MR. GIBSON: Objection; form.

7 THE WITNESS: What do you mean?

8 MR. MANZO: Strike the question.

9 Q Let's move on to the next claim element.

10 The next claim element says, "Wherein the 03:53:04
11 second conductive line and the transparent
12 conductive layer are in direct contact through an
13 opening in the second insulating film."

14 Does the opening in the second insulating
15 film provide the ability for the second conductive 03:53:27
16 line and the transparent conductive layer to have
17 direct contact?

18 MR. GIBSON: Objection; form.

19 THE WITNESS: Whether it provides the
20 ability for the second conductive line and the 03:54:00
21 transparent conductive layer to have direct contact
22 or, alternatively, between the vertical walls of the
23 opening, the second conductive line and the
24 transparent conductive layer are in direct contact
25 depends upon how you construe the word "through." 03:54:24

1 That sentence alone is subject to the
2 construction of the word "through."

3 We can look at the earlier sections above
4 and we can try to derive a sequence of layers and we
5 can try to see if one of those two possible outcomes 03:55:02
6 for the construction of the word "through" can be
7 revealed. If the word "through" can be construed
8 as -- as you said, whether the opening provides the
9 ability to have direct contact, which I guess it
10 would be construed as being because of the opening, 03:55:44
11 or that the contact existed between the opening, the
12 vertical -- the edges of the opening, the vertical
13 walls of the opening.

14 And if we do the analysis as we have
15 started doing it, an expert will -- not an expert, 03:56:03
16 someone with ordinary skill in the art will see that
17 there is no specific order that is described, rather
18 a broad language is used that -- to describe the
19 relationship between the second conductive line, the
20 flexible printed circuit and the second insulating 03:56:41
21 film.

22 Both the second insulating film and the
23 transparent conductive layer, they are both over the
24 second conductive line. They do not list the order
25 which one is above what. 03:56:59

1 MR. MANZO: I think we have to change the
2 video disk.

3 THE VIDEOGRAPHER: This is the end of tape
4 2. We are off the record at 3:57 p.m.

5 (Recess.) 03:57:18

6 THE VIDEOGRAPHER: This is the beginning of
7 tape 3. We're back on the record at 4:11 p.m.

8 BY MR. MANZO:

9 Q Professor, I think you were in the middle
10 of analyzing claim 54. 04:11:32

11 Had you finished your answer about whether
12 the opening referred to at column 20, line 25 is the
13 structure that permits the second conductive line to
14 have direct contact with the transparent conductive
15 layer? 04:12:17

16 A What I wanted to say and is not quite
17 captured in my last statement, in the last sentence
18 of my previous statement, is that based on the
19 different limitations listed above for the different
20 elements, one cannot see an order between the 04:13:36
21 transparent conductive layer and the second
22 insulating film.

23 Both are over the second conductive line,
24 but the language is broad and does not express or
25 implies a specific order. In that -- in the context 04:14:11

1 of such a broad language, the word "through" cannot
2 be construed in a unique way.

3 Q Looking at Figure 4A, would you agree that
4 the second conductive line shown in this figure is
5 in direct contact with the transparent conductive 04:15:01
6 layer, which is 114, only because of the existence
7 of the opening in the resin inter-layer film 113?

8 MR. GIBSON: Object to the form.

9 THE WITNESS: In the particular Figure 4A
10 in this particular embodiment in this particular way 04:16:22
11 of fabricating and constructing the structure, this
12 is true, but the language used in the claim -- and,
13 if I may add, the language that is in the text of
14 the specifications within '204, and, in particular,
15 the section that I read to you earlier within the 04:16:55
16 example 3, column 8, lines 53 to 55, the language is
17 broad and is not limited to just one embodiment.

18 BY MR. MANZO:

19 Q That language says, "Referring to
20 Figure 4A, the external connection lines 403 are 04:17:31
21 electrically connected to an FPC (flexible printed
22 circuit) 107, through contact holes provided in the
23 resin inter-layer film 113 through ITO (indium tin
24 oxide) film 114."

25 Is that what you're citing? 04:17:58

1 A Exactly.

2 Q And you agree -- let me ask.

3 Do you agree from the very first words of
4 that sentence that it is referring to Figure 4A,
5 where it says, quote, Referring to Figure 4A, closed 04:18:20
6 quote?

7 A Right. But that language, if I may ask,
8 how is it different from the Figure 1B of Sukegawa?
9 Isn't that language here that the "external
10 connection lines 403 are electrically connected to 04:18:39
11 an FPC (flexible printed circuit) 107 through
12 contact holes providing the resin inter-layer film
13 113 through an ITO (indium tin oxide) film 114"?

14 Doesn't that language describe exactly what
15 it is in Sukegawa? 04:18:59

16 Q I don't think so, no, but that's what we're
17 going to let the board decide.

18 A No, I understand.

19 But if we -- we agree that Figure 4A shows
20 something. 04:19:15

21 Q Yes.

22 A I don't think we disagree with that part.

23 Q Good.

24 A Okay. Now, referring to the text that
25 describes the "external connection lines 403 are 04:19:23

1 electrically connected to an FPC (flexible printed
2 circuit) 107 through contact holes providing the
3 resin inter-layer film 113 through an ITO (indium
4 tin oxide) film 114," and I say that that sentence,
5 someone with ordinary skill in the art will see 04:19:50
6 exactly that part. That's how someone ordinarily
7 skilled in the art will describe the connection
8 between the external connection lines and the
9 flexible printed circuit board by looking at the
10 Sukegawa, and that's the only reference I find in 04:20:07
11 the specifications that is relevant to construe the
12 word "through," Figure 4A and that sentence.

13 And I said that sentence is exactly what is
14 described in Sukegawa if we just change the numerals
15 to the ones used by Sukegawa. 04:20:42

16 I understand that the words should be --
17 could be construed in light of specifications, but
18 in this case, the specifications themselves contain
19 a very broad language.

20 And if there is any other section in the 04:21:29
21 specifications that you read something else in
22 relationship to the order of the different layers,
23 in particular the second insulating film and the
24 transparent conductive layer, please bring out to me
25 so I can review that section in case I have already 04:21:47

1 miss it.

2 Q Give me a moment to consider what you said.

3 A moment ago you said we could substitute

4 the -- we could change the numerals to refer to

5 Sukegawa and change the sentence that's in column 8. 04:24:27

6 Can you go ahead and do that for us so that

7 this sentence would describe Sukegawa?

8 A The external connection lines 31 are

9 electrically connected -- strike that.

10 The external connection lines 7 are 04:25:36

11 electrically connected to a FPC (flexible printed

12 circuit) 31 through contact holes provided in the

13 resin inter-layer film 9 through ITO (indium tin

14 oxide) film 8.

15 If I may add, that sentence even captures 04:26:16

16 better Figure 2C of Sukegawa than Figure 4A that it

17 is referring to, because at least the flexible

18 printed circuit through contact holes.

19 And that's what we see in Figure 2C of

20 Sukegawa, we see the openings in 9. 04:26:38

21 And then says "through an ITO," and we see

22 that in Sukegawa.

23 Q In the '204 patent, looking and the Figure

24 4A or 4B, is there a sealant on only the second

25 insulator and not on the ITO? Do you see that? 04:29:13

1 A This is what is depicted in Figure 4A.

2 Q And do you agree that the ITO is formed
3 after the second insulator?

4 A Based on Figure 4A?

5 Q Yes, based on Figure 4A. 04:29:45

6 A Okay.

7 Q Do you agree?

8 A This is what is shown.

9 Q Okay. And I think, as you just discussed
10 or we've just discussed for a while, Figure 4A shows 04:30:01
11 an opening in that film 113 so that the external
12 connection lines 403 can contact the conductive
13 layer 114; is that right?

14 A Looking at Figure 4A in the way that the --
15 this particular embodiment is drawn, this is right. 04:31:07

16 Q And you agree that in Figure 4A the sealant
17 105 is not on top of the ITO 114, but, instead, it
18 is separated from it; is that correct?

19 MR. GIBSON: Objection; form.

20 THE WITNESS: In this particular embodiment 04:31:49
21 shown in Figure 4A, this is what it shows, but the
22 claims do not provide any limitation on the
23 placement of the sealant with respect to the ITO, or
24 I do not recall such a limitation.

25 BY MR. MANZO: 04:32:11

1 Q Do you agree that the '204 patent reduces
2 the height difference that is caused by the
3 formation of the auxiliary line, which is the first
4 conductive line 401 and the external connection
5 line, which is the second conductive line 403? 04:32:31

6 MR. GIBSON: Objection; form.

7 THE WITNESS: The objective of '204 is to
8 address the issue of unevenness around the seal area
9 and provide certain -- several embodiments of how to
10 do so, depending upon the construction of the wiring 04:33:28
11 used in making the external connections.

12 BY MR. MANZO:

13 Q Okay. Do you agree that the '204 patent
14 uses adjustment layers to keep a relatively constant
15 seal height -- strike that. 04:33:49

16 Do you agree that the '204 patent uses
17 adjustment layers to preserve a relatively constant
18 spacing between the substrate and the counter
19 substrate even though an external connection line
20 and an auxiliary line, one above the other, pass 04:34:11
21 underneath the sealant between those two substrates?

22 A Well, the '204 patent alleges, as
23 innovations, the use of the adjustment layers to
24 preserve a relatively constant spacing between the
25 substrate and the counter substrate, even though an 04:35:13

1 external connection line, auxiliary line, one above
2 the other pass underneath the sealant between those
3 two substrates.

4 And it's my understanding it's the purpose
5 of these proceedings to determine if these are, 04:35:30
6 indeed, new innovations worthy of issuing a patent
7 or not.

8 In my analysis, I found prior art that meet
9 exactly the same -- provide similar structures --
10 actually, same structures to solve that problem. 04:36:00

11 Q Is it true that you did not find any
12 adjustment layer in the Shiba patent for attacking
13 that problem?

14 A Shiba does not address the issue of the
15 spacing between the two substrates, but the prior 04:36:27
16 art reference which I utilized, namely, the Watanabe
17 patent, address that issue.

18 So Shiba, in view of Watanabe, teach or
19 render obvious these substrate gap adjustment
20 layers. 04:37:32

21 Q In Shiba, you have spoken about a
22 transparent conductive layer, right?

23 A (No audible response.)

24 Q Do you recall that we talked about a
25 transparent conductive layer in Shiba? 04:38:07

1 A There is a transparent conductive layer
2 disclosed in Shiba.

3 Q Is there any disclosure or teaching or
4 suggestion in Shiba that the transparent conductive
5 layer should not extend to the second region that is 04:38:22
6 defined by the claims at issue here?

7 MR. GIBSON: Objection; form.

8 BY MR. MANZO:

9 Q Well, Professor, I think your counsel wants
10 me to point you to the particular claim, so let me 04:39:44
11 modify my question.

12 Do you see that claim 54 refers to a first
13 region and a second region of the second conductive
14 line?

15 MR. GIBSON: Which claim? 04:40:05

16 MR. MANZO: 54.

17 MR. GIBSON: Thank you.

18 THE WITNESS: Yes.

19 BY MR. MANZO:

20 Q Okay. So I'm asking whether there's any 04:40:44
21 teaching, suggestion or other specific motivation in
22 Shiba that the transparent conductive layer should
23 not extend to the second region defined in claim 54
24 of the '204 patent?

25 MR. GIBSON: Objection; form. 04:41:23

1 THE WITNESS: I use Shiba, in view of
2 Watanabe, and I also use Shiba, in view of Sukegawa.

3 So if we consider Shiba in both of the
4 prior art references, so Shiba, in view of Sukegawa,
5 and Shiba, in view of Watanabe, as I indicate in my 04:42:08
6 declaration, one skilled in the art will modify the
7 common pad of the -- which is shown in Shiba to
8 include the transparent conductive layer so that it
9 can -- above it, so that it can gain the advantages
10 of the corrosion protection -- protection from the 04:42:45
11 corrosion that the transparent conductive layer
12 offers.

13 In the pad region, this is where the metal
14 is exposed, the underlying metal below the
15 transparent conductive layer is exposed. And it 04:43:18
16 is -- and is subject to corrosion. And the common
17 pad 751 is far outside the sealant region, as shown
18 in Figure 3, because you have the wiring 121 next to
19 751, and that wiring 121, which is before the
20 sealant, is all under the passivation layer. So all 04:44:05
21 that wiring is already protected by the passivation
22 layer.

23 The only part of the wiring that will be
24 exposed and subject to corrosion is the part of- --
25 is the part labeled 751, which is exposed through 04:44:34

1 the slit 243. That part will be modified in view of
2 Sukegawa.

3 Someone with ordinary skill in the art will
4 not be motivated to protect wirings that have
5 already been protected by the second insulating film 04:45:08
6 by adding additional piece of metals, such as ITO,
7 the same way that they will do it in the terminal
8 pad region.

9 And in view of Sukegawa -- sorry. Strike
10 that. 04:45:26

11 In view of Watanabe, which addresses the
12 issue of the gap spacing, the person with ordinary
13 skill in the art will also understand that adding
14 additional metal will create a bigger step in the
15 gap region -- in the sealant region. 04:46:10

16 So you asked me whether there is it any
17 teaching, suggestion or other specific motivation in
18 Shiba that the transparent conductive layer should
19 not extend to the second region defined in claim 54
20 of the '204 patent. And in my answer I said that 04:46:44
21 someone with ordinary skill in the art based on the
22 teaching of Shiba, in view of Watanabe and Sukegawa,
23 will place the transparent conductive layer only in
24 the terminal region in the common pad 751 and will
25 not extend it into the second region under the 04:47:18

1 sealant, because you will not result in any
2 additional advantages and may, rather, create a
3 bigger step.

4 BY MR. MANZO:

5 Q Thank you. 04:47:50

6 If you were to look at claim 54 again, at
7 line 23, I think, the claim talks about electrical
8 contact. And at line 25 it talks about direct
9 contact.

10 Do you see that? 04:50:24

11 A I see that.

12 Q Are those two the same to a person of
13 ordinary skill in the art?

14 A A direct contact implies a direct physical
15 contact, that the two layers touch each other. 04:51:53

16 An electrical contact can occur between two
17 elements, even if they're not touching each other,
18 in other words, even if they are not in direct
19 contact. But if each touch a third element, third
20 object, they can be in electrical contact without 04:52:18
21 being in direct contact by -- through this other
22 material or object.

23 So in the case it says line 22, the second
24 conductive line and the flexible printed circuit are
25 in electrical contact through the transparent 04:52:46

1 conductive layer, that implies that the flexible
2 printed circuit is not touching directly the second
3 conductive line, but rather, in between there is
4 another material and that other material is the
5 transparent conductive layer.

04:53:07

6 So an electrical connection, which means
7 that the layers have to be in the same potential and
8 current can flow through them, can be established
9 through the transparent conductive layer.

10 In the other section, the direct contact,
11 it means that the two layers physically touching
12 each other.

04:53:27

13 And we had a lengthy discussion yesterday
14 about an electrical contact is established when you
15 have the passage of current, and that will require
16 some sort of an excitation source, some sort of a
17 voltage difference, such as those provided by an
18 external board through the flexible printed circuit.

04:54:09

19 Q Professor, if you have a television set,
20 the kind that runs off of AC power rather than a
21 battery, and it's plugged into the wall socket,
22 would you say that the television set is not in
23 electrical contact with the wall socket until the
24 on/off switch is turned on on the TV set?

04:56:52

25 MR. GIBSON: Objection; form.

04:57:20

1 THE WITNESS: You have a television set and
2 you have a wire, a cable, that is plugged to the
3 socket on the wall --

4 BY MR. MANZO:

5 Q The power supply cord. 04:58:23

6 A The power supply cord.

7 Before you turn on the power switch, the
8 television set will not consume any power. There
9 will be no current flowing into the television set,
10 no current will flow out of the wall to power any 04:58:43
11 electronics because the switch will prevent the flow
12 of the current.

13 Q So does that mean that until the switch is
14 turned on, the TV set is not in electrical contact
15 with the wall socket? 04:59:13

16 MR. GIBSON: Objection; form.

17 THE WITNESS: The cable, which is plugged
18 in, is physically attaching the external cable. A
19 potential along the cable line is established to be
20 the same as that of the -- of the outlet. And 04:59:49
21 somewhere there is a switch and that switch is off.

22 Now, from the streets and into the circuit
23 of the television there is no electricity that has
24 been sent. The cable is at the same voltage as the
25 outlet, like 110, 20 volts, and then there is a 05:00:31

1 switch that is opened. And the circuit within the
2 television apparatus is isolated.

3 And when you turn on the switch,
4 electricity flows. And when you turn off -- and
5 power is consumed. And when you turn off the 05:01:08
6 switch, current stops to flow.

7 BY MR. MANZO:

8 Q So --

9 A But the means to flow the current in and
10 out of the television set exists. 05:01:24

11 Q And --

12 A Whether -- it is controlled by the switch.
13 You have the ability to flow current in and out of
14 the television through the switch.

15 Yesterday we were discussing in the context 05:02:18
16 of Sukegawa when you have a continuous passivation
17 film, and I have explained that before the opening
18 in the passivation film there is no ability to flow
19 currents in or out because the whole system was
20 coated with insulations, there was no, in this 05:02:45
21 context, a magical switch that you can turn on or
22 off, so I don't know what you're trying to lead --
23 where you're trying to lead with your line of
24 questioning.

25 I am trying to be as explicit as possible 05:03:07

1 in my answers.

2 Q And we appreciate that, Professor.

3 Just going back to the TV set, you've
4 talked about the circuits in the TV set.

5 Is the power cord of the TV set in 05:03:21
6 electrical contact with the wall socket once it's
7 plugged into the wall socket without regard to the
8 state of the on/off switch in the TV set?

9 MR. GIBSON: Objection; form.

10 THE WITNESS: So if I understand your 05:04:13
11 question well, you're asking me, the switch is
12 off -- you asked me without regard to the state of
13 the on/off switch. So if the switch is on,
14 electricity flows to the TV set through the cable,
15 so in that case everything is electrically 05:04:40
16 connected, electricity flows. If the switch is off,
17 that's what needs to be addressed.

18 If the switch is off, no electricity flows
19 inside the TV set; however, at the moment you --
20 starting from the moment where the switch -- where 05:05:16
21 the cable is not plugged. Okay? We now have a
22 cable which is not plugged in the wall. Let's
23 assume that the TV is also in the off position. And
24 now we're plugging in the cable -- we're going to
25 plug the cable. 05:05:41

1 The voltage on the two leads of the cable,
2 the voltage difference is zero. There is no voltage
3 potential difference on the volt -- on the cable
4 that's not plugged to anything. It is a long cable
5 with a zero volt across it. Two cables who equally 05:05:59
6 have zero volt across them, if they are made of the
7 same material. They are not some weird effects, you
8 may recall from physics, that if two metals are made
9 of different materials, you may have other
10 phenomena. 05:06:19

11 But in this case you have two copper wires
12 that you have in the cable that is plugged into the
13 wall, assuming the two plugs. If we measure the
14 voltage difference before we plug them in, that
15 voltage difference is zero. 05:06:34

16 Once we are plugged in and we have means to
17 access the voltage difference between the two
18 cables, we will see that there is a voltage
19 difference between them. They both have obtained
20 voltage that is supplied by the outlet. So the 05:06:52
21 cable became electrically connected the moment you
22 plugged it in, into the TV wall, because the
23 electricity flew, current flew and established a
24 voltage difference between the two cables.

25 But from the switch inwards, the circuit is 05:07:15

1 isolated and no electricity can flow, no potential
2 difference still exist inside the circuit, and that
3 will continue until you press the on switch in the
4 on state.

5 BY MR. MANZO: 05:07:40

6 Q Professor --

7 A Thank you.

8 In the morning we were discussing a
9 hypothetical structure in Shiba.

10 Do you recall that? You were saying about 05:08:14
11 the presence of the dielectric layer 211 in between
12 the two wirings -- the two layers of wiring 127? Do
13 you recall that?

14 Q Yes. We were discussing dielectric and the
15 wiring in 127, and we had a discussion about whether 05:08:39
16 there's dielectric there or not.

17 A Right.

18 And you allege that there may be a means
19 that the two structure, the two layers will be
20 formed that will physically attach each other 05:09:05
21 because the dielectric layer will not be there.

22 Do you recall that?

23 Q Yes.

24 A And I have asked you whether there is
25 evidence, and you did not -- I did not recall you 05:09:20

1 showing me such evidence other than the allegations
2 that that -- somehow it is possible. If I recall, I
3 did not see evidence to point out that this
4 dielectric layer somehow is removed.

5 Q Did you want to amend your answer? 05:09:43

6 A No. What I would like to do is provide you
7 evidence that this layer is not removed, and I want
8 to back that evidence from the statements within
9 Shiba why that is not occurring. If you're
10 interesting (sic) to obtain that evidence from 05:10:09
11 Shiba, I will tell you that this hypothetical
12 structure has not been taught on Shiba. In
13 contrast, Shiba teaches away from that hypothetical
14 structure that you allege that may exist.

15 Q Where is that teaching? 05:10:30

16 A If we go to Shiba, column 7, line 45, it
17 reads, "Since the wiring line 127 is constituted by
18 a plurality of narrow lines as shown in Figure 6,
19 the protective overcoat 241 and the gate dielectric
20 211 are directly connected to each other through the 05:11:11
21 gap between the narrow lines. As a result, there is
22 a removal of the first wiring line 127 together with
23 the sealing agent 113 is reduced. Accordingly, the
24 degree of freedom of selecting material of the
25 sealing agent 113, depending on the adhesion 05:11:36

1 capacity, can be increased."

2 In other words, this section --

3 Q That's the end of the quote?

4 A Yes.

5 Q Okay. Go ahead. 05:11:53

6 A I read from line 46 to line 54.

7 Q Thank you.

8 A In that section Shiba is teaching the value
9 of maintaining the gate dielectric 211 in this
10 region, and the benefit of that one, it provides 05:12:17
11 better adhesion, protection for the first wiring 127
12 and the overcoat 241.

13 So here Shiba says the gate dielectric 211
14 serves a function. And the hypothetical structures
15 that you allege may exist will weaken the adhesion 05:12:54
16 of the overcoat and of the first wiring line 127
17 and, thus, will compromise the selection of the
18 materials that could be used for the sealing agent
19 113.

20 Q Where does this paragraph talk about 05:13:42
21 adhesion? Oh, are you referring to line 34,
22 adhesion capacity?

23 A Are we in the same column 7?

24 MR. MURPHY: 54.

25 BY MR. MANZO: 05:14:01

1 Q Oh, a 54. Sorry.

2 The last line of that paragraph, you
3 mentioned adhesion capacity. Is that the part
4 you're --

5 A Well, that's the adhesion capacity of the 05:14:11
6 sealing agent, but let me explain.

7 You have some structure on the glass and
8 now you're going to bond that glass to another piece
9 of glass and you're going to be using this sealing
10 agent 113. 05:14:34

11 Q Yes.

12 A But that process you may come down or you
13 may move it or you may not place in the right
14 location and then you have to remove it and reapply
15 it again. 05:14:53

16 And as it reads in line 54, the risk or
17 removal of the first wiring line 127 together with a
18 sealing agent 113 is recused. This means that when
19 you remove the sealing agent 113 to reposition the
20 second glass in order to align the color filters 05:15:24
21 with the right pixels, you're running the risk of
22 removing from the substrate the wiring 127 and the
23 overcoat 241.

24 If the sealant adheres very well to 241 and
25 241 adheres to 127, if you remove the sealant, you 05:15:47

1 will tear those lines apart and you're causing a
2 manufacturing defect.

3 241 is anchored to the substrate through
4 the gate dielectric 111. If you are removing the
5 dielectric 211, you create a bigger step for the 05:16:13
6 overcoat 241 to go all the way down to the
7 substrate.

8 Furthermore, you may undercut the wirings
9 127, and then will you start compromising how the
10 wiring 127 adheres onto 211, because even portions 05:16:35
11 around the edges of 127 may be exposed because the
12 211 may be undercut when you try to remove it.

13 So removal of 211 will create a lot of
14 risks in weakening the way that the 241 and 127
15 adhere into the substrate and will make the 05:17:07
16 placement of the counter substrate a very dangerous
17 operation.

18 But if you leave it intact, and the process
19 I said that someone with ordinary skill in the art
20 will opt to do to create contacts only on top of 05:17:36
21 the -- in selected areas on top of the underlying
22 layer, you will not remove the layer 211 from that
23 entire region and, yes, it will be -- the structure
24 will not be compromised.

25 Q Thank you for that clarification. I think 05:18:02

1 we'll take a recess now, please.

2 THE VIDEOGRAPHER: Off the record at

3 5:18 p.m.

4 (Recess.)

5 THE VIDEOGRAPHER: Back on the record at

05:18:17

6 5:31 p.m.

7 BY MR. MANZO:

8 Q Professor, just to conclude, a little while

9 ago you were talking about what happens if you need

10 to move the counter substrate relative to the

05:31:52

11 substrate.

12 Do you remember that?

13 A I was just explaining the passage from

14 column 7.

15 Q Okay. And the question we want to ask you

05:32:02

16 is with regard to the wiring that's under the

17 sealant --

18 A You mean 127?

19 Q Yes.

20 -- if that wiring -- strike that.

05:32:23

21 With regard to that wiring 127, is that

22 wiring more likely or less likely to be ripped out,

23 as you said, if it is indium tin oxide or metal?

24 MR. GIBSON: Object to the form.

25 THE WITNESS: As I explained earlier, there

05:32:56

1 is no reason why to form that wiring with 127. The
2 indium tin oxide will result in a high resistance,
3 so your question is a little bit not relevant
4 because you will not form that wiring with indium
5 tin oxide, it will be very resistive, it will serve 05:33:30
6 no purpose.

7 BY MR. MANZO:

8 Q Well, hypothetically, if -- let's modify
9 the question, then. So make it hypothetical so that
10 in one case it is metal that is not covered with ITO 05:33:45
11 and in the other case it is metal that is covered
12 with ITO.

13 Is one more likely to be ripped out than
14 the other when the counter substrate has to be moved
15 relative to the substrate? 05:34:05

16 MR. GIBSON: Object to the form.

17 THE WITNESS: Even if, hypothetically, one
18 includes ITO, based on your statement, that will
19 still be under the protective overcoat 241.

20 The issue is not so much if you have or not 05:34:36
21 have ITO, which I explained I see no reason to have
22 ITO there, but the issue is whether you have or not
23 have the gate dielectric 211.

24 As I explained, Shiba teaches away from
25 removing the gate dielectric 211 from that region 05:35:01

1 because that will weaken the structure. And if you
2 weaken the structure by removing the gate dielectric
3 211, whether you have or do not have the ITO, the
4 structure has already been compromised and it will
5 be very weak based on the approach you discussed the 05:35:24
6 morning.

7 So I'm trying to say Shiba teaches a way of
8 removing the gate dielectric 211 and Shiba
9 acknowledges that ITO is a highly resistive material
10 so you would not use ITO to create a wiring line 05:35:56
11 that runs long distance. And Shiba acknowledges
12 that the length of the first wiring line is very
13 long because it has to distribute the power to the
14 pads that in the opposing long side to the side
15 where the power is supplied since the wiring line 05:36:20
16 has to be low resistance.

17 In my testimony I have only described
18 modifications in Shiba that will result in current
19 flow transverse to the thickness of the Shiba --
20 sorry -- transverse to the thickness of indium tin 05:37:34
21 oxide, hence the presence of the layer will not add
22 resistance, because that layer is so thin.

23 But you're referring to a line that is very
24 long. And I did not find the rationale anywhere in
25 Shiba to add that line -- to the transparent 05:38:15

1 conductive layer in the first wiring line.

2 BY MR. MANZO:

3 Q Okay. Well, let me ask you hypothetically,
4 assuming that the dielectric 211 is present in the
5 lines and one wire is ITO, hypothetically, and 05:38:39
6 another wire is another metal.

7 Is the sealant adhesion different for the
8 two wires?

9 MR. GIBSON: Object to the form.

10 THE WITNESS: I don't think I can answer 05:39:29
11 this hypothetical question because it all depend
12 upon how you put the ITO, what stresses you have in
13 the ITO layer and what is the passivation -- this
14 protective overcoat 241, what is the gate dielectric
15 on top of which the ITO will be deposited and what 05:39:55
16 is the sticking coefficient or the adhesion between
17 the ITO and these layers.

18 And then the same analysis has to be done
19 for the other wire, which is made by another metal
20 to convert them. 05:40:21

21 For example, you can put a wire down that
22 it -- a metal down to form a wire, and if you have a
23 lot of stresses built in that material during the
24 deposition process or if the thermal expansion
25 coefficient of that metal is such that when you are 05:40:42

1 putting all these other layers and you're hitting
2 the structures, you build a lot of stresses in the
3 structures, you may compromise the adhesion.

4 So it's not a straightforward answer. You
5 can have each the same material that as you go 05:41:03
6 through different deposition conditions and
7 different annealing conditions, you can modify the
8 stresses in the metal layer, and those ones may
9 affect the way that layer interacts with the
10 overcoat and the underlying coating, so there are a 05:41:36
11 lot of unknowns in your hypothetical example.

12 Some layers, for example, aluminum and
13 chromium, adhere very well. So there are layers
14 that are known to have good adhesion. But even
15 chromium, if you make it too thick, it will have a 05:42:03
16 lot of stresses and the adhesion will compromise.
17 So a lot of factors affecting that.

18 BY MR. MANZO:

19 Q Thank you.

20 What is the adhesive property of ITO 05:42:57
21 relative to chromium and aluminum, which you did
22 mention?

23 A You mean the sticking coefficient of -- I
24 think it is called sticking coefficient of I- --

25 Q ITO? 05:43:32

1 A Yeah. I have to work from memory, I don't
2 know exact numbers, but I know, for example,
3 chromium is a very good adhesion to silicon dioxide
4 layer, and most likely it will be better than ITO.
5 I just don't remember exact numbers or relative 05:43:55
6 rating of the two. I know some are better than
7 others.

8 MR. MANZO: Thank you, Professor. We have
9 no further questions.

10 MR. GIBSON: I do not have any questions. 05:44:19

11 THE VIDEOGRAPHER: We are off the record at
12 5:44 p.m. This concludes today's testimony given by
13 Dr. Hatalis. The total number of media was 3 and
14 will be retained by Veritext LLC.

15 (TIME NOTED: 5:44 p.m.)

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I, MILTIADIS HATALIS, PH.D., do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made any corrections as appear noted, in ink, initialed by me, or attached hereto; that my testimony as contained herein, as corrected, is true and correct.

EXECUTED this _____ day of _____,
2013, at _____, _____.
(City) (State)

MILTIADIS HATALIS, PH.D.
Volume I

1 I, the undersigned, a Certified Shorthand
2 Reporter of the State of California, do hereby
3 certify:

4 That the foregoing proceedings were taken
5 before me at the time and place herein set forth;
6 that any witnesses in the foregoing proceedings,
7 prior to testifying, were placed under oath; that a
8 true and correct record of the proceedings was made
9 by me using machine shorthand which was thereafter
10 transcribed under my direction; further, that the
11 foregoing is an accurate transcription thereof.

12 I further certify that I am neither
13 financially interested in the action nor a relative
14 or employee of any attorney of any of the parties.

15 IN WITNESS WHEREOF, I have this date
16 subscribed my name.

17 Dated: 8 July 2013

18

19

20


DENISE BARDSLEY
CSR No. 11241

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