SEL EXHIBIT 2012

INNOLUX CORPORATION v. PATENT OF SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

IPR2013-00068

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRAIL AND APPEAL BOARD

INNOLUX CORPORATION, Petitioner, vs. PATENT OF SEMICONDUCTOR ENERGY LABORATORY CO., LTD., Patent Owner.	No. IPR2013-00066 Patent 7,876,413

VIDEOTAPED DEPOSITION OF MILTIADIS HATALIS, PH.D.
Irvine, California
Monday, July 1, 2013
Volume I

Reported by:
DENISE BARDSLEY
CSR No. 11241
Job No. 1684547

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Videotaped deposition of MILTIADIS HATALIS, PH.D., Volume I, taken on behalf of Patent Owner, at 3 Park Plaza, Suite 1100, Irvine, California, beginning at 9:02 a.m. and ending at 6:32 p.m. on Monday, July 1, 2013, before DENISE BARDSLEY, Certified Shorthand Reporter No. 11241.

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Irvine, California, Monday, July 1, 2013

9:02 a.m.

THE VIDEOGRAPHER: Good morning.

We are on the record at 9:02 a.m. on July 1st, 2013. This is the video-recorded deposition of Dr. Milt Hatalis. My name is Scott Slater, here with our court reporter, Denise Bardsley. We are here from Veritext Legal Solutions at the request of the patent owner.

This deposition is being held at 3 Park Plaza, Suite 1100, in the city of Irvine, California 92614. The caption of this case is Innolux Corporation versus Patent of Semiconductor Laboratory Co., Ltd., Case No. IPR2013-00066, Patent 7,876,413.

Please note that audio and video recording will take place unless all parties agree to go off the record.

Microphones are sensitive and may pick up whispers, private conversations or cellular interference.

I am not authorized to administer an oath, I am not related to any party in this action, nor am I financially interested in the outcome in any way.

May I please have an agreement from all parties that we may proceed.

MR. MANZO: Agreed.

MR. GIBSON: That's fine with me.

THE VIDEOGRAPHER: Thank you very much.

At this time will counsel and all present please identify themselves for the record.

MR. MANZO: For the plaintiff -- sorry.

For the patent owner, my name is Edward Manzo, M-a-n-z-o.

With me are Mark Murphy and Stanley Schlitter.

Mr. Murphy and I are from the firm of Husch Blackwell, LLP in Chicago. Mr. Schlitter is from Steptoe & Johnson.

MR. GIBSON: Stan Gibson on behalf of the petitioner.

THE VIDEOGRAPHER: Thank you very much.

Will the court reporter please administer the oath.

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MILTIADIS HATALIS, PH.D.,

having been administered an oath, was examined and testified as follows:

EXAMINATION

BY MR. MANZO:

Q Good morning, Professor. My name is Edward Manzo, and I'm here on behalf of SEL to ask you some questions about topics that are raised in your declaration and otherwise.

A Good morning.

Q Could you please state your name.

A Miltiadis Hatalis.

Q And do you live in Pennsylvania somewhere?

A In Bethlehem, Pennsylvania.

Q Thank you.

How old are you, Doctor?

A 54.

Q I'm going to hand you what's been previously filed as Exhibit 1005. It purports to be the declaration of Miltiadis Hatalis.

Could you just take a quick look at that and tell me if that is the declaration that you signed?

A Yes, it is.

Q Thank you.

How did you prepare for today's deposition?

A I reviewed the petition, I reviewed my declaration, I reviewed the board decision, I reviewed the rehearing request by the patent owner, and I reviewed the decision of the board from the rehearing, and I also reviewed the initial response of the patent owner.

Q Did you look at the challenged patent?

A Yes. I also looked at the '413, and I look at the two prior art patents, namely the one from Sukegawa and Nakamoto.

Q For convenience, why don't we refer to those that way.

We'll call Exhibit 1003, which is U.S. Patent 5,636,329 the Sukegawa patent.

Is that okay with you?

A It will be fine.

Q And we'll call the Japanese reference to Nakamoto, N-a-k-a-m-o-t-o, and that was filed as Exhibit 1004, we'll call that Nakamoto.

Is that all right with you?

A That will be fine.

Q Okay. Thank you.

Did you meet with anybody in preparation

for today's deposition?

A Yes. I met with my counsel, Stan Gibson, and his colleague, Ali Shalchi.

Q About how long did you meet?

A I arrived in the area Wednesday night, so we met the last four days.

Q Professor, do you know how you came to be hired or why you were hired for this expert engagement?

A I am a professor in the field of microelectronics and, in particular, my group and my Ph.D. thesis is advancing the technology of thin-film transistors, which is the main electronic device used in flat panel displays and, in particular, the active metrics liquid crystal displays. I'm director of a laboratory which I have founded in the early '90s at Lehigh, which is called the Display Research Laboratory, and I have published extensively in this field, both in scientific journals and in conference proceedings.

I also published two book chapters, so I consider myself to be expert in this field.

Q Have you actually worked in the microelectronics field producing any products, commercial products?

A I have been in academia and I have worked with companies as a consultant, but the academic institution that I have been as a student or, for the last 25 years, as professor is a nonprofit institution so we do research. We do not produce and sell commercial product.

But we produce prototype displays and produce processes, device structures, materials that different companies may adopt in their manufacturing process for making displays.

Q Can you tell me the difference between a process engineer and a circuit design engineer with respect to the semiconductor field?

A A process engineer and a circuit design engineer -- a process engineer deals more with the actual fabrication, so it deals with the different processes that are used to deposit material, to lay down materials, to remove materials, to clean substrates, to do a process known as a photolithographic process, which defines the areas that will remain on the substrate during an etching process. So it's involved with all the different fabrication steps that are used to implement the design into a physical product.

Whereas a design engineer, he deals with

the abstract elements. He deals with device models, and he does not fabricate the components, but he is designing them using different softwares to find out what would be the electrical performance of a system before it gets fabricated so it can do changes in the design, say the width or the length or the line, in order to determine whether the different electro characteristics, such as resistance or capacitance, will affect the performance and whether the system specification at the end will be the desired ones.

Q Do those persons have different backgrounds and skill sets?

A The circuit design and process engineers, well, they start from -- if you start from the field, say, of electrical engineering, the background education is going to be the same.

For example, our electrical engineer students take courses in circuit design, they also take courses in microelectronic technology, so they are exposed to the whole spectrum of what it takes to design a system as well as to fabricate the system.

Now, once such engineer goes into a company, the specific tasks that I will be assigned, they will probably be one or the other. But if he

change positions and if his education has been good, he could move from processing to circuit design and from circuit design to processing.

But after a while, I would think that some people will tend to become known as -- for one aspect and they maybe enjoy doing more circuit design and enjoy doing more process engineer. But it is not one unique answer. It depends on the interest of the people and the opportunity they have in life and so on.

Q Thank you.

Would you consider yourself closer to a circuit designer or a process engineer?

A Well, I am a professor, so -- and I teach courses related to circuit design. For example, I teach the course on very large-scale integration, VLSI. That course deals with the design of circuits that go into electronic systems, but I also have a laboratory that we do actual fabrications and deal with materials and processes, so I am, by virtue of my position, exposed to both.

Q I see.

Do you teach any courses in process engineering for semiconductors?

A I have taught a course, "Microelectronic

Technology," and I taught it several times when I was first started as a professor. Right now I'm teaching a course in VLSI design, and as a part of that course there is a section that deals with the fabrication.

Q I see.

Now, I see from an attachment to your exhibit -- sorry -- your Appendix A on Exhibit 1005, right after page 51, that you've been involved in some patent litigation cases starting in 2001; is that right?

A That's correct.

Q And it looks like in 2001 you were hired to be a witness or an expert for Sanyo against SEL; is that right?

A Correct. I think it was SEL against Sanyo. I am not an expert who is against who. I represented Sanyo.

Q And you were an expert for CMO in 2007 against SEL?

A Correct.

Q And you were an expert in 2008 for CMO?

A Correct.

Q And you were an expert against SEL in a case SEL versus Samsung in 2009?

A Correct.

Q And then you were an expert for CMI in 2011?

A Yes.

Q And you continued as an expert in 2011 for Samsung? Yes?

A Correct, yes.

Q So, in a nutshell, for 12 years, approximately, you have been an expert witness for companies opposing SEL; is that right?

MR. GIBSON: Objection; form.

THE WITNESS: The record shows -- this is what the record shows, but I do not choose the cases. The different law firms come and hire me.

BY MR. MANZO:

Q What is your relationship with CMO?

MR. GIBSON: Objection; form.

THE WITNESS: I have been hired by several law firms to serve as an expert on behalf of the defendants, which happened to be CMO or CMI. And I did not deal with CMO directly, I dealt with the law firms.

BY MR. MANZO:

Q Has your experting work in patent litigation always been against the patent owner?

A So far. The recent -- a new case I have been asked and I have been retained in which it will start, if it doesn't settle earlier, later this year, and in that case I will represent the patent owner.

Q But otherwise not?

A So far, no.

Q You have a relationship with the Display Research Laboratory that I think you mentioned a moment ago; is that correct?

A I am a director of the laboratory.

Q Who funds the laboratory?

A Well, the physical infrastructure, the construction of the laboratory, the utilities for the laboratory, that is funded by the university. The university also pays for my nine-month salary.

I am responsible for raising the funds to cover the actual expenses of consumables and for the salary and tuition of the graduate students that work in the laboratory, as well as for the staff engineer that works in the laboratory.

Q Where does the capital equipment come from?

A The capital equipment comes from a variety of sources. Some of it are been donated by industry, some of it would come -- we buy from

special equipment grants that we get from their regular solicitations from the government, different agencies, or we buy them from the budget of specific research program. If, during the research for that program, we need a particular piece of equipment, we budget that equipment in that -- in the proposal.

Q Please tell me whether you have had any kind of economic support or the Display Research Laboratory has had any support or donations from any of the following entities.

Acer?

A No.

Q ViewSonic?

A No.

Q Vizio?

A No.

Q Westinghouse?

A No.

Q Innolux?

A No.

Q CMI?

A No.

Q CMO?

A No.

Q Professor, without asking you specific

dollar numbers, what portion of your personal income comes from expert work for law firms, as opposed to your compensation from the university for teaching? And, again, I don't want any dollar numbers, just a percentage.

A Well, that percentage, it varies from year to year, and it -- and, as you see, my litigation or patent involvement work or consulting has been sporadic.

So if you are talking about a particular year or you are talking about since 2001?

Q Well, let's start with 2013, year to date.

A The contribution of the patent litigation is significant.

Q More than 50 percent?

A Up to now?

Q Yes.

A It may. I didn't do the calculation. I have to do the calculation.

But this is an unusual year, because the -- some of the legal fees -- some of the work that I've done in 2012 were paid in 2013, so it's always a period before you send in an invoice and you get paid. So in 2013, it reflects work that was done in 2012.

Q Thank you.

What would you say -- between 2001, between the interval of 2001 through 2013, what would you say is the highest percentage in a single year that was represented by compensation for working as an expert witness?

So I'm asking you for a percentage number and a year in round numbers.

A Of the total income earned that year or --

Q Yes.

A -- compared to my academic year salary?

Q Total income earned.

A The highest amount total income earned in any year since 2011 --

Q 2001.

A Sorry. 2001.

Q I'm only asking for percentage, not dollars, again.

A Right, but I haven't done the calculation. That's many tax years I have to try to go back and try to do it.

But in round numbers, I don't know, I cannot give you the exact number, but I would say 30 to 40 percent may have been the highest.

Q Have you been an expert in other

litigations besides patent cases?

A Expert to law firms?

Q Law firms or others.

A I have been an expert and I have a section in my resume that I built, consultant to industry since 1997, so I list a number of companies where I serve as a technical consultant.

Q What page is that on?

A Page 1 of my vitae -- actually, page 51 of Exhibit 1005.

Q I see that you list a number of companies. Have you been an expert witness for any of those companies in litigations?

A You compare this list to the list that I list in my litigations, you see that none of them have been involved in litigation.

Q Professor, the listing in section V is confined to patent cases, and my question is not confined to patent cases.

So there are many other kinds of cases besides patents.

A You're talking about in general legal?

Q Yes.

A No.

Q Okay.

A My only consulting to companies related to legal matters has been the litigation cases that I list in page 2 of my resume or page 52 of 1005, which was accurate as of the writing of that time. It excludes the present case.

Q Have you had any direct discussions with CMO, CMI, Innolux, Acer, ViewSonic, Vizio, Westinghouse about this case?

A About this case? No.

Q And when I say "this case," I mean these proceedings at the patent office, as well as the district court litigation.

A Again, related to this case, no.

Q I'm going to show you several pages, but before I mark, I just wanted to know if these are all related to one another. If they are, I'm going to mark them as a single exhibit.

I'll staple them together if they are from a single place.

A These are pages from our laboratory Web page.

MR. MANZO: Okay. Let me make that a single exhibit, which I'll staple together, as Exhibit 2008.

MR. MURPHY: You said 2008?

MR. MANZO: Yes. I believe that's the next number.

(Deposition Exhibit 2008 was marked for identification by the court reporter and is attached hereto.)

BY MR. MANZO:

Q So your answer is that Exhibit 2008 comes from the website for the Display Research Lab; is that correct?

A Yes, it appears so.

Q And that's a picture of you on the very first page at the top, correct?

A From a long time ago.

Q It looks much the same.

A Thank you.

Q And these next two pictures of doctoral candidates of yours -- or, sorry.

The first one is a doctoral candidate and the next one is a master's candidate; is that right?

A Our website is a bit outdated. The master student is also a doctoral candidate right now, and there is another student that has been hired, and there is a post doc also.

Q Look at the last sheet, please. There are some wave forms.

Do you see that?

A These are IV characteristics. We call them IV characteristics.

Q Okay. I just wanted to identify the page. And then I want to actually look at the page right before that one, the one that starts out, "Polysilicon TFT on Steel."

Do you see that?

A Yes.

Q Professor, the first drawing there is a sectional representation; is that right?

A It is a cross section, a representation, correct.

Q And the top layer is labeled as "Metal-1"; is that right?

A That's correct.

Q It sits on top of passivation oxide?

A That is correct.

Q And I see that there is a transistor shown; is that right?

A That is correct.

Q The transistor has source and drain regions; is that right?

A That is correct.

Q How is metal-1 connected, if at all, to the

source or drain regions?

A Well, in this particular device structure, after we form the source drain and gate regions of the transistor, the whole device is -- structure is covered by an oxide, which is labeled as passivation oxide.

Then there is a lithographic step that is define contact holes, followed by an etching step that opens and removes -- open the contact holes and removes the passivation oxide above the source and drain regions.

Then there is a deposition step that lays down the metal-1 throughout the substrate, followed by a lithographic step that defines the regions where the metal remains.

And upon completion of the etching step, we form what's known as a source and drain electrode. This is the metal-1 regions that are attaching the source and drain regions of the device.

Q So does the metal-1 extend through the opening, the contact hole that you talked about, to reach the source and to reach the drain region?

MR. GIBSON: Objection; form.

THE WITNESS: The metal-1 conformily coats the walls of the holes and the bottom of the contact

hole and establish a region between the two vertical walls of the opening where the metal-1 and the source or the drain is in direct contact.

BY MR. MANZO:

Q Does metal-1 contact the source region or the drain region through the contact hole?

A The metal goes down the metal hole and makes a contact to the source and drain region.

Q Is that referred to as contact through a contact hole in the semiconductor industry, Professor?

MR. GIBSON: Objection; form.

MR. MANZO: Strike that.

Q Is that type of contact referred to as contact through an opening or through a contact hole in the semiconductor industry?

MR. GIBSON: Objection; form.

THE WITNESS: There are many ways to express an opening in a contact hole, and sometimes we call contact hole, sometimes we call them opening, sometimes we call them via. The contact is considered many different ways. Through hole is one way to accurately depict whether you have the hole open directly above -- the hole has been open through the layer that is deposited in between the

two layers that you want to make a contact.

So in the cases where you have an intermediate insulating layer and you need to open a contact hole or the via or form some sort of an opening in the insulating layer, then the metal goes and covers conformily the hole. It has to cover conformily the edges of the hole, otherwise there will be a discontinuity. And even though you may have a metal on top of the passivation and you have a metal in the bottom of the opening, it is not covering the walls of the hole, you will not be able to maintain electro continuity of the metal.

BY MR. MANZO:

Q When you use the word "conform," what do you mean?

A That there is -- as illustrated here in the schematic, that the metal coats the wall of the hole or the opening, so then there is a continuity of the metal from the upper surface of the oxide to the bottom of the opening.

Q In your interactions with people, namely, engineers and the like, during your consulting with any of the companies you listed on page 51 of your declaration, namely, IBM, Kodak, et cetera, did you ever discuss circuit design with the people there?

A Yes, we did.

Q So is there a shorthand way in the semiconductor industry that you are aware of for this type of contact in a semiconductor circuit?

A Well, when we are talking about a device structure, and there are many different ways to fabricate a device structure, we always list the sequence of the layers. We describe the device structure and we list the materials and we list the order with which the materials are laid down. And we have a very specific description of the device structure of how it is made and what is -- in what order the different steps are performed and what order the different layers and materials are put down.

So within that context, words that you mentioned, like through hole, get a specific meaning and been understood by the experts in the field what they mean or ordinary skilled in the art of what they mean.

Q So if one of your students working in the Display Research Laboratory or an engineer at one of these companies with whom you've consulted use the phrase "contact through an opening in an insulation layer," would you understand what they were talking

about?

A If they give me the structures -- and even in this particular device structure that you're referring here, we have two different -- actually, we have more than one metal layer. What is shown in this particular structure is something called metal-1.

In our design we have another layer which we call it metal-0. And the metal-0 goes directly on top of the gate, and then there is a passivation oxide on top of it.

So in that case when we opening the contact holes, we can reveal that layer, namely, the metal-0 below the passivation oxide.

So when we're referring to a structure, it is helpful to understand the sequence of the layers put down so we can understand what we mean by the word.

Q Okay. Well, taking this structure in this figure in this Exhibit 2008, which is before you, does metal-1 contact the source region through the contact hole?

A The metal-1 contacts the source through hole.

Q And metal-1 also contacts the drain region

through a different contact hole; is that right?

A Metal-1 is making contact through hole to drain.

Q How do people skilled in the art refer to those holes? What words do they use? I think you mentioned a few. You said "hole" or "through hole" and "via"; is that right?

A The openings can be called vias, it can be called contacts, it can be contact holes, it can be called cuts.

Q Cut?

A Cut.

For example, in our process, the metal-1 goes to the edge of the substrate and then it is covered by another passivation layer, so that passivation layer is covering the metal-1 completely and we cannot make electrical contact because it is protected by another passivation layer.

And we defined regions on top of those metal regions which we call those metal regions pads -- p-a-d-s, pads. And we're removing the second passivation oxide from those pads -- from above the pads, and we call that glass cut. Glass is the name for the final passivation layer.

So the meaning or the name of those holes,

there are several.

Q I see. You said "glass cut," if I'm not mistaken?

A That's how we call it, yes.

Q Good.

A That's the name of the mask layer we use to define those openings.

Q How many people work at the digital research laboratory?

A You mean the Display Research Laboratory?

Q I apologize. You're right. I do mean the Display Research Laboratory.

A How many people work as of now or --

Q Yes.

A -- how many people went through and completed their degrees through their Ph.D.s?

Q Let's say today. I mean, currently. I don't mean today, July 1, but these days.

A My group, as I mentioned, right now consists of three graduate students, two undergraduate students, one post doc and one research engineer. They spent intermediate times through the laboratory.

Q I'm sorry. I lost you. You said one research what?

A Engineer.

Q Okay.

A He is a lab manager who takes care of some of the processing equipment and performs some of the processing steps in the more sophisticated equipment in the lab.

Q Does the Display Research Laboratory conduct research for industry -- strike that.

Does the research laboratory receive assignments from industry and execute research in response to those assignments?

A We receive funding from industry. Some of the funding comes in the form of sponsor research programs. The sponsor research programs include what you refer to as assignments, but it is not specific assignments. As we define the research area and whether that would be some new material or some new device structures, and we investigate that area.

And in other times we receive funding in the forms of research gifts, which are money that we receive, but that don't have a specific deliverable assigned to it.

Q Professor, you have many published papers, yes?

A I have a number of it.
Q More than a hundred journal papers and conference papers?
A I think it is more than 150, but, yeah.
Q Okay.
A But it's not a world record.
Q Understood.
How about patents, do you have any patents in your name?
A Yes, I have a patent that was issued this spring.
Q What is it about?
A It is about a way to drive a new type of active metrics display called active metrics organic light-emitting diode displays.
Q AMOLED?
A Correct.
Q You're the -- are you the sole inventor?
A One of my -- a former graduate student of mine are co-inventories. His name is first.
Q Is your name in there?
A Yes.
Q Okay. Who is the owner of that patent?
A Lehigh University.
Q Will you share in any royalties that that

patent may receive?

MR. GIBSON: Objection; form.

THE WITNESS: Yes.

BY MR. MANZO:

Q To rephrase, if Lehigh University grants any license or collects revenue as a result of that patent, will you participate monetarily?

A I think I answered yes.

Q Okay. Are there any other patents that are pending or for which -- or which have issued for which you are the named inventor or a named inventor? And I just mean yes or no.

A I'm trying to recollect. I work with a former graduate student of mine who is currently a professor in Taiwan, and he had filed for some patents some time ago, and he had named me co-inventor. I don't know whether those patents have been issued or not, so there may be other patents that I've been named as co-inventor, but those may be Taiwanese patents, but I don't have a good record of those ones.

So either the work at Lehigh, the one that has been issued recently is the only one.

We have filed some invention disclosures previously that are -- well, IP office has a very

limited budget, and we went through a lot of changes over the years. So we're not as efficient in protecting our IP as maybe some other schools.

Q Have you ever considered the question of whether something -- some development was obvious or nonobvious with regard to the patent law of the United States?

A I think these -- all these proceedings deal with this topic that you referred to.

Q So you have?

A That's correct. And also in my previous litigation case, I also done invalidity expert report where the issue of obviousness is relevant.

Q What is your understanding of obviousness in the U.S. patent law as it applies to whatever you've considered?

A There's a specific section in my expert report that gives you a more exact definition. Can I refer to that or do you want me to give you --

Q Before you refresh your recollection, why don't you give me your best recollection as you sit there?

A Because I'm a technical expert, not a legal expert, and I may fail the legal examination, but, in general, my understanding of whether a prior art

renders something invalid or obvious is if the elements in the prior art that are disclosed in the patent, which has been questioned, are expressed directly, explicitly, so if the prior art mention those elements that are claimed as inventions in the patent, or the element that existed in the prior art between a specific piece of prior art or through combination of pieces of prior art would render something obvious; in other words, someone with ordinary skill in the art will be able to combine the knowledge and the structures or materials, whatever they may be, in their particular field and create the part which is claimed as an invention.

How did I do?

Q I just need your understanding, Professor. It's not a legal -- as you said, you're not an expert at the law.

Do you distinguish between whether a patent claim having several elements would have been obvious to a person of ordinary skill in the art prospectively as opposed to retrospectively?

MR. GIBSON: Objection; form.

THE WITNESS: As you said, I'm not a legal expert.

Can you elaborate on what you mean by

"prospectively as opposed to retrospectively"?
BY MR. MANZO:
Q Yes.
Let me strike that question for the moment.
When you were forming your opinion that is reflected in your declaration, Exhibit 1005, you considered various pieces of prior art, correct?
A Correct.
Q Where did those pieces of prior art come from?
A They were provided by the counsel.
Q Were any others provided by counsel than the ones shown in this Exhibit 1005?
A For each patent there was a folder and there was some piece of prior art that will serve between different patents.
I have to refer to my notes. There would be in a handful of patents in this whole list I consider more relevant than the ones that I have listed here from that list, but I am trying to recollect because this was work done back in the fall.
Q Let me see if I can help.
Is it true that you were given the patent and the claims that you were supposed to consider

and a package of prior art to look at? Is that a fair characterization?

A Correct.

Q All right. So how did you proceed from there?

A I was asked to express an opinion on whether the elements in the claims of the '413 are disclosed or are rendered obvious in light of the prior art.

Q So you went to the claim, or a claim at issue, and you said this has 13 elements, let's say, and then you asked where can I find element 1, where can I find element 2, et cetera; is that correct?

A No it is more involved than that one. I first read several times and tried to understood each patent separately. I spent quite a bit of time trying to understand the specifications and the prior art and the entire patent, whatever it disclosed from the abstract all the way down to the claims. And I tried to formulate an understanding of each patent and for both the -- in this case the '413 as well as the two prior art that are used in my declaration report.

Q Okay. So after you read and understood the patents in question, what did you do?

A Then I looked for each one of those or the claims or the limitations -- I went and addressed the claims, because not all claims have been -- what's the right word?

Q Not all claims are challenged?

A Not all claims are challenged. A subset of the claims are challenged or are set forward in this proceeding, so I went to this particular claims and I went to all the elements or limitations of each claim and I tried to see if those are disclosed in the prior art or through combination of the prior art they may be obvious to someone skilled in the art at the time of the invention.

Q So you used 1997 as the time of the invention?

A Correct. Whatever is the -- I don't have the exhibit now, I don't have the exact date, priority dates for each element.

Q Okay. You used the priority date as the date for a person of ordinary skill in the art?

A Correct.

Q What were you doing in the field of semiconductors as of the -- as of 1997?

A Myself?

Q Yes.

A By 1997 I already have been full professor at Lehigh and already have established the research -- the Display Research Laboratory. I was teaching courses and I was conducting research.

Q How much interaction did you have with persons of ordinary skill in the semiconductor arts on a day-to-day basis?

A There's a list in my resume, I have projects funded by industry and we also serve as a consultant to industry and we also have collaboration with industry, even if they're not -- they're not sponsoring our research, many times we do research collaborations.

So I had interactions with people. Would that be on a day-to-day basis? Not day-to-day basis, because I was in academia and they were in industry. But when we have review meetings when we are visiting each other, organizations, when we are meeting at our conferences, and I organized several workshops related to the display -- flat panel displays. So in the meetings at Lehigh or in industry or at the technical workshops or conferences.

Q "Technical workshops," did you say?

A Yes. I listed them in my resume as well.

I serve as the organizing chairman of several such workshops. Two of them were held, actually, at Lehigh, one was a couple hundred people show up in each one of them.

I had a lot of interaction with people with ordinary skill in the art.

Q Let me ask you a few specific questions. Is it your understanding that when a company that is in the business of producing a semiconductor device, a VLSI device, if you will, they generally have lead designers for the new products; is that right?

A You mean lead designers?

Q Yes. Are you familiar that they have lead designers assigned to certain new projects?

A Okay.

Q And are you familiar -- are you aware about whether they have group meetings with their teams to discuss progress in the design field and in the process engineering steps?

A You have specific projects?

Q Yes, specific projects. The next generation of a memory chip, for example, or the next generation of a TFT device or a liquid crystal display device.

A I'm familiar with this general processes,

but the processes that you're referring most related to a specific product.

Q Yes.

A And those specific products are typically confidential to the companies. And very few outsiders, only suppliers or key partners, have exact knowledge of what's going on in those meetings.

Q Is it fair to say that you have not participated in those group meetings?

A For specific products development, no, because I am in the field of -- I'm in research, and so we're always looking at not just the next generation, but we are looking at what will be five or even longer years out in the horizon.

And, typically, in that long horizon, research institutions and companies are a little bit more open and we are having like in the context of a conference, when we have a panel discussion and when we have representatives from both industry and academia telling their opinions about the particular issue that has been questioned.

So I have participated in many such panel discussions and discussions that are dealing with what will be happen next.

For example, you listed in my resume for my website, in my website you refer to this devices that are made on a metal-4 substrate and that's belong to the field of flexible displays.

And, as you know, there are no products right now on the flexible displays, but a lot of people worldwide working in the field of flexible displays and we have been pioneers in that field.

So in that context, I interact a lot with engineers from companies, as well as scientists from academia and government, and have discussion of what are the issues and what are the problems and what we need to address.

MR. MANZO: Why don't we take a very short recess to get some coffee and such.

THE VIDEOGRAPHER: Off the record. We are off the record. The time is 10:11 a.m.

(Recess.)

THE VIDEOGRAPHER: We are back on the record the time is 10:23 a.m.

BY MR. MANZO:

Q Professor, referring to your declaration, 1005, apart from the appendices, it has 50 pages, right?

A That's correct.

Q So my question relates to how this document was prepared. Let's start out with who typed it. Do you know?

A I type and other people contribute to the typing.

Q About how much of it did you type yourself? 10 percent, 25 percent, 75 percent, what?

A You like to talking about percentage, but --

Q Well, a lot, a little, most of it?

A This is my declaration. I took sections or guidance or input from other people in legal matters, because I'm not aware of these proceedings. These are actually pretty new proceedings. I've never been involved in inter partes review before.

I was given a general format, but I would not try to say that this is someone else piece of work. This is my piece of work.

Q How long did it take to produce Exhibit 1005?

A I've been involved in preparing five declarations for the five patents that I have been involved. I think we started in October, if I'm not mistaken, and then the last one was filed, I think, in early December.

So in that time frame there were five declarations that were prepared. I don't remember how many days or exact weeks, but you can take the average and you can see how much time was spent roughly.

Q Did you look at drafts and make markups and return them to somebody else?

A I was, for example, provided with a vitae that the counsel was -- pulled from a previous report of mine, and I said, "That's not the right one, that's not updated," so I had to fix that part.

But there was a lot of things discussed in these proceedings, and these are my opinions, these are my report.

Q About how many revisions did the document go through, this particular Exhibit 1005, how many iterations?

A There were five -- five reports. I don't remember how many revisions each one of them had.

Q Okay. Fair enough.

And you said these were prepared over the course of about two to three months; is that right?

A That's my recollection.

Q Professor, I'm handing you what Innolux submitted as Exhibit 1001, which is the

'413 patent at issue in this proceeding.

Do you recognize it?

A Yes, I do.

Q Could you please turn to the claims, and particularly claim 1, which you will find at the last part of column 14.

Do you see that?

A Yes, I do.

Q Why don't you take a moment to reread claim 1 to yourself, please.

Have you read through claim 1?

A Yes.

Did you also give me that one?

Q I'm handing you now a copy of the petition submitted by Innolux in this matter entitled, "Petition for Inter Partes Review of U.S. patent No. 7,876,413," et cetera.

Do you have that?

A Yes.

Q And if you look at that, you'll see that Innolux has reproduced the claims and given the separate paragraphs a numbering system.

For example, claim 1, appearing at pages 16 through 23, is broken into different rows, and the rows are numbered.

Do you see that?

A The claims?

Q Yes, at claim 1, it starts with 1.1, "A liquid crystal displays device comprising," and then 1.2 is the next row, and it's, "A first wiring over a substrate."

So do you see the numbering system?

A Yes.

Q Okay. Good.

Because I'm going to refer to those numberings, if I may.

So I'll -- claim element 1.2 on page 17 recites, "A first wiring over a substrate" --

A Excuse me. You mean on page 16 and 17?

Q Yes.

A Are these the claims charged for APA in view of Sukegawa?

Q Well, I'm not referring to the right-hand column --

A Okay.

Q -- only the left-hand column, which is the claim knowledge.

A Okay. All right.

Q And, theoretically, the two different claim charts should have the claim reproduced the same

way, don't you agree?

A On the left-hand side, yes. The right-hand side would be different.

Q So claim element 1.2 is for a first wiring over a substrate?

A Correct.

Q Now, in the context of this patent which you've studied, does the substrate have to exist before the first wiring is placed over it?

A Of course.

Q Okay. In section 1.3 it calls for a first insulating film over the first wiring. In the context of this patent, does the first wiring have to exist before the first insulating film becomes over it?

A Assuming that there are no other layers that are formed after the first wiring, then -- well, strike that one.

Q I'm only asking you if one is preexisting, that's all.

A Let me see your question.

Q Let me restate the question for you. My question really relates to the sequence, Professor.

A Okay.

Q Does the first wiring have to exist before

the first insulating film in this claim element 1.3 in the context of this patent?

A It says the first insulating film over the first wiring, so that implies that the first wiring comes first and the first insulating film comes afterward.

Q Okay. Moving on to the next claim element, 1.4, is it also true that the substrate and first insulating film have to exist before the second wiring is placed over them?

A Yes.

Q Looking at claim element 1.5, does the second wiring have to exist before the second insulating film is placed over it or somehow provided over it?

MR. GIBSON: Objection; form.

THE WITNESS: The second wiring has to exist before the second insulating film comes over it.

BY MR. MANZO:

Q In 1.6, does the second wiring have to exist before the transparent conductive layer is provided over it?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Let me restate.

Is there an implied sequence in section 1.6 -- or claim element 1.6?

A What do you mean by "implied sequence"?

Q Must one of these two things come before the other? Namely, one of them being a transparent conductive film, the other one being the second wiring.

A Well, in this 1.6, as well as in many of the previous ones, we describe and we refer to two elements. And if you're referring to the sequence with the specific reference to those two elements, then an implied sequence exists, but only which refers -- to elements that are referred. There may be other elements that may exist and they may be laid down before the second piece is laid down.

So referring to a sequence -- referring to certain sections, and these sections refer to its contained two elements. And the language that exists in each section implies a sequence, but the sequence, as far as to those two elements, in particular. There may be other elements that may exist and --

Q Yes, I understand. I'm not asking about -- I'm not asking whether there are any intervening

steps. I'm just asking about is there one before the other.

So would you say about 1.6 that there is one before the other?

MR. GIBSON: Objection; form.

THE WITNESS: The first region of the -- the second wiring, it comes first, but before the transparent conductive layer comes down, there may be other layers that are laid down and then the transparent conductive layer comes down. Or -- and so in this case we are referring to the sequence of those two elements and we forget all the other ones.

So you're asking me about if the first -- if the second wiring comes before the transparent conductive layer, the answer is yes. But whether the transparent conductive layer touches the second wiring, comes immediately after the second wiring or there are other layers in between, that will determined by, perhaps, the other claims, the other limitations within the claim.

BY MR. MANZO:

Q Okay. Thank you.

Let's look at 1.7, which is for, quote, a flexible printed circuit over the first wiring and the first region of the second wiring, semicolon,

and closed quote.

Is there an implied sequence of anything coming ahead of the others in that section 1.7 of the claim?

A That the flexible printed circuit comes last, and that it is -- and before you put down the flexible printed circuit, you already have put down the first wiring and the second wiring.

Q Okay. And in 1.8, which reads, quote, a sealant over the first wiring and a second region of the second wiring, closed quote.

Is there any implied sequence there, Professor?

A That the sealant comes last, after you put down the first wiring and the second wiring.

Q Okay. Thank you.

Can you skip down to page 21 of the petition and look at element 1.11.

I'll read it into the record. "Wherein the first wiring and the second wiring are in electrical contact through an opening in the first insulating film."

Did I read it correctly?

A Yes.

Q Okay. Does that provision or that recital,

element 1.11, call for the first insulating film to exist before the contact is made?

A This particular section taken out of the context of the previous sections that we referred to or in light of the previous section that we referred to?

Q In light of the entire claim and the patent, please.

A In light of the sections that we have just read, there is an implied order that we have just discussed. And that order dictates that you first have the first wiring, then you have the first insulating film, and then you put down the second wiring.

In that sequence, the first insulating film has been placed in between the first wiring and the second wiring, so that is what is implied by the previous sections that you have just read.

Q Is that how a person ordinarily skilled in the art in 1997 would have understood these words in this patent if it had existed in 1997, in your opinion?

A As I said earlier in the discussions, in the morning before the break, the exact sequence of the order of the layers that are laid down is

important for someone to understand the structure that is described.

And I gave you the example that in our laboratory you have two different metals, metal-1 and metal-0. The metal-1 comes on top of an insulating layer, the passivation oxide, or the metal-0 comes -- touches with the gate electrode and then the passivation oxide goes on top of it.

So an implied order of things cannot be taken in absence of more detailed description of the structure.

Q I'm confused. Are you saying, Professor, that a person in 1997 who is ordinarily skilled in the art would not have understood this claim element the way you just described it or would have? It has to be one or the other.

A Understood what?

Q The meaning of 1.11.

A I think the meaning of 1.11 is one thing and the thing you are asking about, the sequence, the implied sequence of layers, and that's a different thing.

Q Okay.

A Did I understand your previous question and your last question? I think you asked me first

about the sequence and now you're asking about the meaning.

Q Fair enough. I was not trying to separate them. I was trying to ask you that when you explained the sequence that you found in 1.11, whether somebody ordinarily skilled in the art in 1997 would share the same view with you. It is not a trick question.

A No, I understand you're not asking trick questions, but I'm asking whether 1.11 by itself describes a sequence, and my answer is 1.11 by itself does not describe an explicit sequence. The previous sections that refer to, those describe a specific sequence.

The meaning of 1.11 is that the first wiring and the second wiring are in contact and that they are in electrical contact, that the exact sequence of the three layers, namely, the first wiring, second wiring and first insulating film, is not implied by 1.11 alone.

Q Understood. We want to understand the claim in the context of the other parts of the claim.

Now, in the context of the entire claim, what is the meaning of electrical contact through an

opening in the first insulating film as it appears in 1.11?

A Well, in the context of the entire claim and in the sequence that is described in detail by the earlier sections of claim 1, the meaning of the electrical contact through an opening in the first insulating film in this particular limitation is referred to that the electrical contact will occur because of the opening in the first insulating film.

The two layers are separated by an insulating film. And in order to have an electrical contact between them, one has to first open an opening in the first insulating film.

Q I understand. Thank you.

I want to ask you, finally, about the final claim element, which you'll find on page 22, namely, claim element 1.13, which states, quote, wherein the second wiring and the transparent conductive layer are in direct contact through an opening in the second insulating film, closed quote.

Do you see that?

A I see that.

Q And just for completeness, why don't you read to yourself the element between the, namely, 1.12 so that we don't skip anything.

Tell me when you're finished reading that. And after you've read that, I'll ask my question.

A Go ahead.

Q Okay. So my question is: Does section 1.13 require the second insulating film to exist before the second wiring and the transparent conductive layer are in direct contact through an opening in the second insulating film?

A Can you explain your question?

Q Yes.

I'm asking whether there is an implied sequence in 1.13 in the context of the whole claim.

A A sequence between which layers?

Q Well, it's a broad question. Any sequence at all.

A Well, if we look at 1.13, there are four elements that are included -- the second wiring, the transparent conductive layer, an opening and the second insulating film.

If you're asking me if there is a prescribed sequence, that prescribed sequence is not clear by 1.13 alone.

Q What about 1.13 in context of the other claim elements of claim 1?

A Okay. 1.13, as in 1.11, the statement not

prescribe the specific sequence.

In the case of 1.11, we look at the previous limitation stated in the claim, and we identify a prescribed sequence.

If we look at the element of the limitations that are disclosed before 1.13, someone skilled in the art will understand there is no prescribed sequence, other than saying that the -- that both the transparent conductive layer and the second insulating film are both over the second wiring, but it does not prescribe a sequence which is right above, which one is in direct contact and which is above the other.

If nothing else, the language in 1.13 is slightly different than 1.11. In 1.11, in light of the previous layers, previous limitations, it was evident that the first wiring and the second wiring are not in electrical contact, because there is the first insulating film in between that it was explicitly stated by referring to the earlier limitations. So an electrical contact in the context of 1.11 is enabled by the opening.

1.13 is referred to direct contact, and direct contact may imply that the transparent conductive layer is for right on top of the second

wiring, and then the second insulating film is on top of the transparent conductive layer. So even though there are the second wiring, the transparent conductive layer in direct contact, that direct contact is revealed when we form the opening.

That direct contact appears when the opening is formed and the direct contact exists between the vertical walls of the opening.

Q So is it fair to say that -- let me ask about the contrapositive.

Is that a word that you're familiar with?

A No.

Q Okay. Is it correct to say that without the opening that's referred to in 1.13, there is no direct contact of the second wiring and the transparent conductive layer -- question mark?

MR. GIBSON: Objection; form.

THE WITNESS: I do not agree with your statement. A direct contact may exist before the opening that the claim requires also other -- the claim requires other things.

For example, it requires the flexible printed circuit to be in direct -- to be in electrical contact through the transparent conductive layer to the second wiring, that's 1.12.

So if you have a second insulating film on top of the transparent conductive layer, an opening is required for that electrical connection between the flexible printed circuit and the second wiring.

BY MR. MANZO:

Q And without such an opening, what happens?

MR. GIBSON: Objection; form.

THE WITNESS: What happens with respect to what?

BY MR. MANZO:

Q With respect to the direct contact.

A There are three layers -- the second wiring, the transparent conductive layer and the second insulating film. There are two ways those layers can be put down, since we know already that both the transparent conductive layer and the second insulating film are over the second wiring.

So there is enough information in the claim to someone skilled in the art to understand that the second wiring comes first.

And then the other two layers, the transparent conductive layer and the second insulating film, follow, but there's no implied order or there's not enough information for someone skilled in the art to see that an order, a specific

order, is required.

So someone skilled in the art will then create the sequence in one of two possible ways. Either you put down the transparent conductive layer on top of the second wiring first and then put the second insulating film as the final layer, or you put the second -- you put the second insulating film first on top of the second wiring in direct contact with the second wiring, and then you will put down the transparent conductive layer on top of the second insulating film.

Q Don't you need to have the opening?

MR. GIBSON: Objection; form.

THE WITNESS: In the first sequence I described an option where the transparent conductive layer is on top of the second wiring and in direct contact with it, and then you put down the second insulating film.

The second wiring and the transparent conductive layer, already in direct contact, wherever those two layers start, because they may have different extent as there for preparation for informationary process.

In that case, they are in direct contact, and the opening serves to expose the direct contact.

BY MR. MANZO:

Q You're saying that in option A there already was direct contact between the transparent conductive layer and the second wiring, and the opening exposes that contact; is that what you said?

A Correct. Between the vertical walls of the opening we will see the two layers being in direct contact.

Q Is the specific order as between -- strike that.

Do the other elements of claim 1 give us the specific order that must follow with respect to options A and options B?

A In this limitation 1.13, in contrast to the previous limitation that we were discussing, 1.11, there is not enough information -- sorry.

The language -- strike.

The language used is broad enough that it covers both options.

Q But, if I may suggest that you look at 1.5, and doesn't 1.5 tell you that there is second insulating film over the second wiring, and section 1.6 says, "and then there is transparent conductive layer over a first region of that second wiring."

Doesn't that rule out option A?

A No, because the language here is broad. It states that both are over the second wiring, but does not -- do not prescribe or do not require a specific sequence.

Q Okay. Let me ask you another question.

What words would you or a person of ordinary skill in the art in 1997 use to describe that the contact between the transparent conductive film and the second wiring occurs because of the opening in the second insulating film?

MR. GIBSON: Objection; forms.

BY MR. MANZO:

Q Professor, I may have said "transparent conductive film" when I meant "transparent conductive layer."

So can you accept my question with that modification?

A Yes.

Q Thank you.

A Your question stated that the contact is because of the opening. The claim requires through an opening. So your question construe that word "through" in a specific way, and that way is not supported by the information of the limitations, at least what is in the claim 1.

MR. MANZO: Okay.

THE VIDEOGRAPHER: We're going off the record. We are off the record, the time is a.m. on July 1st, 2013. This is the end of video number 1 of the continuing deposition of Dr. Milt Hatalis.

(Recess.)

THE VIDEOGRAPHER: We are on the record. The time is 11:27 a.m. on July 1st, 2013. This is the beginning of video number 2 of the deposition of Dr. Milt Hatalis.

BY MR. MANZO:

Q Professor, before the changeover, we were discussing section 1.16 of claim 1 of the '413 patent. And I think you have indicated that it's your opinion that there's -- from the wording of the claim, two different possibilities exist as to the connection between the second wiring and the transparent conductive layer.

Is that a fair characterization of what you've said?

A That in light of the language of the claim in the earlier part of the claim, the order with which the transparent conductive layer and the second insulating film are deposited over the second

wiring is broad, so the exact order can be one of two different ways. And depending upon which way they word "through" may construe a different way.

Q I understand. And how would a person of ordinary skill in the art have understood this phrase about direct contact through an opening in the second insulating film in the context of the entire claim and the patent in 1997? So I'm asking you specifically about the opening part of this claim language.

A You asked me to construe the word "through" or you asked me to construe the word "opening"?

Q I'm not asking you to construe. I'm asking you how a person in the ordinary skill of the art would understand this claim element in light of the entire patent and the claim as a whole with regard to the recital "direct contact through an opening in the second insulating film."

A In light of the entire claim, it will mean that in order to create the system -- and the ultimate goal here is to create an electrical contact to the flexible printed circuit. And because there are many conductive layers and many insulating films put down, that openings are required.

And, in particular, 1.13 means that through the opening, a contact -- through the opening the second wiring and the transparent conductive layer are in direct contact.

So another layer, in this case the flexible printed circuit board, can come down and make electrical connection to them.

Q Now, when you just used the word "through," did you mean through in the sense of "viah" or "vee-a"?

A The word "through" can be construed in a number of different ways, and via is one such way, which means by means of. But "through" could also mean between, it also means what you mentioned earlier, because of.

The language is broad enough that all these meanings are valid meanings to the word "through."

Q Professor, have you ever heard anybody in the semiconductor arts use the word "through a contact opening," and mean through as anything other than via or because of, somebody who is actually skilled in the semiconductor arts?

MR. GIBSON: Objection; form.

THE WITNESS: Excuse me?

I'm not receiving the transcript.

Thank you.

The meaning of the word "through" is because of -- or via is determined whether the sequence of layers, of all the layers, all conductive layers and all insulating layers, that exist in the structure will be such that will support because of.

And that was the case for 1.11 where the order of the first wiring and the second wiring and the first insulating film were such, and that order was specifically stated that you have first the first wiring, then the first insulating film and lastly you had the second wiring.

So in that context, the word "through" means because of, that in the context of 1.13, or in general, because you refer to semiconductor art in general, in the absence of specific description of the structure and specific sequence of the orders that come down, the word "through" may mean more than one thing, because the contact -- sorry -- because the two layers may touch each other, but they are covered by an insulating film, they are not exposed. And if another electrical connection is required, that opening is the one that will -- that will break wire to make that other connection, in

this case to the flexible imprinted circuit board.
BY MR. MANZO:
Q I understand what you're saying, Professor, but my question was how a person skilled in the art would understand the word "through" in this phrase, in this claim with regard to direct contact through the second insulating film.
And, if you remember, I asked you if you ever heard anybody use it in the way that you've just described.
MR. GIBSON: Objection; form.
BY MR. MANZO:
Q So my question, Professor, is have you heard somebody ordinarily skilled in the semiconductor fabrication art use the word "through" in the phrase "contact through an opening in an insulating film" to mean anything other than the contact opening being the cause of the contact?
A Are you asking me to recall every conversation in which the word "through" may have come up --
Q No. I'm not asking about the word in the abstract, I'm asking about this phrase in particular.
A Right. And, as I said several times by

now, in semiconductor art, people involved in that field with ordinary skills, when they refer to a structure, they're not refer to a structure with just abstract words, they refer to a structure that describes a structure, they list the material used in that structure, they list the process, the sequence of the processes. And in that context, the words take specific meaning.

And I gave an example, when the first wiring is put down followed by the first insulating film, followed by the second wiring, the electrical contact is because of the opening. But that implies a specific sequence of an order in putting down the materials for as long as that order is there, and is such that the first insulating film is interposed in between, the word "through" takes the meaning that you referred to.

Q Okay. Well --

A And the language in this claim and in other claims have instances where the information is such or the language is specific that that sequence is evident.

In this particular claim, both layers are over -- both the transparent conductive layer and the second insulating film are over the second

wiring.

There is no information in the claims or in the specifications to dictate the specific sequence in order to limit the structure in a particular embodiment.

Q So is your answer, yes, you have heard people skilled in the art use the word the way you've just explained?

MR. GIBSON: Objection; form.

THE WITNESS: In cases where the insulating layer is in between the two conductive layers, yes, I have heard it to be used through an opening to mean because of.

BY MR. MANZO:

Q Okay. Now, if you look at the patent, which I placed in front of you earlier, I think you should still have a copy there, when a person reasonably skilled, ordinarily skilled, let's say, in the semiconductor fabrication arts or semiconductor arts reads this patent, including looking at the drawings, and sees this phrase in claim 1, namely, the phrase of 1.13 we've been talking about, in the context of this patent, rather than some abstract other structures, does the phrase, "direct contact through an opening in the

second insulating film" mean that the contact occurs as a result of the opening in the second insulating film and not otherwise?

MR. GIBSON: Objection; form.

THE WITNESS: In the context of the '413, where many layers and relationship between those layers is described, there are sections and specific limitations within the claims that dictate or require a specific sequence. And in those cases the word "through" means because of. And someone with ordinary skill in the art will see that order being required and that order being described clearly and will not leave any room for other meaning of the word "through."

But those are -- but in this particular section related to the second conductive -- second wiring and the transparent conductive layer and the second insulating film, the language is broad.

And in that broad language, as we discussed earlier, there can be two ways to build the structure. And you cannot -- I couldn't find any information to say that one is more likely than the other one, that the patent limits to one and not to the other.

BY MR. MANZO:

Q Okay. Let me invite your attention to column 13, line 44, please.

Do you see the word "through" there on line 44?

A It says, "by a spacer or the like which penetrates through the resin inter-layer film because of a pressure applied thereto."

Is that what you're referring to here?

Q Yes.

A Okay.

Q Is the word "through" in claim 13 -- I'm sorry -- in claim 1, element 1.13, used in the same sense as it appears in column 13, line 44?

A The section refers to a spacer that penetrates through the resin, so I think the word "through" in this section means that the resin goes in from one side of the resin and out to the other side of the resin. In other words, the spacer extends throughout -- throughout the resin, so I don't think that word "through" is the same as what we were discussing earlier.

Q Professor --

A In other words, you cannot construe because of spacer which penetrates because of the resin. In this context, as you see, the meaning, because of

for the word "through," doesn't have any context.

Q Let me ask you a hypothetical question.

Going back to claim 1, which you can look at in the patent, so at the very bottom of column 14 it contains the language we've been discussing, namely, "The second wiring and the transparent conductive layer are in direct contact through an opening in the second insulating film."

If I had changed the word "through" to the word "via," would it change the meaning that you understand?

A Which meaning?

Q Well, you've testified that in the context of this patent, the word "through an opening" -- or the phrase "through an opening" can be interpreted two different ways in terms of the structure, I think. And I'm asking you if I make a change in the language, whether it results in a change in the interpretation. And the specific change I'm inviting or calling to your attention is changing the word "through" to the word "via," or some people pronounce it "vee-a."

Do you understand my question now?

A I understand your question.

Q Okay. What do you think?

A I'm not sure all the different ways that the word "via" can be construed, but, in general, you're taking a section of the entire claim in absence of the information that is described within the claim, and you try to limit a structure to a particular structure. And to do that, I don't think you -- I mean, you can do it, especially with a word, and if you choose the right word, maybe you can lead someone skilled in the art to understand a specific structure is the one that is referred.

But, in general, the information of the entire claim is relevant.

Q Well, I don't mean to take a phrase out of context of the entire claim. I do want you to construe my hypothetical in the context of the entire claim and the patent as a whole.

A You asked me to construe the word "via"?

Q I'm asking you if the word -- instead of the word "through" at column 14, line 66, if the word, instead, were via would it have a specific meaning for you and the person in the ordinary skill in the art, namely, that the contact we are talking about, the direct contact, occurs by virtue of the whole.

A I'm not a language expert, so I do not

think that I am qualified to construe words in absence of a dictionary or some study of the meaning of the words and relevant meaning.

Q Fair enough.

A If you -- go ahead.

Q I'm asking how a person of ordinary skill in the art -- let me ask.

How would a person in the ordinary skill in the art convey the idea that it is the contact that permits the open -- no, that it is the opening that permits the contact to occur?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q In this particular contact we are talking about.

THE WITNESS: If the sequence of the layers is listed in a specific way, similar to the way that the other layers that we discussed earlier were listed -- so, for example, first wiring, first insulating film over the first wiring, a second wiring over the substrate and the first insulating film -- you see, in this case you list the layers and you list, specifically, the order with which the layers are put down, and then you explicitly state that the first insulating film is in between the

first wiring and the second wiring.

So, in that case, the word "through" -- and that word "through" appears in the limitations. It says, "Wherein the first wiring and the second wiring are in electrical contact through an opening in the first insulating film," so in view of the limitations listed above would describe a specific sequence, the word "through" means because of.

In this case, it lists two layers, a conductive layer and an insulating layer above the second wiring, and it does not dictate a specific order.

So someone with ordinary skill in the art will understand there are two ways to build that structure. And only one of those two ways the word "through" means because of.

BY MR. MANZO:

Q Well, if I change the word "through" in 1.13 to the words "because of," would that be enough to mean that it is only because of the opening that the contact occurs in section 1.13?

MR. GIBSON: Objection; form.

THE WITNESS: I think if the inventors wanted to have a specific language to interpret -- to construe the word "through" is "because of," the

inventors could have listed the order of the layers in the earlier parts of the claim in such as they've done for the first wiring and the second wiring and the first insulating film. They could have list the order between the transparent conductive layer and the second insulating film so that whatever apply earlier, it can also be applied for this one.

So, in other words, you don't, necessarily, need to change the word "through" here to mean because of, but you can just list in the earlier part more specific order with which the layers will be put down.

So, for example, if you say "a transparent conductive layer over a first region of the second wiring and over the second insulating film," then all the discussion that we had for the last two hours would be irrelevant, because then someone with ordinary skill in the art would understand that the second insulating film is in between the second wiring and the transparent conductive layer, hence the opening is because -- hence the contact because of the opening.

But, in that case, it would be more elegant also to change the word "indirect contact" to what was listed earlier and refer to as an electrical

contact. Because if you have the two layers, one above the other, and you have an insulating layer in between and you have contacts, then the two layers are an electrical contact -- sorry -- yes, the two layers are in electrical contact.

In other words, the entire layer is in the same potential as the other layer, and not only where they are in direct contact.

So the direct contact here is a little bit confusing what it means.

Does it mean that the one transparent conductive layer to overlay completely the second wiring or do you want the transparent conductive layer to be an electrical contact?

So I would change the sequence of the layers and I would change the word "indirect contact" with the term "electrical contact."

And that part is also used, the part of electrical contact is listed in two limitations, in the one that says, "the first wiring and the second wiring on electrical contact through an opening in the first insulating film," and is listed, "wherein the second wiring and the flexible printed circuit are in electric contact through the transparent conductive layer."

In both those cases, the two elements, they are not in direct contact, they are in electrical contact, because there is something else between the first wiring and the second wiring, there is an opening. And in the second case there is the transparent conductive layer in between the second wiring and the flexible printed circuit.

BY MR. MANZO:

Q Professor, why don't you look at the figure that's on the cover of the '413 patent, the first page, and I think you will see that is Figure 4A. You can look at either one.

Isn't it correct to say that in this figure the -- there is a substrate, 101, and there is a first electrical layer called auxiliary lines, 401; is that right?

A Yes.

Q And above that is a first insulating film, 112; is that right?

A Yes.

Q And there are openings that are in insulating film, 112, right, contact openings?

A Correct.

Q And above layer 112 is the second electrical wiring, marked as 403, external

connection lines.

Do you see that?

A Yes.

Q And that second -- sorry. Strike that.

And those lines, 403, make electrical contact with line 401 through the openings of which three are shown in that figure; is that right?

A Correct.

Q Okay. Now, above -- on the top of the second wiring, 403, on the left side, do you see a resin inter-layer film, 113, right?

A Yes.

Q And on the right-hand side of the figure you see above this external connection line, 403, you see an ITO film, 114, above which is the flexible printed circuit, 107; is that right?

A Yes.

Q Now, on this figure, is it fair to say that electrical contact of the ITO film, 114, with the external connection line, 403, is because of an opening in the resin inter-layer film, 113?

MR. GIBSON: Objection; form.

THE WITNESS: As we discussed earlier, there are two ways to put down ITO and this insulating film called resin.

So in this drawing, 113, the insulating layer is right above 403, the external connection lines, since the contact between 114, the -- the electrical contact between 114 and 403 is because of the opening. Because if it wasn't the opening, the 114 would be laid above the insulating film, 113.

But this is one of two possible ways of constructing the structure.

BY MR. MANZO:

Q What's the other way?

A The other way is to put 114 right above 403, and then put the 113 above 114.

Q But that's not how it's shown in this figure, is it?

A No. This figure is one embodiment. But the claim language is broad, that it covers both embodiments.

And there is nothing in the specifications to describe that structure, either. The language in the specifications is as broad as the language in the claims.

In this particular case there is nothing in the specifications, either, to help someone construe the word "through."

Q Does the specification use the word

"through" in the sense that you've been using it as a possibility?

MR. GIBSON: Objection; form.

THE WITNESS: Referring to the Figure 4A, the only relevant sections that I found is in column 8, and it reads -- column 8, line 52 to 55, and it reads, "Referring to FIG 4A, the external connection lines 403 are electrically connected to an FPC, (flexible printed circuit) 107 through contact holes provided in the resin inter-layer film 113 through an ITO (indium tin oxide" film 114."

That's the only part that I found. And in this case the word "through" clearly mean because of the contact holes in the resin, because the resin can be construed -- can be applied above the other embodiment that I described.

So if you have the ITO on top of the external connection lines and you have the resin above that part, then you will cover the metallization of the substrate.

So you need contact holes to expose the metal lines in the substrate, the external connection lines in the ITO, in order to make the electrical connection to the flexible printed circuit.

So the section I referred, it can cover both embodiments.

(Deposition Exhibit 2009 was marked for identification by the court reporter and is attached hereto.)

BY MR. MANZO:

Q Professor, do you recognize Exhibit 2009?

A Correct.

Q Do you recognize it as a semiconductor structure?

A What do you mean by "semiconductor structure"?

Q Is that what's shown in this figure?

A It is wiring elements and insulating elements. There is no insulating -- there is no semiconductor material disclosed in this particular section.

So you're referring whether it is a microelectronics structure used in the field of making semiconductor devices, the answer is yes.

You're asking whether there is any semiconductor material, I do not recollect seeing any semiconductor material in Figure 1B.

Q Okay. Thank you for that clarification.

Now, this is a figure from the Sukegawa

reference; is that right?

A Correct.

Q So let's identify what some of these structures are.

A May I refer to the entire Sukegawa reference?

Q Of course. Let me give you a copy of that.

I'm handing you a copy of Exhibit 1003.

Let me just ask you to confirm a couple of things, preliminarily. The part marked number 2 is a metal wiring; is that right?

A That's correct.

Q And the part number 3 is insulation?

A That's correct.

Q And the part 7 is wiring?

A Correct.

Q And the part 8 is a transparent conductive layer?

A Yes.

Q And part 9 has been called a protective layer, or what would you call part 9?

A It's another insulating layer that serves as passivation.

Q Okay. Does Sukegawa suggest that it be nitride, do you remember?

A I believe so. That's an insulating layer.
Q Okay. What is part 6?
A Part 6 are openings in that insulating layer labeled element 3.
Q Is there an opening in the protective layer or the passivation layer 9?
A Yes.
Q Would you call it a contact opening?
A It is an opening, something is going to come in contact; you can refer to it as a contact opening.
Q Okay.
A But, as I said earlier in my testimony, different openings have, in the art, different terminology. In my lab we call that glass cut and I believe in the industry we call it also glass cut. We generally refer to them as openings.
Q So the opening in 9 is something you refer to in your lab as a glass cut; is that right? Is that what you said?
A Without making connections to flexible printed circuit in my lab, but we have different -- we refer to openings with different names, so then we can understand with what opening we're referring to in the structure.

So in my lab we call one contact -- actually, I call them active contact, we call another one via and we'll call another one glass cut. I recollect three names. We call them all contacts, we have different language. Which contact were you referring to?

Q I'm referring to the contact -- I'm sorry -- I'm referring to the opening in 9.

A I understand. So that opening can be called opening, it can be called contact, it can be called glass cut. I don't know how the engineers at NEC may have labeled that opening or name that opening. I gave you names that we use in our laboratory to refer to a specific opening. We call them all openings or contacts.

We have to use words and describe which one, so sometimes we refer to them as -- we give them specific names. But that's for convenience purpose.

Q Thank you.

So with reference to Exhibit 2009, can you point out the -- do the words "metes and bounds" carry a meaning for you? Do you understand that phrase?

A No -- I may have heard it in other context,

but --

Q Okay.

A -- perhaps use it more specific.

Q Can you please delineate the opening in region 9 or film 9 on Exhibit 2009?

A Indicate the opening in Figure 9?

Q Indicate the opening --

A Sorry. In Figure 1, the opening in the element labeled 9?

Q Yes, please.

A I think I've done that in my declaration.

Can I refer to my declaration?

Q Sure.

A It's a different figure. Whatever is -- the figure is the same, the underlying structure is the same, but Figure 2, she has other elements on top of it.

Q Well, I have a copy of 2, which we can get to in a minute.

A Okay.

Q But in your declaration you gave us a double-headed arrow that shows us the left side and the right side of the opening, I think, or tells us where they are.

Do you understand what I mean?

A This one?
Q Yes.
A Yeah.
Q So what I'm really asking you to do is to tell me where the rest of the opening is.
You've shown us horizontally. Where is it vertically?
MR. GIBSON: Objection; form.
THE WITNESS: That would depend on the layout of that particular element. So how far that contact extends outside the plane where this one is indicated would depend upon the planar section view, and I cannot say just from the cross section, if I understand your question well.
BY MR. MANZO:
Q I probably haven't explained it very clearly. Let me try it a different way.
Can you draw a box on the exhibit to show us where the opening is in layer 9 at this particular cross section?
A You mean a box, meaning a 3D object?
Q No, not 3D. 2D.
A In semiconductor art, you involved in semiconductor art as we discussed, you have friends in that field, you may be familiar that we use terms

such as a layout. So layouts are 2D representations of the structure. And this tells us where the opening is, how -- what is the length and width of that opening.

So from a cross section you are only going to be able to get a 1D representation of the opening; in other words, tells you what is the length in this direction where that cross section was taken.

The Z direction only refers to the thickness of the film, and that's something that in the processing we use timing.

There is nothing in the -- it is not something in the design that we use to refer to the opening, at least in the mask design. I'm not -- maybe I am sounding too technical here. Please guide me and help me what you exactly want me to do.

Q Okay. I wasn't really thinking about the mask or the layout that you would see from above, but rather just in this cross sectional view I'm trying to understand the horizontal and vertical limits of the opening in the part number 9.

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Can you tell me what those are?

MR. GIBSON: Objection; form.

THE WITNESS: Well, in general, the vertical limits are the walls of the layer, and these are the -- so we go to one end of what we define from the mask as being the start of the opening, and then we go to the other end, the opposing end in that direction, let's call that the X direction. And then we go in the 3D structure or in the cross section of the structures, and we look at the thickness of the layer in that region and we then say, okay, if D is the thickness of the layer, then the depth in that -- of that contact is D. Or it can be a micron or half a micron or a hundred nanometers or whatever that number is.

Is that what you're asking me to do?

BY MR. MANZO:

Q Yes.

A And that thickness typically is required by the process engineer to adjust the etching time so that the etching time can then be appropriate for etching and removing the layer to form the opening.

So the -- in that contact, if I understand the context of your question, the two opposing ends of the contact are -- one is the vertical wall that is between the numbers 8 and 9, and the other one is

opposing end to the other -- to the far right of that structure.

Q Would you please delineate the contact opening -- or the opening in 9 with this red pen, please, on Exhibit 2009.

A So what, exactly, do you want me to delineate?

Q The opening in the layer 9.

A In the Z direction or in the X direction?

Q On this piece of paper.

MR. GIBSON: Objection; form.

THE WITNESS: Right. In the Z direction or in the X direction?

BY MR. MANZO:

Q Both directions.

All right. Further considering -- just to clarify, you drew a horizontal line with two arrows, arrowheads, and a vertical line with two arrowheads?

A Right.

Q So in the horizontal line, are the arrowheads at the vertical walls of film 9, one over on the left side and one over on the right side of the figure? Is that where the opening stops?

A Can you repeat the question?

Q I just want to clarify that the opening

stops at these vertical walls that you testified about earlier, the opening in 9.

A The lateral extent of the opening in 9 in the direction parallel to the long side of these figures, it starts from one vertical wall and ends to the other vertical wall. And the thickness of the layer 9 is indicated by the smaller double arrow that starts from its bottom -- where it touches its previous layer and extends to the upper surface of it.

Q Now, regions or films or layers -- let's pick a term. Let's call these layers 7 and 8 in this figure.

Can you tell whether they were in electrical contact before the opening in 9 was established?

MR. GIBSON: Objection; form.

THE WITNESS: Electrical contact -- they be able to pass electricity through the opening?

BY MR. MANZO:

Q I'm sorry. Could you please repeat that?

A You asked me whether there is electrical contact before the opening in 9 was established, and I ask a clarification question, is: By electrical contact, meaning the ability to pass electrical

current?

Q Yes, from 8 to 7 or vice versa?

A Before the opening?

Q Before the opening in 9 occurred.

A Well, 9, according to the specification of Sukegawa, covers the entire surface of the substrate. And the entire surface of the substrate then is -- it is insulating so no current can flow in and out of the entire structure.

Q I see. Well, was layer 7 made before layer 8?

A That's correct.

Q And was layer 8 made before layer 9?

A That's correct.

Q And was layer 8 directly in contact with the top surface of layer 7 before layer 9 was put there?

A That's correct.

Q And is that direct contact between 7 and 8?

A The two layers touching each other.

Q You would call that direct contact, right?

A You can call it touching, direct contact.

Q You can also call it ohmic contact?

A What's that?

Q Ohmic.

A Ohmic, again, implies the passage of current. There is two kinds of contacts; there is ohmic contact and schottky contact. That depends what are the layers 7 and 8 and whether that contact will be ohmic or not, maybe a native oxide in one of the layers that would prevent the ohmic contact formation, and that may require some annealing steps at the end of the process to establish ohmic contact.

So it is a little bit not clear at this point whether the contact from an electrical perspective will be an ohmic contact or not, but the two metals touch each other.

Q Okay. So is it fair to say that there was direct contact between layers 7 and 8 before the opening was cut in the region or the film 9?

A The layers are put down sequentially, so, yes, so one is on top of the other.

MR. MANZO: Okay. Counsel, is this a good time to break for lunch?

MR. GIBSON: That's fine.

BY MR. MANZO:

Q Is that okay with you if we break for lunch, Professor?

A That's fine.

Q Thank you.

THE VIDEOGRAPHER: We are off the record. The time is 12:35 p.m.

(Recess.)

THE VIDEOGRAPHER: We are back on the record. The time is 1:44 p.m.

BY MR. MANZO:

Q Professor, good afternoon.

A Thank you. Good afternoon.

Q From the time we began the deposition this morning up until now, have you discussed your deposition with anybody?

A No.

Q Before the lunch recess we were talking about Figure 1B, which was marked as Exhibit 2009, Figure 1B of Sukegawa, that is. And when I asked you about electrical contact, I think you adverted to or made mention of potentially an oxide layer on top of 7 that would have to be annealed away or something like that.

Do you remember discussing that or mentioning that?

A I think that was in the context of you saying whether the contact is ohmic.

Q Okay. Well, my question really is -- let

me try it a different way.

From looking at Figure 1B, would a person of ordinary skill in the art conclude that film 8 and film 7 were in electrical contact with each other before nitride layer 9, or if layer 9 is made from something else, then whatever it is made of, is placed in the position we see it in Figure 1B?

MR. GIBSON: Objection; form.

THE WITNESS: In Figure 1B the layer 7 and 8 are in physical contact.

BY MR. MANZO:

Q Are they also --

A And before --

Q Sorry.

A And before nitride layer 9 were down, they were exposed so one could pass current through them, can pass current from 8 to 7, or if, from another region, current was coming to 2. If 2 was exposed through another opening somewhere, it was coming from 2, then that current can pass through 7 to 8. And now to whatever the electro circuit that may be formed at the time.

But after we are putting in layer 9, there is a passivation layer over the stack of layers 7 and 8, and no current could pass through before we

have an opening in 9.

Q When you say, "no current could pass through," do you mean no current could pass from something above where 9 is until the opening in 9 was created? Is that what you mean?

A Right. 9 -- from one side of the substrate you have the glass substrate, that's element 1, so knowing can come from that side. And the glass is fairly thick.

If you have 9, then you are completely isolate -- you put an insulating layer on top of the entire structure, the entire surface.

So everything which is enclosed between 1 and 9 are completely isolated from the outside world and no current can pass through into the structures unless you have an opening in 9.

Q But you still agree that layers 7 and 8 are in electrical contact with each other?

MR. GIBSON: Objection; form.

THE WITNESS: The ability to pass current from one to another is there, but for the current to pass through, you need to have something connect, like a battery or some sort of inlet or source.

And if that 7 and 8 are completely enclosed by insulating layers, that current cannot come from

anywhere. And the -- so the layers may be in physical contact. And if means to provide the voltage and a vias are created, then they can pass the current. But when they are completely isolated, I do not see how that ability to create a current can be established.

BY MR. MANZO:

Q So what I understand you to be saying, Professor, is that current flows only when there is a circuit, and there is no way to make a circuit if both sides of this was covered, one side with the glass substrate, 1, and the other side with the nitride, 9?

Do I understand you correctly?

A Right. If 9 completely covers the surface, the top surface, and 1 is covering the backside of all the structures, there is no means to connect into a board or into a source that will provide the voltage in order to generate the current.

Q Understood.

Is it fair to say that, notwithstanding that, there is electrical contact, not necessarily current flow, but plain old electrical contact between 7 and 8, regardless of 9?

MR. GIBSON: Objection; form.

THE WITNESS: You have two metals that are actually in physical contact so they have the ability to conduct electricity from one to another. But if you don't have a voltage difference between them, you will not be able to conduct any current. And so an opening in 9 is required for an external connection to be made, such as that for the flexible printed circuit, which will then bring the current from an outside source to be passed through the circuit and the devices that you have on substrate 100. And while you are passing the current, it will be passed through 7 and 8.

BY MR. MANZO:

Q Correct me if I'm wrong. What you're saying is that the two layers, 7 and 8, are in direct contact and would permit electrical current flow between them if there were electricity applied to one or the other; is that right?

MR. GIBSON: Objection; form.

THE WITNESS: Well, to have a current flow, you need a voltage difference between two elements. So you need to have a voltage source somewhere and another connection somewhere else that will be at a different voltage.

So one would be like at 5 volts and the

other to zero volts, which we refer to as ground. In that case, then current -- you establish the voltage difference and then current flows.

BY MR. MANZO:

Q Okay.

A But if all the layers are buried under insulating layers and there are no openings for something to be providing an excitation from outside, provide a signal from outside, the layer 7 and 8, by themselves, will not generate any currents.

I think it is a matter of definition what will define one.

Q Okay. Would it be possible, Professor, to have -- since this is just a cross section, if I had current or a voltage potential applied to 7 somewhere in front of the page and a different voltage applied to 8 somewhere behind the page, there could be a circuit and current would flow from 7 to 8; is that true?

MR. GIBSON: Objection; form.

THE WITNESS: If you had openings in the insulating layer 9 or if you have openings through the glass substrate 100 and you apply a voltage difference, then current will flow.

BY MR. MANZO:

Q That's good.

A But you need to have those openings.

Q If there were a buildup of static charge somehow on 8, would it flow to 7?

MR. GIBSON: Objection; form.

THE WITNESS: The buildup of static charge -- the buildup of electric charges on 8 more likely will develop before it gets passivated from 9. The charges are created through, like, friction. Once 7 and 8 are completely covered, the charge will be generated most likely in 9 and not in 7 or 8.

But this is a hypothetical question that you're referring --

BY MR. MANZO:

Q Yes. Yes, it is.

So, Professor, is it your testimony that there is no electrical contact between 7 and 8 in this Exhibit 2009 unless current is flowing between the two of them? Is that your testimony?

A My testimony is that 7 and 8 are in physical contact, they have the ability to conduct electricity from one to another, but that electricity has to be generated or closed through the application of the voltage difference or some

other excitation source that will be coming from outside, and that one will require a physical opening.

(Deposition Exhibit 2010 was marked for identification by the court reporter and is attached hereto.)

BY MR. MANZO:

Q Professor, can you identify what's been handed to you as Exhibit 2010.

A It's a Figure 2C from the same patent that we are discussing, namely, Sukegawa.

Q What's the difference between Figure 1B and Figure 2C? Let me withdraw that question.

Apart from the addition of the structure 31, which is a flexible wiring substrate, having a film, 31A, and a copper foil, 31B, and the film 10 between member 31 and the lower portion of the figure and the sealant -- not the sealant, strike "the sealant" -- the silicone resin 13, are there any other differences between these two exhibits?

A Well, some of the elements are not labeled in 2C compared to Figure 1B, but as far as the additional components, what you listed is correct.

Q Okay. So would your testimony about electrical contact between films 7 and 8 be the same

with regard to Figure 2C as it was with regard to Figure 1B?

A Well, in figure -- when you asked me earlier about electrical contact, you are always referring to before the opening of -- in the passivation layer 9, at least that's how I understood you.

In Figure 2C you have an opening in layer 9, so the layers are -- can be connected to the outside world. And, as shown in Figure 2C, there is a connection to the flexible printed circuit, 31, that provides such connection to the outside. Maybe it could be a power supply, maybe a board that provides signals that will going to the circuitry within the display, which is fabricated on the glass, element 1.

Q Okay.

A So in Figure 2C we have the ability to provide and have current flowing because the connection is established to the outside world.

Q Just to complete that thought, I think what you're saying is that the flexible printed circuit 31 structure can apply a voltage via the conductive film 10 to the upper surface of layer 8 and develop a voltage on that, and that voltage would be an

electrical -- would flow to wiring 7; is that right?

A What does it say there? You need two connections, you need to have a voltage difference. If 31 makes a connection and it comes up and provides the voltage, if you don't have another connection somewhere else to establish that voltage difference, current and/or flow, you need always to have a voltage difference for the current to flow.

But if 2 leads, for example, into a capacitor and that capacitor is -- the other terminal of the capacitor is connected to the ground, then you may have a transient current flowing until you completely charge the capacitors. The capacitors or capacitor.

But if you talk about only like ohmic contacts between two different points and the continuous passage of current between those two reference points, you need to have two connections.

But, in general, in operation of the display, multiple connections are provided, such as shown in Figure 2C. And during operations currents flow from -- through these external connections.

Q Thank you. So in a nutshell are you saying that layers 7 and 8 are in electrical contact in Figure 2C, but they are not in electrical and

contact in Figure 1B?

A I did not say layers 7 and 8 are not in electrical contact. I said they are in physical contact and they have the ability to conduct electricity. But to have -- conduct electricity, you need to provide an external source.

Q When you say "an external source," you mean in Figure 1B?

A It's like what you say in Figure 2C, you have a flexible printed circuit board that is making contact to layer 8, and you're referring earlier in Figure 1B in your questioning, you're referring to Figure 1B with the passivation layer covering completely layers 7 and 8 and you're asking me whether 7 or 8 are in electrical contact before opening, before moving 9 from above. And I responded that before removing 9, you do not need to provide connections to 7 and 8 in order to conduct electricity. The ability to conduct electricity is established after opening and removing layer 9 above 7 and 8, after creating the opening.

Q Okay. So let me see if I can summarize it this way.

In Figure 1B --

A Before the opening or after the opening?

Because you referred to both of those things earlier.

Q Understood. Listen to the question.

With regard to the structure in Figure 1B, I think what you're saying is that the layers 7 and 8 are in direct contact and have the ability to conduct electricity from one to the other, and I understand from your testimony that providing the opening in the passivation layer 9 gives you the ability to connect a circuit or a source of electricity to let that current flow to occur; is that right?

A Correct.

Q Okay. Is it true that in your declaration, which is Exhibit 1005 -- and specifically with regard to Sukegawa, you do not refer to Figure 3A, B, C, D or E?

I should make that more precise by saying you do not refer to any of those figures, 3A, B, C, D or E; is that correct? Well, strike that.

A Yes, the answer is not correct.

Q I see it at page 35.

Do you see it anywhere else?

A Multiple occasions, 35, 37.

Q All right. For what purposes do you cite

in Figure 3?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q In your declaration.

MR. GIBSON: Objection; form.

THE WITNESS: Well, in my analysis I was giving the '413, and '413 has several claims, and each claims has a series of statements which is referred to as limitations of the claims. So I have studied the prior art, and I was looking where those limitations are either met or provide enough information through the figure, through the text or through combinations of other pieces of prior art to make those limitations obvious.

BY MR. MANZO:

Q Okay. So starting at page 35 with regard to section X, Roman numeral X, which started on page 32 of your declaration, the first time that I see Figure 3 is Figure 3D on page 35.

Do you see that?

A That's correct.

Q Okay. So is it fair to say that you cite Figure 3D to show that there is a color filter that is just outside the connection of the flexible wiring circuit and sealed with an active matrix

substrate? Is that why you cited it?

I'm at the language right above Figure 3D -- I'm not trying to change anything -- starting on line 5 of that page.

A Well, if -- you're referring to paragraph 99?

Q Yes, paragraph 99, the fourth line of that paragraph.

A But if you look at paragraph 98, which is -- provides the, more or less, kind of the rationale of why I'm referring to this one is because the paragraph 98, it reads, "Paragraph 8 of Claims 1, 7 and 10, and Paragraph 9 of Claims 17, 22 and 24 requires 'a sealant over the first wiring in the second region of the second wiring.'"

So this is what is required in the claims of '413. So in 99 I describe evidence that that -- those elements are present in Sukegawa.

Q Okay. Now, do you agree that Figure 3D does not show the sealant?

MR. GIBSON: Objection; form.

THE WITNESS: To someone skilled in the art, when the text refers to the -- let me cite exactly from Sukegawa.

BY MR. MANZO:

Q Let me help you.

Are you saying that it is implicit from Figure 3D, but it's not really shown there in a drawing; is that right?

A Well, the sealant is in between 200 and 100 at the -- close to the vertical edge of 200 that is shown. And there is an arrow pointing to where the sealant would be.

So the fact that an element is not shown explicitly in this schematic is not the proof that that element is not there.

For example, in Figure 3D we do not see anything before the element 10. So we don't see the line 2, we don't see the wiring of 8, 7, we do not see all that -- all that level of detail.

So it doesn't mean that this flexible printed circuit board element 300 is just connected to the glass substrate that doesn't do anything, it is implied that all the other elements are there.

So when the specifications in Sukegawa refer to the color filter substrate and say it is sealed with the active metric substrate, that, inherently, is implied that there is a sealant between them, otherwise the liquid crystal would not be contained within.

And before attaching element 300, the gap between elements 200 and 100 is filled with the liquid crystal. So if it goes to fill that, the liquid crystal will not be contained in the display and the display will not function. The element 300 comes after the information of the sealant and after the filling with the liquid crystal.

Q I understand. Just to make it clear, you agree that the sealant between 100 and 200 is not explicitly shown in Figure 3D, correct?

A Explicitly shown like a drawing of an element and a numeral referring to that element saying that that's the sealant or that the sealant is not at all present or implied in Figure 3D?

Q I'm not asking about implied. I'm just asking about whether it is literally shown in Figure 3D.

A What Figure 3D literally shows is the two substrates, 100 and 200, and some of the other elements which are not related to the sealant, but it shows the 100 and 200 and the specifications, the text within Sukegawa, referred to that -- the two substrates and referred to them as being sealed.

Q Okay. But the sealant is not pictured here; is that right?

A As I said, the level of detail of this figure is such that it shows that the two substrates, the sealant is in between them and close to the vertical edge of 200 and referred to it in the text.

I don't know -- I don't understand what your line of question is trying to say. Are you trying to say the sealant is not present? I disagree.

Q No, I'm not asking you that, Professor. I'm just asking if it is shown pictorially. That's a plain vanilla question.

A This shows the two substrates, 100 and 200, and the text is referred to that assembly as being sealed.

Q Let me try it another way. Does it show 200 and 100 with no space between those two?

MR. GIBSON: Objection; form.

THE WITNESS: I don't understand what you're trying to do. It doesn't show also some of the other elements, so it doesn't show the wiring 2, it doesn't show the layer 3, the wiring 7 and 8.

Are you going to try to also tell me that those elements are not there, so people attaching these flexible printed circuit for nothing?

So the fact that something is not showing -- is not shown or is not referred to by a numeral in the artwork is not an indication that something is not there, but that the purpose of the artwork is to point out the presence of some of the elements that are described in the -- in the specific -- in the specifications and the relative relationship of those elements, and other elements may not be shown in the artwork, but, clearly, in light of the entire specifications and descriptions, those elements are there, are implied.

BY MR. MANZO:

Q Professor, what kind of apparatus is used for forming a conductive layer in a liquid crystal display device?

A There are different apparatuses that are used to provide -- that are used to form a conductive layer in a liquid crystal display.

Q Could you tell us the different kinds?

A One is called an evaporator, another is called a sputterer, another one called CVD, chemical vapor deposition, laser-assisted depositions, just to name a few.

Q So you named four. An evaporator, a sputterer, a CVD apparatus and a laser-assisted

deposition apparatus?

A I named a few, depending on the layer and depending upon the extent to which that layer -- whether that layer will be a thin layer or thick layer, there are other techniques, like screen printing, for example, which is typically used in solar cells. But in some of the new displays for printable electronics, new methods may be used beyond what I mentioned. I think I gave you some representative examples.

Q Okay. Thank you.

Now, what kind of apparatus is used for patterning a conductive layer in an LCD device being constructed? How is that done?

A In general -- in the general field of microelectronics, we refer to two general processes, the additive processes and the subtractive processes.

In the additive -- sorry.

In the subtractive processes, which is the majority of the steps I perform, you deposed a layer everywhere and then you go through a process known as photolithography, and then you define the regions that you want to leave.

And through a sequence called etching

style, you remove the layers that are not protected by the layer called photoresist, which is patterned through the photolithographic process.

That's the common thing for making the features that we see in most of these figures.

There is also the additive process in which you selectively place material down only the regions that you need and you do not have to go through the other steps that I mentioned, namely, the photolithography and etching steps, because the material is put down only where you need it and nowhere else.

An example of an additive process is if you deposit a material in one of the apparatus that I mentioned earlier, but you have a screen, you have a layer like a metal sheet that has openings, and the openings define the regions where the thin film that you will deposit will go onto the substrate and the screen or that metal sheet chemical will then block that layer from -- and prevent that material to be deposited and flow anywhere else on the surface. And that could be an example of an additive process.

Q Are you saying metal slit or metal sieve? I just didn't understand you.

A Screen.

Q Metal screen?

A Right. So it's a piece of metal, very thin piece of metal, that has openings. And the material goes through the openings. And the metal -- typically, it is made by metal -- is covering all the other regions of the substrate.

So then the material that you're trying to put on to the substrate only goes to where there is an opening in that screen.

Q It is like a stencil, right?

A Yeah.

Q Okay.

A Although, I do not use stencils -- like a stencil like silicone printing? -- sorry -- like in screen printing?

Q Yes.

A Yes, a similar thing.

Q But on a microscopic scale?

A Yeah.

Q Okay. So -- but I was asking about --

A Excuse me.

Q Yes.

A Historically, before the advent of photolithography and the ability to do find features, the bursting through an opening -- using

those screens was a standard way of putting down, particularly in the laboratory -- there are companies that have created products and even today there are companies that sell such products for making circuits and displays, but that ability -- that technology has limits on the size or the features that you can define.

So you have large features that you want to put metal, that is fine. But you cannot do micron-sized features, or let alone submicron, with that technology, because you can not etch a hole in the metal so thin, because the metal will also have a certain thickness that will prevent.

So that technology is valid for large features, such as those used in making external connector, like the pad, those connections to the outside world is -- but in making the transistors, they have certain limitations.

Q Okay. So I had asked you what are the etching apparatuses, and you then talked about additive processes and subtractive processes. Let's get back to what are the etching apparatus that are used in the liquid crystal display field.

A I can classify them in three categories -- actually, two categories, and one is like something

you would apply everywhere onto the substrate and some that will be applied selectively to the substrate.

Selectively through the substrate would be, for example, using a laser ablation removing the material locally. If you add something and create features that will exist throughout the substrate, the laser process will be very slow. So in that case you use a process that will be applied to the entire substrate at the same time.

And those processes then classify into two categories also, one is called -- referred to as wet processes and the other one is referred to as dry processes.

The wet process requires chemicals, liquid chemicals, and you immerse the substrate into that solution.

And the dry processes, you have a vacuum chamber and then you strike a plasma and then you create reactive elements.

Now, between those two, there can be other techniques, such as focused ion beam etching that can be applied selectively -- I didn't know this would be a test in microelectronic technology processing, I would have studied a little bit more

to give you all the techniques, but, in general, there is no shortage of technologies to do whatever one wants to do.

Q Okay. And is it generally true that wet etches are isotropic and dry etches are anisotropic?

A Well, the dry etchings can be anisotropic. When you operate a plasma system in what's known as the reactive ion etching mode where you use the bombardment of the ions as a means to provide directionality, and for that one you have to have a lactate film, and that is created by biasing the substrate. But the plasma process or a dry etching process can also be isotropic, and that is referred to plasma etching to distinguish from the reactive ionating which has directionality control.

Q Okay. Well, how are substrates that are used in LCDs put into the deposition apparatus and the etching apparatuses that you've just testified about?

MR. GIBSON: Objection; form.

THE WITNESS: How are they put into the position of etching rub is depending upon the step of the fabrication and the equipment or the process used.

As I mentioned, there are a variety of

processes and a variety of technologies and the way to lower the substrate into each one of them, depending upon --

MR. MANZO: Okay. Well, I think we're at a point where we need to change the video disk, so let's have a short hiatus.

THE VIDEOGRAPHER: We are off the record. The time is 2:33 p.m. on July 1st, 2013. This is the end of video number 2 of the continuing deposition of Dr. Milt Hatalis.

(Recess.)

THE VIDEOGRAPHER: We are on the record. The time is 2:48 p.m. on July 1st, 2013. This is the beginning of video number 3 of the deposition of Dr. Milt Hatalis.

THE WITNESS: If I may correct the transcripts so then maybe the same mistake will not appear. In line -- page 110, line 21, it states "lower the sin strate," I think it means the substrate.

If I may finish the sentence, it depends on the type of equipment, what is the type of process that will be used, so there is no one weak way to do that.

BY MR. MANZO:

Q Okay. In typical mass production for LCD devices, after the counter-substrate is bonded to the TFT substrate, are those same substrates put again into a deposition apparatus or the etching apparatus that you've talked about?

MR. GIBSON: Objection; form.

THE WITNESS: After the completion of MLCD device and if the system performs, there is no need to go back into one of those depositions or etching apparatus.

BY MR. MANZO:

Q What happens if they are not -- if the system is not performing properly? Can the LCD be put back into the patterning or the deposition apparatus or the etching apparatus?

MR. GIBSON: Objection; form.

THE WITNESS: If it's intrinsic defect in the TFT array, then nothing can be done at that point.

If it is a defect that is related to the creation of the external connections, if those external connections have defects, then steps can be taken to correct that defect.

BY MR. MANZO:

Q How?

A It depends on what is the defect.

Q Let's say the defect is in the external connections.

A Let's say like, for example, two of those is external leads, like these wirings, let's say wiring 2 that go to the adjacent pads, let's say that they are shorted together, then there is a repair stamp that you can go with the laser and cut the metal wiring and remove that defect.

So it depends upon what the defect is, then you choose the means to correct it, if it can be corrected.

Q Looking at Figure 2C of Sukegawa, in your paragraphs 122 and 123 of your declaration marked as Exhibit 1005, is the second wiring the upper level wiring 7?

A That's correct.

Q And is the transparent conductive layer 8?

A Correct.

Q Does the layer 8 cover the end of wiring 7, as shown in Figure 2C?

A Where we are seeing cross section, we don't know how 8 cover 7 in the entire planner section view in Figure 2C, but looking at the cross section, 8 extends beyond the edge of 7 on either end.

Q On both ends, right?
A Correct.
Q To be more precise than saying it goes beyond, it actually covers the ends that are shown in the cross section of the figure; is that right?
A What do you mean by "ends"? The vertical walls?
Q Yes, the vertical walls.
A Yes, it does.
Q So the top of -- so 8 resides on top of layer 7. And then when layer 7 ends, 8 descends vertically and then continues horizontally, according to the representation of Figure 2C; is that correct?
MR. GIBSON: Objection; form.
THE WITNESS: Well, as depicted in Figure 2C, 8 is conformily coating 7, conformily covering 7.
BY MR. MANZO:
Q Okay. So the ends of 7 that are shown in Figure 2C are not exposed; is that right?
A In reality, that will depends upon how thick is 7, how 7 has been patterned and -- and whether the coverage of 8 on top of 7 is conformal as the Figure 2 is shown or it is discontinuous.

In Figure 2C the artis shows a conformal coating. And, in reality, 7 will be -- could be thicker, a lot thicker, than 8. And if the walls are vertical walls as patterned with the reactive ionating process that we discussed earlier, there may be a discontinuity from the surface of 8 on layer 7 and the layer 8 which exists beyond 7. All depends upon the relative thickness of the layers, the means they put down, and the slope the shape of that edge of 7.

Q What does it mean -- in the context of the answer you just gave, what do you mean to conform?

A Conformal coating, which is the word I was referring to, conformal coating is a coating that covers the underlying material in all aspects, in all directions, whether its horizontal or vertical.

So, in other words, it will cover the surface and will cover the sidewalls, and then the overall thickness will be independent, whether it is on the upper surface or whether it is on the edges of the region that is being coated.

You asked me, if I understand, if something shown in Figure 2C will always be like that, and I tried to elaborate that something is shown in Figure 2C but it is an artwork and the exact shape

and continuity of the layers will depend on the thicknesses and how you pattern it and what shape you create to those edges.

Q Okay. Well, do you know if there is a reason in Sukegawa why layer 8 goes beyond and conforms to the layer 7?

A Layer 8 is used to protect layer 7.

Q Protect it from what?

A Protecting from corrosion, from moisture, from --

Q Okay. So do you agree that Sukegawa does not show wiring 7 extending beyond the layer 8?

A In this particular embodiment.

Q I'm sorry. In this particular embodiment that's correct?

A Yes.

Q Okay. Is it incorrect for a different embodiment in Sukegawa?

A Well, there are three layers here, there is 7, there is 8 and 9. And upon the order with which you put those layers down and how -- what means you provide for interconnecting them, one can be bigger or smaller than the other one.

But in answer -- something else here, we're referring to the Figure 2C. In the Figure 2C is the

connection for the scan lines. And scan lines are referred to are the gate lines.

Q Okay.

A So the layer 2, the wiring 2 labeled in Figure 2C --

Q Yes.

A -- will be the one that will extend from this pad region all the way out to the almost other end to the display.

In any display you have two sets of lines. You have the gate lines and you have the data lines. The gate lines also referred to as scan lines. And the data lines also referred to as signal lines.

If we look at Figure 3C from Sukegawa, it depicts the signal lines 7A and referred to them as the data signal wiring.

So the data signal wiring, and you have hundred such wiring, is at the level different than the scan lines, and they are -- one runs almost perpendicular to each other but at a different level, but they are not crossing because they are at a different level.

So the Figure 2C is a terminal connection for the scan lines and, as such, the element 2 is the one that will propagate to the display portion.

But if you -- to draw an artwork for the for terminal connection for the data signal pads where the data signals will receive the connections from the flexible printed circuit board, it will not be true that will propagate all the way across the display, because then it will cross the existing gate lines and will cause defects.

Instead, it will be 7 that it will propagate across the display. And, in that case, 7 will be above the scan lines and it can form the required data signal wiring without causing a defect.

So in that embodiment the wiring -- the transparent conductive layer 8 will not continue across, because it is not shown in the Figure 3C as being on top of the data signal wiring 7A. So at some point that layer 8 will terminate, but the material of layer 7 will continue to form the data signal wiring.

Q Won't there be a discontinuity between the portion of layer 7 shown in Figure 2C, even shown in Figure 3B and the display portion?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Let me rephrase the question.

In Figure 3C we can see portions of layer 7 marked as 7A, which is the data signal wiring, I think you testified, we can see a 7B, which I think is a drain electrode, but he can tell me if I'm wrong, and we can see 7C to the left of 7B, which I believe is a source electrode; is that right?

A Correct.

Q Okay. So are these connected continuously to the layer 7-1 that we see in Figure 3B in the terminal portion?

MR. GIBSON: Objection; form.

THE WITNESS: I think all embodiments in Sukegawa are referring to the terminal connections to the scan lines or gate lines. That's why it shows the wiring 2, which is the first wiring, the one that will continue to display portion. And it can do that and forms the gate wiring.

So for each terminal contact, you have one continuous scan line going across the display. But that's on one side of the display.

On the other side of the display you need to do the same thing, but in order to formulate the connections to the data signal wiring, which are the wiring 7A in Figure 3C.

So that wiring, 7A, continues all the way

up to the edge of the display.

BY MR. MANZO:

Q What happens when it gets to the sealant?

A It goes under the sealant.

Q 7 goes under the sealant?

A Of course. It's the wiring that formulates the 7A, the data signal wiring 7A.

Q Is there anything in Sukegawa that says that 7 goes under the sealant?

A Well, there is a 7 listed in Figure 2C that is part of the terminal connections for the scan line. And I said that these are the connections that you will have in one side of the display. And in the other side the display, perpendicular to that side, you have another set of terminal connections that will be providing connections to the data signal wiring, and that will be the line 7A, and you will have hundreds of those data signal wirings.

And the material for those wiring lines will continue under the sealant and into the terminal connections in order to provide -- in order to receive the signal for the flexible printed circuit board.

Q In that case, is it correct that the wiring 7 is not protected by layer 8 and is subject to

corrosion?

A Well, the wiring 7 will be covered by the protective layer 9 and it will be under the sealant and will be inside the array, so there will be no means for -- to be corrected, it will be protected.

So the 8 will extend and cover 7 up to distance. Beyond the distance, 7 will be protected by other means, by 9, by the sealant or by the counter glass.

Q Just to try to visualize this a little better --

A If you look at APA, and there is two sets of wirings.

Q Looking where?

A Okay. Look at Figure 5 of Exhibit 1001 on page 5, there are two sets of wirings that extend all the way up to the edge. This is the bottom edge and this is the right-hand side edge.

The vertical ones review the data signal lines and the horizontal ones, the ones on the right, that terminate on the right edge, are the scan lines. And those lines run across the display, and the other lines run also across. So you have a grid where the two lines are crossing each other at multiple occasions. But because they are at

different levels, they did not create a short.

Now, in Sukegawa, the display that is described is a bottom gate of silicon display. So at each data signal wiring and it each gate signal wiring, scan line, there will be external connections for the gate lines or scan lines, they will be such as those depicted in Figure 2C.

But for the signal lines, the data signal wiring, which is going the opposite direction, the layer 2 cannot extend because -- across the display, because then it will cross all the horizontal lines and the display will not function.

And in that case it will be the upper layer 7 that will continue and will create that wirings indicated in Figure 3C as 7A.

Q Professor, let's visualize this whole conference table that we're sitting at as substrate. And the court reporter is at one end, along one side and you and I are on opposite longitudinal sides and your counsel is further to the left -- to your right and my left. Okay? So this whole substrate has a lot of different portions.

Now, if we come along with a layer 7, we could put a little square foot of it over by the court reporter, we could put a square foot over by

you and have a bunch of space between that and maybe run some lines down the other end of the table that are all disconnected from one another; is that right?

MR. GIBSON: Objection; form.

THE WITNESS: Well, the portions of the layer that we will put on the material -- on the substrate, it will have to form -- it has to serve a specific function. So one function is to create this double-layer conductive structures at the terminal regions. But 7 also serves another function, to form the data signal wiring 7A, as indicated in Figure 3C.

So you refer to the reporter and to me. Now, one of us is going to be a data signal wiring and the other one is going to be a gate signal wiring or scan line wiring. Can you choose one of us to be -- what do you want me to be?

BY MR. MANZO:

Q Well, I would like to figure out that somewhere there is an external connection line down at one end or the other end.

A We both extend our connection, because we are both outside the display. You said the table is the display.

Q That's right.

So let's say the court reporter is at the right-hand side, so that is the -- did you say that's the gate scan lines?

A Yes, that's the gate lines, scan lines.

Q Okay.

A So starting from the reporter going all the way out to the screen, the other end of the table, on your left or my right it will be continuous line that it will start from the reporter and will terminate at the other end to the display, at the other end of the table, and that wiring line will be made from the wiring element 2, which is the lower wiring.

Q Okay.

A From my end you assigned me to be the data signal wiring terminal, there will be another wiring that will start from me and will terminate to you, who are sitting of across from me. In other words --

Q I understand.

A -- there will be a 7 going perpendicular to the 2, and those wirings should not cross -- I mean, can cross, but have to be at a different level. Those wirings should not form -- should not touch

because then they will form an electrical connection and then the current will flow who knows where.

Q You mean if they directly contact, they'll be in electrical contact?

A Well, you see we're both at the external terminals so we both receive signals.

Q Okay.

A So now we are touching and the signals will be routed to who knows where.

Q Correct.

A So the current will not flow where it is supposed to flow.

So there are two set of wirings in any display, as the Figure 5 illustrates, and they run across at two different levels.

Q They are orthogonal?

A Exactly.

Q Okay. Now, let's talk about the sealant because we haven't talked about that very well -- I mean enough, we haven't talked about that enough.

If the substrate is this table, where is the sealant going to be, typically?

A Well, is the substrate the element 100 --

Q Yes.

A -- or the 200?

Q Yes, 100.

A And I am the terminal connections for the data wiring.

Q Same arrangement as before. That's the gate lines down there and --

A Okay. The sealant will be placed -- based on information disclosed, someone skilled in the art will understand to place the sealant where the element 13 stops, so in this case it will be right where -- the two metals still overlap, the two wirings, 8 and 2 -- or 7 and 2 overlap, that's where you place the sealant.

Q Does Sukegawa say that anywhere, that the sealant overlies both 7 and 2?

A Sukegawa doesn't say it explicitly. It shows that to that figure that we referred earlier, 3D. And if you take the relative dimensions of the element 10 and if you take the relative dimensions of the gap form between where 10 ends to the left and 200 starts further in, then you will see that that vertical edge of 200 where it will overlap with the sealant will be placed at the -- where that numeral 8 is listed adjacent to element 13. But --

Q Numeral 8 in what figure?

A 2C. I thought we were referring to

Figure 2C.

And the relations between the sealant and the silicon layer 13 is explicitly shown in the other piece of prior art that I'm referring in my declaration.

Q Is that Nakamoto?

A Nakamoto, correct.

Q Let's talk about Nakamoto in a minute.

Could you look at Figure 3A of Sukegawa, please.

What does that represent, just by way of a general statement of what it is?

A It is the artwork for the layout for the mask set that is used to pattern the different elements that are used to formulate that particular embodiment.

Q Okay. So this is a representation of the mask set for what ends up being shown on Figure 3E; is that right?

A Yes, 3E -- and shown in 3B, they are the same.

Q Okay. Now, does that Figure 3A show us that the region -- sorry -- show us the regions 7-1 and 7-2? Are they delineated in Figure 3A?

MR. GIBSON: Objection; form.

THE WITNESS: What do you mean by "delineated"? Are they shown?

BY MR. MANZO:

Q Yes, are they shown? Perhaps my question was unclear.

What is -- in Figure 3A, what is the region 7-1? You say it is a rectangle on the left side. What does that mean?

A Well, it is the portions of the layer 7 that remain in that location.

Q Okay. So does that mean that 7-1 is inside that rectangle that has the 7-1 attached to it?

A Well, the external -- are you talking about the rectangle labeled 7-1?

Q I am.

A All right. That rectangle defines the area where the layer 7 will be within.

Q Okay. I mean, that corresponds to Figure 3B which is the sectional view, yes?

A Sectional view, correct.

Q Okay. And in the same way, does 7-2 in Figure 3A delineate the region where layer 7-2 is going to be within?

A In that particular embodiment, correct.

Q Okay. So according to Figure 3A, this part

of layer 7 does not extend further to the left; is that correct?

A No, layer 2-2 is the one that extends.

Q Layer 2 is the one that extends, but not 7, right?

A That's what I said, that this is the terminal connection for the scan line wiring and not the terminal connections for the data signal wiring.

Q Now, do you see the outermost rectangle in Figure 3A, do you see that that's labeled with the number 8?

A Correct.

Q Does that mean that the conductive oxide layer overlies both region 7-1 and 7-2 to the extent shown in Figure 3A?

A In this particular embodiment, yes. But -- yeah.

Q Now, you mentioned -- strike that.

A If I may add, Figure 3A is not the one, or 3B is not the embodiment that I have used in my declaration, just to make the record clear.

Q I didn't understand.

A You are referring to the Figures 3A, B and Figure 3E in our discussions a few moments ago?

Q Yes.

A And I said that's one embodiment that I did not use in my declaration --

Q Okay.

A -- just clarifying the record.

Q You did not use Figure 3A and Figure 3B?

A That's a different embodiment than I have utilized -- that I utilized.

Q So which embodiment did you use?

A I used the embodiment in Figure 2C.

Q Very well.

Is it correct that in Sukegawa the first wiring, 2, and the second wiring, 7, contact each other outside the sealant in order to make a secure corrosion-resistant local connection to the flexible wiring substrate, 31?

MR. GIBSON: Objection; form.

THE WITNESS: You defended your question as contact outside the sealant, and I believe in my testimony a few minutes ago I placed the -- I placed the sealant in a location that overlaps the two -- both wirings.

You're right, that the contacts where the two regions are touching each other through those holes labeled 6 is depicted in E, Figure --

BY MR. MANZO:

Q 1A and 2B?

A Those contact holes in that particular embodiment are outside the sealant, because they are located in the region that either overlaps the flexible printed circuit board or that testing region, which is below the silicon layer 13.

But the sealant does provide some corrosion protection because I think in your statement you refer to -- also to corrosion protection. And the sealant also protects the -- whatever is overlapping --

Q Referring to Figure 2C, could be tell me where the sealant is relative to reference numeral 13 and reference numeral 8, please?

A The Figure 2C in view of the prior art Nakamoto, someone skilled in the art and in view of the figure, Figure 3D, the sealant will be next to 13 and the two will touch each other.

Q Can you point, just point where the sealant is going to be, please.

A Well, the sealant is a very wide region, so the start of it will be here, and then it will extend from -- we're on opposite sides, so it will extend to my right, to this direction, over hundreds of microns.

Q Okay. So on Exhibit 2 -- what is this number? 2010? Could you please mark on Exhibit 2010 with this red pen where you believe the sealant would go based on your testimony?

A I'm marking Exhibit 2010, the location of the sealant based on the information disclosed in Sukegawa and in view of the prior art Nakamoto?

Q Yes, that's my question.

And you marked in red -- I think you put the letters SL for sealant; is that it?

A Yes.

Q Okay.

A And, of course, this indicate the sealant will continue.

Q Yes, I -- that's what your arrow indicates, correct?

A Correct.

And you can see that the relationship clearly in the prior art labeled "Nakamoto" referred in my declaration.

Q We're going to turn to that pretty shortly.

A I also want to clarify in this -- in this point that once we are next to 13, wherever area remains, if it is not covered by the sealant, it is an area that will be totally wasted on the display.

It is an area that will be adding to the overall dimensions of the display without having any functional purpose. It will add to the entire length of lines, which will increase the resistance. So from both the physical dimension size, it will be undesirable from the electro-performance point of view, it will also be undesirable, so the motivation to reduce the size of the display in order to either maximize the viewing portion or to be able to fabricate more displays per mother glass.

Typically a display is fabricated onto a larger piece of glass that contains a plurality of displays. And then that larger piece of glass has been separated to the individual displays.

And if there is an extra dead region on the periphery of the display that serves no purpose, it will increase the cost, it will degrade the performance and it will not be desirable from the consumer point of view because it will increase the border around the display.

Q Professor, is it your testimony that the person of ordinary skill in the relevant art would have understood these things in 1997?

A The issues of cost and performance was pervasive and was well known in the field since the

beginning of the industry, because there was a lot of competition between companies, so ability to put more glasses or ability to design -- put more displays per mother glass or the ability to fabricate larger displays was from the onset of the industry. People raced to fabricate bigger, cheaper displays. So minimizing the area around the periphery of the display was something that was well known.

Q How do you spell that -- how do you spell that?

A Mother.

Q Mother, like mother/father?

A Yes.

Q Okay. The mother glass?

A Yes, two words, that's what it is. People refer the bigger substrate, the bigger glass substrate on top of which you fabricate the many individual displays. But they become individual displays once you scribe and separate them from the mother glass.

Q I'm handing you a copy of Exhibit 1004.

A Before we go into lengthy discussion, may I have a two-minute break?

Q Yes.

THE VIDEOGRAPHER: We are off the record. The time is 3:41 p.m.

(Recess.)

THE VIDEOGRAPHER: We are back on the record, the time is 3:50 p.m.

BY MR. MANZO:

Q Professor Hatalis, you mentioned several times your view of Sukegawa in view of Nakamoto, right?

A For the placement of the sealant.

Q Okay. Can you show us in any of the figures of Nakamoto where that sealant goes?

A You can see, for example, in Figure 9, which it shows a cross section and it indicates the terminal region and it shows the silicon layer, which is similar to the element 13 in Sukegawa.

And you see that the silicon layer is physically touching the sealant between the two opposing glass substrates, substrate 1 and substrate 2, as indicated in Figure 9 of Nakamoto was sub 1 and sub 2.

Q The silicone resin, is that marked SIL?

A The silicon, yes.

Q And it looks -- is the sealant marked SL?

A In the specification referring to both SL

and EPX, which is epoxy resin, they are both used for sealant.

Q Does Figure 5 show a sealant SL from a plan view?

A It does.

Q And do we see a -- actually just a corner of the sealant; in other words, we have a portion of the sealant that goes from about the middle of the drawing towards the right and a portion that goes from that same middle of the drawing straight down; is that right?

A Yes. That's the part of the sealant labeled SL in Figure 9 --

Q Okay.

A -- in the cross section of Figure 9.

Q Now, I think that you testified that -- well, let's put it another way.

In section 100 of your declaration -- why don't we turn to that paragraph 100, where you show Figure 9 and Figure 5 together.

In that paragraph 100 -- and, by the way, Counsel, we are still waiting to receive a color copy of this colored exhibit. We've not received one yet.

If you have one around, we'd love to --

MR. GIBSON: I wasn't aware that you had requested it, but I will check at the next break.

MR. MANZO: I appreciate it very much. We did make that request. Mr. Murphy requested it of Scott McKeown.

MR. GIBSON: Okay. I wasn't aware of it until just now, but I will be happy to take a look and see if I can find it.

MR. MANZO: That will be superb.

Q Sorry for that limna.

In Figure 5, as shown on page 6 of your Exhibit 1005, there's two ovals with arrows pointing to them, which I suppose were colored.

Do you see those two?

A Yes.

Q What do those represent, please?

A Well, Nakamoto is describing an accumetrics liquid crystal display and described means to make electrical connections to a flexible printed circuit board -- to a flexible circuit board, which is placed at the terminal regions.

So as you see in Figure 5, there are wirings that start from the edge of the array, which is the element labeled "AR," and that wiring goes into the horizontal directions and terminate in the

terminal labeled as GTM.

And there's wiring that start from the vertical/horizontal end of the array and terminate in the upper end of the corner of the figure and form the data terminals, referred to as DTM.

That wiring, one of them is for the gate lines. The GPM refer to the gate lines and the DTMs refer to the data lines. That wiring cross under the sealant. And those circles and Rs indicate the location where that wiring is crossing under the sealant.

Q Now, you say in paragraph 101 the following, quote -- and I'm starting with the second sentence of paragraph 101 -- as Sukegawa explains that its LCD panel includes a sealing material, and Nakamoto shows that the placement of the sealant near close to the connection to the tape carrier package was known, and also that the placement of the sealant over the first and second wirings that extend outside the sealant was known, it would have taken only ordinary skill to include a configuration having the sealant over the first and second wirings, closed quote.

Did I read it correctly?

A Yes, you read from what's in paragraph 101.

Q Okay. Is there any disclosure here about the claimed first region or second region that are in the claims of the '413 patent being challenged?

MR. GIBSON: Objection; form.

THE WITNESS: I don't understand your question. What do you mean?

BY MR. MANZO:

Q Well, okay. If you look at the first para- -- the first sentence of section X1 or paragraph 101, it talks about a sealant over the first wiring and a second region of the second wiring.

A And that's a claimed feature of the '413.

Q Yes. That's what I'm asking about.

I don't understand how -- let me put it another way.

It seems to me that the ending of paragraph 101 is a non sequitur, and I'm asking you why that is wrong. I don't see anything in the ending of section 101 1 that tells me anything about the second region.

Did I miss it?

A In my declaration I have performed an analysis of Sukegawa and I have identified the first region and the second region of the second wiring,

and I have identified the first wiring also.

I did not perform -- at least I did not disclose -- I did not describe it in my declaration a similar analysis of Nakamoto to identify the exact first wiring and second wiring and the first and second regions of the second wiring.

I referred to the first and second regions, the second wiring, with respect to Sukegawa and the first wiring also with respect to Sukegawa. And I used Nakamoto in order to indicate the placement of the sealant over wiring that was used in Nakamoto, which is as many of the features and of the first and second wirings in '413.

Q Okay. Well, where are the first wirings and the second wirings in Nakamoto?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Okay. Are there first wirings and second wirings in Nakamoto Figure 5?

A You want me to perform an analysis and show you where the first wiring is in Nakamoto?

Q Yes, please.

A First let me say I didn't perform this analysis because I didn't thought it was required since I have identified those elements already in

Sukegawa.

If you want me to identify where is the first wiring and how that first wiring is meeting the claims of '413, I can do that.

Do you want me to do that?

Q Will that take long?

A No.

Q A minute or two?

A Yeah.

Q Go ahead, please.

A The first wiring in Nakamoto is the portion -- of the wiring made by the scan line material. And the scan line material is referred in the Figure 4 as G2.

Do you see element G2 in Figure 4?

Q Not yet.

A It is the gate, the bottom gate to the transistor.

Q Can you point?

A It says "GT," "G2" next to it.

Q Is that what it says? Okay. I see a GT.

A And next to the small letters is G2.

Q That's too small for me to read. I apologize. I see something that looks like a 9 and a 2?

A If we refer to --

MR. GIBSON: The letter G looks a lot like a 9.

THE WITNESS: There is a reference in -- I'll read for you. That's the -- I'm sorry.

BY MR. MANZO:

Q I don't need a reference. That's okay.

So that's the first wiring?

A Well, the first wiring is the wiring that forms onto the substrate, over the substrate is the very first wiring. And the first wiring form over the substrate is the wiring that is formulated by the material of the scan lines.

Q Okay. So is there a second wiring over that somewhere?

A Okay. For example, look at the prior art 70, it says, "The gate dielectric G2 are formed in the single layer of the second conductive electric film g2," with small g, "for example, the aluminum fill on the sputterer."

So the first wiring is made by aluminum going to, according to paragraph 70, which is the first metal layer that is put down over the substrate. And in between the substrate and the first metal layer you have the element SIO, which is

an insulating, coated, an oxide, silicon oxide coating.

Now, this wiring in the horizontal direction continues all the way out to the end, continuous line starts from the one end of the display and propagate all the way out to the other end of the display. These lines are form the scan lines, the horizontal scan lines. Okay?

Q You are pointing to figure what? Figure 5?

A Figure 5. The gate lines of the scan lines are the horizontal lines, because these are the gate terminals.

Q That are marked GTM?

A GTM are the gate terminals.

Q Okay.

A Now the material, the aluminum material, is used in Nakamoto to form these successive continuous horizontal lines that go across the display and there are hundreds of those lines.

Q Where?

A Those lines continue all the way across the display, like all across the table. All right? These are the scan lines. Okay?

Q I think so. I think I'm following you.

A That material that is used to make these

lines, the aluminum material that is used to make these lines, is also used to form wiring that are going in the data terminals.

So somewhere above the first gate line and the horizontal lines, which is labeled as "GI" -- you see a line labeled GI?

The GI has a vertical line and horizontal line.

Q Yes, that's the gate insulator, I think?

A That's the gate insulator.

That GI, inside of it the gate insulator remains, and outside of it the gate insulator is removed and create an opening in the gate insulator.

So somewhere between the boundary line called GI, the horizontal boundary line GI, and the first horizontal gate line will be the start of a vertical line that is made by aluminum, which is the same aluminum as that used to fabricate the horizontal scan lines. And that material goes all the way out to the terminal regions, DTM.

So these are individual lines, which that go all the way out to the end, the top end.

Q And are all of these the first wiring?

A I'm describing it.

Q Thank you.

A And that portion made with the aluminum, which is used in forming the wiring for the DTMs, okay, it can be seen in the cross section in the Figure 9, and that is the element labeled G1.

Do you see G1? There is a G1 and D1.

Q I see them?

A G1 is the layer right above the SIO layer, which is, as we said a moment ago, is the insulating oxide above the substrate sub 1.

Q So G1 is a first wiring?

A So G1 is a first wiring made of aluminum, and that one overlaps another wiring. And that other wiring -- do you see the other wiring by the double layer D2, D3.

D2, according to the specifications, is a chrome layer and D3 is an aluminum layer, if I'm not mistaken.

And those two layers are in electrical contact because the GI layer has been removed. So in this region here you have both the G1 layer below and you have the D2 and D3 layers above it. And in this region, GI, which is the gate insulating layer, does not exist.

Q That's in the display area, yes?

A No. This is right above the display area.

The display is what is known as AR.

Q Okay.

A AR is the display area --

Q I'm --

A -- and outside that area called as AR, you have the wiring leading to the terminal regions.

Q Okay. So perhaps I misspoke. What you're pointing to is inside the sealant region, not under the sealant region but in the interior to be marked by the sealant region, SL?

A The double wiring -- the double wiring starts from inside the sealant region and extends under the sealant region and you can see -- maybe not clearly, you have to zoom out and magnify the pictures, but the D2, D3 extend below the sealant. So the power combination of D2, D3 is overlapping G1 inside the sealant and also under the sealant.

Q Professor, as best as I can make out, neither D3 nor D2 goes all the way under the sealant in Figure 9.

A They go partly under the sealant.

Q And they both terminate there, is that what you see?

A Right, they terminate -- let me see exactly where they terminate. They terminate under the

sealant.

Q So those conductive lines, G1, D2 and D3, among those is it true that only G1 goes all the way under the sealant from the terminal portion into the region inside --

A That's correct.

Q -- of the sealant?

When I say "inside the sealant," I don't mean in the sealant itself, but I mean in the portion of the LCD demarked by the sealant?

A That is correct.

G1 is the layer that extends all the way outside. G1 is the one that extends from inside the sealant all the way out to outside of the sealant.

Q And that's shown in Figure 9, yes?

A And that's shown in Figure 9, correct.

Q Okay.

A So as you see here, the two wirings overlap under the sealant, they overlap between them, they have an electrical contact or electrical connection that goes through an opening in the insulating layer GI. So they show many of the features of the first and second wiring discussed in the '413.

Q Okay. Now, in your section paragraph 101 you reach the conclusion that only ordinary skill is

needed to have a configuration with sealant over the first and second wirings, but it seems to me that in this paragraph you do not express an opinion about whether the sealant is over a second region of the second wiring. Am I correct that that's not in the declaration?

A Well, the declaration identify the first and second regions and identify the first wiring in Sukegawa, so in my declaration I did not try to identify all of these region in Sukegawa. I draw the analogy between the wirings in Sukegawa and the wirings in -- the wirings in Nakamoto and the wirings in Sukegawa and the elements of the claims in '413 to -- to show that between the two pieces of art, in Sukegawa and Nakamoto, it was well known in the art where the sealant is relative to the wirings that leads to the terminal portions, and so it would take ordinary skill in the art to configure the wirings with the placement of the sealant, as indicated in Nakamoto.

As I spent several minutes describing to you, the wirings in Nakamoto have many similarities and serve many of the -- meet many of the limitations of the '413, so it is different wirings or something, is not related. They are both in

liquid crystal displays and they both are double layer wirings to reduce resistance. And I didn't go into a discussion, but if you look at the terminal region, you will see that above G1 you have D1. And D1, according to the specification, is a transparent display, D1.

Q And that's what?

A And that's transparent conductive layer. And as you see in the prior art of Nakamoto, the transparent conductive layer is the upper layer exposed in the terminal regions, and that is because it was well known that ITO provides protection against corrosion.

So you see in Nakamoto you have a double-layer line to create -- to reduce resistance and you have ITO to improve the liability and reduced corrosion.

Q Can you point out where it says what D1 is in Nakamoto? Do you have that handy?

A It will take me a minute or two. If I look through the pages here.

Okay. If you refer to page 25 in paragraph 80.

Q Yes, paragraph 80 says that G1 is a transparent conductor film.

A In the translation.

Q In the translation, yes.

A But if you turn to the original paragraph 80 of the Japanese version.

Q I'll be happy to do that.

Okay. Paragraph 80?

A If you forget all the Japanese and you just focus only on the English and the Latin character, you will see that the layer referred here is D1 and not as G1. So the G1 in the translation is a typo, it should be referred as D1.

Also, if you look in the Figure 4 and you look at the pixel active layer ITO 1, D1, right here, ITO 1, corner D1.

Q I see that.

A And that is referring to the pixel electrode region.

Q In the '413 patent claims where they call for a first region, do you understand that the first region is where the transparent conductive layer and the flexible printed circuit are both located over the second wiring?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Professor, I'm just referring to features 6

and 7 of claim 1, for example.

Feature 6 says, "a transparent conductive layer over a first region of the second wiring," and next element says, "the flexible printed circuit over the first wiring and the first region of the second wiring."

So my question is: Do you understand that the first region has both the transparent conductive layer and the flexible printed circuit located over the second wiring?

A Correct.

Q Is that the case in Nakamoto?

A As I said, I did not rely on Nakamoto to identify the first and second region omitting all the claim limitations of the '413. I rely on Sukegawa to do that. I rely on Nakamoto to indicate the placement of the sealant over the wirings and through the discussions that we have for quite some time. And as I went into detail to describe certain elements of Nakamoto, there are many of the limitations listed in the claims are met in the wirings described in Nakamoto.

So the wirings in Nakamoto and the wirings in Sukegawa are related. They have many commonalities, many features.

The ones in Sukegawa meet all the claim limitations as required under patent law, so I used Nakamoto to indicate the placement of the sealant for that wiring.

Q Well, referring to your declaration, Exhibit 1005, can you point out somewhere beginning on page 32, paragraph 89, or thereafter, telling us or showing us where your declaration tells us what the first region is in Sukegawa or Nakamoto?

A I put my papers here in order so I will not get lost.

Q If you give me the exhibit, I'll put it in order and staple it for you while you look at your declaration.

A In my declaration I went to the different limitations of the different claims and I compared to the different elements found in the prior art and I explore an opinion where there is a difference where those elements are similar. I think it is the -- the point-by-point analysis that you're asking me too, that was something that was done in the claim charts, and I have advised the attorneys in the creation of the claim charts and identified specifically each claim limitation for each -- for each limitation of each claim.

So I have contributed in the claim charts. In my declaration, I did not do this point-by-point analysis as you present that level much detail in the claim charts, but I consider those two to be -- the claim charts to base on the opinion I express in my declaration regarding those different regions or different elements.

Q Okay. So I understand your testimony to mean that your declaration, Exhibit 1005, does not explicitly tell us where the first region is for claim 1 in any of the prior art, but we can find it in the petition. Is that a correct conclusion from what you've just told me?

MR. GIBSON: Objection; form.

THE WITNESS: I said, in general, I grouped the claim limita- -- many of the claim limitations appear over and over in multiple claims. I group wherever is possible some of those limitations and I've expressed an opinion. If you wonder how those are related to the prior art, I can spend a minute to review my declaration to see how -- to what extent the first region is identified and described in my declaration.

BY MR. MANZO:

Q Yes, I would very much appreciate that.

And, of course, I think we're focusing on section X, Roman numeral X, but I'm not going to restrict your inquiry.

Section X is the one that begins at page 32 for the combination of Sukegawa in view of Nakamoto. But look wherever you want.

A So looking at paragraph 96 -- actually, 95 and 96. And 95, at least of the limitation which appears in multiple claims, quote, "the flexible printed circuit over the first wiring and first region of the second wiring," so the first region of the second wiring is the part of the second wiring which is below the flexible printed circuit.

So in paragraph 96 I read -- I write, "Sukegawa explains that in the multilayer wiring structure for providing an external connection, including a flexible printed circuit over the first wiring and the first region of the second wiring was a known method to provide connectivity. See Figure 2C, showing a flexible printed circuit (flexible wiring substrate 31) over the first wiring (lower layer metal wiring 2) and the first region of the second wiring (upper layer metal wiring 7)."

So shown in Figure 2C the part of the upper layer wiring 7 that is below the flexible printed

circuit is defining in the first region of the second wiring.

And in an earlier paragraph I have identified the 7 as the first -- the second wiring.

Q Only. That answers my question. Thank you.

Now, going back to Nakamoto, you've said that D1 is a transparent conductive layer of ITO, I think?

A No, that is what the specification, Nakamoto state.

Q And you referred us back to the Japanese text.

Do you read Japanese?

A No, I don't. I look at the Figure 4 that it referred to the -- to the ITO 1, which is the pixel electrode, and I saw it was labeled as D1.

And then in paragraph 8 it talks about a transparent pixel electrode IT0 1, and in this paragraph it is referred to as G1. And that is in contrast to whatever is in Figure 4 where ITO 1 is also labeled as D1. So I thought maybe that is a typo, so that's why I turn to the Japanese version to see in the Latin characters are used in the proper sequence, and that's how the mistake. I do

not claim that I read Japanese or knowledgeable.

Q I understand.

A Or have any sort of language of that language -- any sort of knowledge of that language.

Q I understand.

Do you agree that D1 is not an insulator, then; is that correct?

A D1 is ITO, transparent conductive layer, that's a conductive layer.

Q Which means it is not an insulator?

A Correct.

Q And in Figure 9, are D1 and/or G1 the external connecting lines?

A Well, the '413 does not refer to them as external connecting lines, and I think the '204 patent connects them as external connecting lines.

Q Okay. Well, they may be referred to that way in the claims, but in the figure there is a label that says "external connection lines, 403." I'm just wondering if there are external connection lines in Figure 9 of Nakamoto. And, if there are, what are they labeled?

A Since you refer to the external connection lines, may I also refer you to column 9 on the '413, line 47. So it reads, "In the present embodiment,

the auxiliary lines and external connection lines may be replaced with each other to use the lines provided in the layer under the first inter-layer film as external connection lines which establish electrical connections with the EPC."

So you see here that paragraph, column 9, lines 47 to 51, is covering what is depicted in Figure 9 of Nakamoto where the external connection line is the lower line.

So in view of the specifications of the '413, Nakamoto Figure 9 is relevant.

Q And how is the external connection line labeled?

MR. GIBSON: Objection; form.

MR. MANZO: Strike that.

Q Does Figure 9 show an external connection line?

A Figure 9 and all the other figures that we discussed in Nakamoto, they describe wirings that connect the gate lines and data lines to the terminal regions. And I tried to present the similarities of those lines to the specifications and to the claims discussed in '413.

I've not performed the analysis in order to meet all the claim limitations in Nakamoto and I'm

just pointing out some features of those lines.

Q Okay. Would you agree with me, Professor, that looking at Figure 9 there is no insulation between D2 and D3?

A D2, D3 are formed sequentially, as one is a chrome and the other is aluminum. The combined double layer is forming a wiring.

Q Okay. And is there any insulation between D1 and D2 in Figure 9?

A Between D1 and D2? No.

Q In the region of the sealant in Figure 9, is the first insulator that is above D1 labeled as PSV1?

A That is correct. For the portions of where PSV1 overlaps D1, there are portions of D1 that are covered by the D2 and D3, and those are intermediate layers before PSV1.

Q Would you agree that in Figure 9 there is no second wiring that extends across the sealant from a region to a region on one side of the sealant to a region on one side of the sealant to a region on the opposite side of the sealant?

MR. GIBSON: Objection; form.

THE WITNESS: You are using a different terms from the claims and sometimes you are using

terms from the specifications.

As I said a moment ago, I did not try to identify all the elements of the claims in Nakamoto. I described the series of such elements and how they are meeting the specifications. I did not do the analysis to find all those limitations.

BY MR. MANZO:

Q Very well.

This is a good time for changing the video disk.

THE VIDEOGRAPHER: We are off the record. The time is 4:55 p.m. on July 1st, 2013. This is the end of video number 3 of the continuing deposition of Dr. Milt Hatalis.

(Recess.)

THE VIDEOGRAPHER: We are back on the record. The time is 5:13 p.m. on July 1st, 2013. This is the beginning of video number 4 of the deposition of Dr. Milt Hatalis.

BY MR. MANZO:

Q Professor, if you look at paragraph 99 of your declaration marked as Exhibit 1005, you'll see on the third line that you referred to a, quote, more secure connection, closed quote.

Does Sukegawa actually say that or is that

your characterization?

A Give me a moment, please.

Q Certainly.

A If we look at Sukegawa in the column 6, line 61, continuing to column 7, line 8, it describes the double-layer wiring, and it shows since -- presents that the double-layer wiring, when have you multiple holes 6, element 6, that is made less peeling, p-e-e-l-i-n-g. So there is less peeling if you have a double-layer line, that means -- and that I what I mean by making a connection which is more secure, it is more resistance to peeling.

Q Are you referring to covering the top metal wiring 7 with the layer 8 of ITO or the film 9 or are you referring to the lower wiring 2?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q With regard to your explanation of making a more secure connection.

A Well, the peeling connection I refer to is one example where Sukegawa talks about more secure connection. And that was when you having the layer 7 anchored to layer 2 through the holes 6.

If you're referring to the double layer

between 7 and 8, there is another section in Sukegawa, and that is in column 1, line 28, and it reads, "In such a structure, the terminal portion for connection is made of a metal wiring layer covered with a chemically stable transparent conductive film."

So in this section it discuss the advantage of having transparent conductive layer, which is a chemically stable layer, so the secure connection applies to multiple double-layer wiring elements, so depending upon which one you're referring to.

But in any case, Sukegawa discussed those advantages. They are not my conclusions.

Q Well, in paragraph 99, the first line, you refer to a multilayer wiring structure. So what is the multilayer wiring structure that you referred to at that part of your declaration?

A The multilayer wiring structure that starts from the wiring 2, includes the wiring 7 and includes the wiring 8.

So in that section 2 and 7, it create two parallel lines that reduce resistance, and to a lesser extent 8 can also contribute to the overall lateral reduction of resistance. 2 further serves to fasten 7 down to make it more resistant for

peeling and 8 serves to provide a protection against corrosion.

Two parallel lines instead of patterned alliance -- page 161, line 7, to create two parallel lines.

MR. MANZO: The professor is saying that you've got -- the rough transcript says "pattern alliance," and he was saying "parallel lines."

Q So, Professor, it's correct, I take it, that in Sukegawa layer 8, or film 8, is only in the terminal region; is that correct?

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Well, maybe I can restate that.

Professor, in Sukegawa is the layer 8 located in only the terminal region?

A What do you mean by "terminal region"?

Q Well, if I look at Figure 1B, if you look at the bottom left part of it, there is an arrow pointing upwards and under the arrowhead there is the legend "for display portion." And that same indication is found in Figure 3B and 3E.

Do you see that?

A I see that.

Q So I understand there is a terminal portion

and a display portion. Is that understanding correct?

A What it referred to as display portion, it refers to the area where you have the scan lines and the data signal lines and also you have the pixel electrodes. So you have multiple wirings at different levels. So not all elements shown in the Figures 1B can extend to the display portion because they will make shorts to connections -- they will be touching other metal lines, and that will lead to a malfunctioning of the display.

Whereas the terminal portion that you refer is typically referred to a region outside the sealant. And, as we discussed earlier, again, the sealant is also someone skilled in the art, the portions of the structures shown in Figure 2C.

Q So can we agree that this structure 8 extends in -- does not extend in the display portion?

MR. GIBSON: Objection; form.

THE WITNESS: The only element of those three layers, 7, 8 and 2, that can extend to the display portion is the element that will be used to form the wiring for that particular element. For example, if it is -- if we're going to have the scan

line wiring, then only element 2 can extend. If we're going to have the data signal wiring, then only 7 can extend all the way to the display portion.

They can extend under the sealant, but cannot interfere with the actual pixel electrodes or with the data scan lines that's there, unless the material which extends all across is the same material used to perform scan lines or data lines, which is -- the purpose of extension is to form those lines.

BY MR. MANZO:

Q I see. And the purpose of 8 is to cover the upper level of metal, number 7, correct?

A 8 is to cover and protect the parts that will be left exposed during the assembly process for putting down the flexible printed circuit or during the testing purpose before putting down the element 13.

Q Okay. So we are talking about 8 being in the terminal portion of the LCD; is that correct?

MR. GIBSON: Objection; form.

THE WITNESS: You're asking the same thing. I'm going to give you an answer.

What do you mean by "terminal portion"? I

think I explained -- I answered it and you asked me again. Is your terminal portion different from the previous terminal portion or is it something I answered that is not clear?

BY MR. MANZO:

Q No. I'm trying to make the answer simpler.

If you remember, we looked at Exhibit 2010, and you drew where a person of skill in the art in consideration of Nakamoto would place the sealant.

Do you remember that?

A Yes. And then based on that, in view of Nakamoto, I placed the sealant in Figure 2C of Sukegawa.

Q Okay. So maybe a simple way to ask my question is: Do you agree that the layer 8 does not go further to the left of this exhibit and, instead, it stops under the sealant where the sealant would go?

A Well, how far -- it can certainly -- it will have to stop before the first pixel electrode. Where, exactly, it will stop will be determined by the particular design. It cannot extend so far as to touch the first pixel electrode, because it will then be connected and the signal from the flexible printed circuit will then appear to that pixel

electrode. So it will to stop short of that.

How far extends between the edge of where it is now and inwards, it will depend upon the particular design, the particular materials used and --

Q Okay. Is there any indication in Sukegawa that it can go from one side of the sealant to the other side of the sealant?

MR. GIBSON: Objection; form.

THE WITNESS: You mean form one side of the display over to the other side of the display?

BY MR. MANZO:

Q No, I did not mean that.

There is a sealant somewhere.

A Right.

Q And somewhere inside the sealant is a display area?

A The sealant on one side.

Q You're talking about the sealant circumscribes --

A I understand.

Q -- a display area.

A Yes.

Q And outside of the sealant is what I've been calling the terminal portion, right or wrong.

A Okay. That's where you're referring outside the sealant as the terminal portion?

Q Right.

A Okay.

Q And my question is -- and when I say "inside the sealant," I don't mean literally inside the sealant itself, I mean in the part of the LCD within the region circumscribed by the sealant.

A Okay. I understand.

Q Good. So my question is: Is there any indication in the Sukegawa patent that layer 8 can traverse past the sealant?

A On the inside portion of --

Q Yes, of the device.

A I don't think Sukegawa describes that element that you're referring to. It is a very specific question. Sukegawa describes certain features, and someone skilled in the art will then have to take the features of Sukegawa, other prior art and the particular requirements for the display product that you want to fabricate in order to make designs.

Q I understand.

A I told you in principle you cannot go inside the array, but where, exactly, you will stop

it will depend upon many considerations.

Q Thank you.

A For example, in Nakamoto the ITO, I believe, extends inside the sealant, but again stops short of the array.

Q Well --

A If you look at the element D1, which we refer in Nakamoto as ITO, it shows that it continues from outside the sealant, under the sealant and continues to the display.

But it will stop short of what is array, because to continue to create a defect. So a different pieces of prior art and depending upon the design, it provide different implementations. All these variations were well known in the art.

Q Now, if the ITO extends through or under the sealant, does it cause a height difference by virtue of it being -- of the ITO being there? When I say "height difference," I mean it pushes the space apart from the counter-substrate to the substrate.

A ITO is a very thin layer relative to the thickness of the other layers, so it will have a very small effect on the high difference spread to the other layers.

Q Going back to Sukegawa, with respect to the relationship of wiring 2 to wiring 7, wiring 2 is beneath wiring 7; is that right?

A 2 is right onto the substrate, correct.

Q So is it fair to say that the direction of signal path from 7 to 2 is downward?

MR. GIBSON: Objection; form.

THE WITNESS: Well, within any given context, you have -- within a given contact, the signal will be downward, but between two adjacent or between the first and the last, you have the signal that will also propagate laterally.

In this particular embodiment, there are four holes that are depicted, so depending upon the extent of that region, and, of course, someone skilled in the art will choose to make even more holes, the signal will propagate on both lines in the lateral direction, from the portion of the lines that starts from the first hole all the way out to the portion of the line that ends in the last hole.

BY MR. MANZO:

Q And it will also propagate downward through the holes; is that right?

A In each individual hole, within an individual hole will propagate downwards.

Within a hole -- you see, a hole has a finite extent, so even within a hole, which may be several microns long, the two wiring, 7 and 2, will also constitute two parallel lines. So, in a way, you also have a lower resistance in the X direction or towards that direction which is along the bottom of the hole, you'll also have a lower resistance because you also have two lines.

So the power combination of the lines in order to reduce -- which results in overall reduction to the resistance of the structure is continuous, starting from the rightmost hole in Figure 2C from the rightmost edge of the first hole continuing all the way out to the left edge of the last hole.

In that entire segment, the two lines constitute two parallel lines. Whether they are touching physically or they are in separation, for the purpose of electroanalysis they act as two parallel lines.

Q Thank you.

If a person ordinarily skilled in the art wanted to lower the resistance of wiring in the terminal region of a LCD, wouldn't he or she be more likely to use other ways than to add another line,

such as widening the existing line or thickening it?

MR. GIBSON: Objection; form.

THE WITNESS: In the semiconductor art, you -- one who has skill in the art will understand the advantages and the disadvantages of any action that he takes in order to achieve a certain goal.

So if, for example, you say you increase the thickness of a line, of a metal, and let that be the wiring 2, for example --

BY MR. MANZO:

Q Okay.

A -- you say why, don't we just make -- triple the thickness of 2, that will have some -- and don't add 7, for the sake of argument, this is hypothetical example that you mentioned.

If you increase the thickness of 2, you increase the thickness of the scan lines, which go across the display.

As we talked about, you have the scan lines in orthogonal direction, you have the data lines in an orthogonal direction, you're getting the data lines. So the data lines have to go up and down the crossovers with the 2. If you make 2 thick, you make that more difficult for the data wiring to go up and down and make a step coverage more difficult.

Q I see.

A If you make the -- so there is a limitation of how thick you can make a line.

If you make the line wider, you may have limitations of how close you can space the lines before one is touching another one. You make yourself susceptible to particle defects. In the area of display itself, you don't want to make the lines too wide because then they block the light.

So on the other hand, a double-layer line may also have some shortcomings which are coming from increased complexity.

So someone skilled in the art will take all the advantages and disadvantages from every possible way that he can use to make a structure and then choose the best way possible for the particular application.

In this particular example where you have to make a connection and then you have to potentially peel that connection and redo the connection, you have to make it resistant to peeling, as Sukegawa does.

And one way to make it resistant to peeling is to anchor it, one layer with respect to another layer.

Q In your declaration, paragraph 101, I just wanted to ask you about 24. This phrase on the very bottom line of page 36, very near the end, the phrase that I'm asking you about is, quote, near close, closed quote.

What does that mean? Or is --

A So if we look at Figure 9, you have tape carrier package, 11, TCP, and that is instead of -- -- maybe that "near close" maybe that was a typo, I have to write "very close" -- it is very -- located very close to the sealant. It's a gap that is -- according to Sukegawa is used for testing or a small gap in order to be able to align and move the tape carrier package.

But you don't want to make that gap too wide, because, as I said earlier today, that's a region of the display that gets wasted that contributes to the data area, not useful to make display, and that unnecessarily increases the size of the display, which limits how many displays can be produced on a given mother glass size. And also it contributes to an increase in the line resistance if the length of the line becomes longer. So it serves no advantage to make it far away.

Q If you turn to paragraph 106 of your

declaration, at page 38 you refer to the -- in parentheses on the second line, you say, quote, the sealant having been discussed above.

My question is where above?

A Can you give me a moment to read it, please?

The sealant starts from paragraph 98, the oldest paragraphs from 98 to 106, it's discussions of -- that refer to the sealant.

Q Okay. Do you agree that Sukegawa does not teach or suggest or motivate a person ordinarily skilled in the relevant art in 1997 to place a sealant in direct contact with a second insulating film that is located over the first and second wiring separated by a first insulator where both of the first and second wirings traverse beneath the sealant.

MR. GIBSON: Objection; form.

THE WITNESS: No.

BY MR. MANZO:

Q You don't agree?

A That's what you asked me, correct?

Q Yes, I asked you that.

A You asked if I agree it does not teach or suggest and so on, and I said I do not agree with

your statement.

Q So you think that Sukegawa would teach the direct contact with a second insulating film, or at least teach, suggest or motivate the combination I suggested?

MR. GIBSON: Objection; form.

THE WITNESS: Yes -- directed between the sealant and the second insulating film, if I understand your question.

BY MR. MANZO:

Q So is the second insulating film the layer 9 in Figure 2C?

A Correct.

Q And --

A And that, as you see in my drawing that I have annotated, an exhibit that you handed me over you see that sealant is in direct contact with 9.

Q Yes.

A You have argue on the placement of the sealants, and reading in the response, you also -- the patent owner argue the placement of the sealant. But no matter where the sealant is placed, whether you agree or not agree with my drawing, in view of Nakamoto, you have to agree that 9 is continuous.

So wherever you place the sealant, even if

you do not place it, where I place it, where a person skilled in the art will place it, where I have placed it, but for whatever reasons you disagree that that is correct. But wherever you choose to place it, it will still be placed over 9.

Q Okay. Let's assume that's correct for now.

A What do you mean by assuming it is correct? You disagree that 9 is continuous?

Q I'm just trying to ask the rest of the question?

A I'm trying to understand also your formulation.

Q I understand. I'll try to be more clear. Forgive me for my imprecision here, but it is important that we understand this correctly.

So assuming that the sealant does contact 9, take that as a given for the question. My question was assuming that that's true, does Sukegawa disclose, teach, suggest or motivate a person skilled in the art that both the first wiring and the second wiring should traverse, completely traverse, the sealant?

MR. GIBSON: Objection; form.

THE WITNESS: I -- is it a claimed limitation that requires that the first wiring and

the second wiring traverse the sealant, or are you talking about hypothetical structures?

BY MR. MANZO:

Q Well, if you look at Exhibit 1001, which is the '413 patent, looking at the figure on the first page of the patent, you'll see that the sealant at the top marked 105, and it's in contact directly with this second insulating layer marked 113, and that below that both the external connection line, 403, and the auxiliary line, 401, go past where the sealant is, at least that's what I see.

Do you see that too?

A I see in the Figure 4A which refers to a particular embodiment, but I asked you whether there are specifications in the claims that will require that -- sorry -- whether there are limitations in the claims that requires that.

Q Well, my question is regardless of the claims, I'm asking you a factual question.

Does Sukegawa teach that or not?

MR. GIBSON: Objection; form.

THE WITNESS: Sukegawa teaches that the lines can overlap with the sealant. Someone skilled in the art will determine if they wish to extend below the sealant one or both, depending upon the

particular design of product they wish to propagate.

You asked me hypothetically, in the design of a particular display or particular product -- I'm sorry, I don't understand completely the nature of your question.

BY MR. MANZO:

Q Well, I think I'm -- what I'm hearing you say is that a person of ordinary skill in the art will decide. But my question was: Is there anything shown or described in Sukegawa that says that both of these, lines 7 and 2, should extend from one side of the sealant on the terminal portion and go past the sealant to the other side of the sealant?

MR. GIBSON: Objection; form.

THE WITNESS: Well, definitely, as I highlight earlier, the prior art that is in Figure 2C that refers to that discuss to the connection. But for the scan lines, then 2 can extend under the sealant, and not only under the sealant, but can extend all the way out to the other side to the display.

When you are -- form the pads for the data lines, data signal lines, as I described earlier, 7 will be the one that will extend all the way under

the sealant and all the way across the display.

So there's nothing in Sukegawa that puts any limitation on whether 2 or 7 cannot extend under the sealant or across the sealant. Because in one set of pads, one is extended, at least, in the other set of pads, the other is extended.

So it will take someone ordinarily skilled in the art to say that if for the particular display product that they are making, they need to get that extra improvement in resistance across the length of the sealant to continue both lines for the length of the sealant.

But the length of the sealant relative to the length of the pad and relative to the length of the display is a small part.

But there is no limitation imposed that it cannot be done across the length of the sealant in the teaching of Sukegawa. Whether someone does it or does not -- choose not to do it, it will depend upon the particular design.

As you mentioned earlier, whatever we put -- and the '413 discuss, whatever we put under the sealant will increase the height of the materials under the sealant.

One difference between the '413 and the

Sukegawa is that in the '413 it referring to displays that had integrated display drivers within, so you need to propagate under the sealant and you need to reach that display driver at the periphery of the display, of the TFT array.

In Sukegawa it is a display that is using amorphous silicon and it uses external drivers, and that's why you have hundreds of terminal connections, each one for each gate line and each data line. Hence, the display would start right after the end of the sealant, so it would not be a long distance past the sealant where you have something else, such as the driver that the '413 discuss, that the length of the line that you have, it will be long.

So that's why I said whether you choose to have it as a single layer or double layer will depend upon the particular display product and application.

If you have integrated drivers and you need to propagate long distances and you're sensitive to the resistance, you can have a double-layer wiring as -- if you continue double-layer wiring past the sealant and if you don't need that one, then you will stop short of extending -- you will

stop somewhere under the sealant.

There is not one unique answer, always this or always that. It will depend upon the design and the teaching -- excuse me, the design and requirements of that particular system.

Definitely Sukegawa does not limit into one or the other. The teaching is there to implement both approaches.

BY MR. MANZO:

Q Is it? Where is the teaching that says you can have both of these lines going all the way past the sealant?

A Well, you have two parallel lines that extend four holes -- 1, 2, 3, 4.

Q I see that.

A And they extend past the edge of the flexible print circuit, element 31. And so -- and the contents of double-layer lines, multilayer lines, is not new, it is something that has been used in semiconductor art for a long, long time. So this is not a revelation or a new innovation. Double layer lines were well known in semiconductor art that are effective in reducing resistance between two points.

And Sukegawa talks about using this

structure your to the reduce resistance.

And, as I said earlier in my testimony, someone skilled in the art need to extend longer distance, there's no -- they can do that. There's nothing in the Sukegawa to suggest otherwise. On the contrary, it does show structure, so all someone needs to do is add more contact holes.

Q Do you agree that in Sukegawa the ITO layer 8 is never above, never on top of the layer 9?

A In the specific embodiments depicted in the different figures, is not. But that's not -- someone skilled in the art will not be able to change, and there are ways to put 8 on top of 9.

As I said, there are three layers here and one is fixed in the order, and that is 7. And then you have 8 and 9 to lay over. And there are two possible ways to lay them over. Put 7 first -- sorry.

Put 8 first and then 9 or put 9 first and then put 8. It's not rocket science. People knew how to do those things for a while.

Q Is there any embodiments shown in Sukegawa where 9 is put down before 8?

A I think I said not in the particular embodiments described in Sukegawa, but someone

skilled in the art will know how to do that.

Q Was there a reason why Sukegawa put 8 down before putting 9 down in the structure shown in Figure 2C or any of the other structures?

A I do not recall Sukegawa putting a reason of limiting to this particular embodiment or this particular structure.

Q Could -- well, does 9 have a function in Sukegawa?

A Sure. All layers have a function, otherwise they wouldn't be used because they have costs to the manufacturer. So 9 is a --

Q I think you called it a passivation layer earlier.

A Right. As we saw in Nakamoto, there was a label, passivation layer, in Nakamoto.

Q What is a passivation layer?

A The final insulating layer that puts on top of the electronic devices for protection.

Q If 8 were on top of 9, we've decided that 8 is a conductive layer, isn't it?

A (No audible response.)

Q 8 is the ITO, the transparent conductive layer.

A 8 is the transparent conductive layer.

Q Would you want to have that on top of your passivation layer?

A If someone involved skilled in the art would choose to have 8 as the outer layer or the last layer, in other words, put 9 first and then the 8 on top of 9. Then instead of -- then that person could create an opening in 9 before put down the 8.

Q Did you say could create an opening in 9 or would have created an opening in 9?

A If you wanted 9 to touch 7, then it should have created -- would have created -- now you are playing with my English and it is speculative.

Q I apologize. I didn't mean to do that.

A If 8 -- if 9 is between 7 and 8, then contacts are required for 8 to make the connection to 7.

Q Well, could layer 9 serve its function if 8 were on top of 9?

MR. GIBSON: Objection; form.

THE WITNESS: Yes.

BY MR. MANZO:

Q Can you explain that?

A Well, 9 serves to protect the regions below, and from, say, moisture or other things that may corrode the metals. But as we discussed, 8

is -- Sukegawa refers to chemically stable material. So having that material exposed as an outer layer, it will not create a problem.

And that's also what is disclosed in Nakamoto, so you have multiple pieces of prior art that have 8 exposed. And even after you opening the -- after you create the opening in 9 in Figure 2C, 8 is exposed. So 8 does not need to have environmental protection.

MR. MANZO: Let me take a recess, please.

THE VIDEOGRAPHER: We are off the record. The time is 6:15 p.m.

(Recess.)

THE VIDEOGRAPHER: We are back on the record. The time is 6:25 p.m.

BY MR. MANZO:

Q Going back to Sukegawa and layer 9 and passivation, what is -- I'm not sure that I understood your explanation of what a passivation layer is in an LCD in this region.

Could you help me understand that? What does layer 9 achieve?

A So in column 5, lines 12 it list finally a silicon nitride film of about 200-nanometer thickness covering both the transistor-forming

portion and the terminal portion is deposited by a plasma on CPT method to perform a protective insulating film 9.

So 9 is silicon nitride film. A nitride film is resistant to -- does not -- it does not let moisture and oxygen to go through, so it protects the thin-film transistors and the wirings from corrosion.

In the thin-film transistor area, there is also another layer that will be deposited. That will be the rubbing layers, or liquid crystal alignment layers.

And those layers will go through what's known as the rubbing process. It's a physical process where -- almost like a brush will go and rub the substrate to create channels where the liquid crystal molecules will lay down and thus be aligned along the direction of the rubbing, the rubbing direction.

So having an insulating passivation layer above the wiring above the TFTs and below the rubbing layer will serve also as a mechanical protection to the lines and the transistors so they will not be damaged or scratched. So it serves a plurality of reasons, purposes.

Q I see. I see.

Looking at Figure 2C, can you see that part of the flexible printed circuit contacts that layer 9, the unlabeled part of it over here, on the right-hand side of Figure 2C?

A This is what is depicted, so I cannot argue with what is shown there.

But as you -- as I think I alluded earlier, there is some alignment process that will happen during the application of the flexible printed circuit, because you have one element, being the flexible printed circuit, and you have the substrate that has this wirings for underneath. And the two have to be aligned, because there are hundreds of them, so you don't want the wrong signal to go to the wrong connection.

So the two will first be aligned and then they will be pressed to make a contact, and there will be some sealant material in between.

Now, in this alignment process, if the 31 is shifted to the left, that overlap that you indicated to me on the right portion of the figure may not exist. It all depends how the 31 will be aligned and what is the proper specifications during the alignment process in whether it is going to be

successful or a failure.

MR. GIBSON: I think we're at seven hours.

MR. MANZO: Okay. In that case, we have no further questions.

MR. GIBSON: I do not have any questions.

MR. MANZO: Well, let me ask him one more question.

Q Is there anything you wanted me to ask you that I didn't ask you? You don't have to answer that.

A I'm sure you have the opportunity tomorrow to ask me a lot more questions that you didn't ask me today because the -- are you going to be the person that will depose me tomorrow?

Q Yes.

A The specifications are the same, so I'm sure there's plenty of opportunity to ask me lots of questions tomorrow.

MR. GIBSON: With that, I think we're done.

MR. MANZO: Thank you very much, Dr. Hatalis. Very nice to meet you.

THE WITNESS: Thank you.

THE VIDEOGRAPHER: We are off the record. The time is 6:32 p.m. This concludes today's testimony given by Dr. Milt Hatalis. The total

number of media used was 4 and will be retained by Veritext Legal Solutions.

(TIME NOTED: 6:32 p.m.)

I, MILTIADIS HATALIS, PH.D., do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made any corrections as appear noted, in ink, initialed by me, or attached hereto; that my testimony as contained herein, as corrected, is true and correct.

EXECUTED this _____day of _____, 2013, at _____, _____.
(City) (State)

_____
MILTIADIS HATALIS, PH.D.
Volume I

I, the undersigned, a Certified Shorthand Reporter of the State of California, do hereby certify:

That the foregoing proceedings were taken before me at the time and place herein set forth; that any witnesses in the foregoing proceedings, prior to testifying, were placed under oath; that a true and correct record of the proceedings was made by me using machine shorthand which was thereafter transcribed under my direction; further, that the foregoing is an accurate transcription thereof.

I further certify that I am neither financially interested in the action nor a relative or employee of any attorney of any of the parties.

IN WITNESS WHEREOF, I have this date subscribed my name.

Dated: 5 July 2013

DENISE BARDSLEY
CSR No. 11241