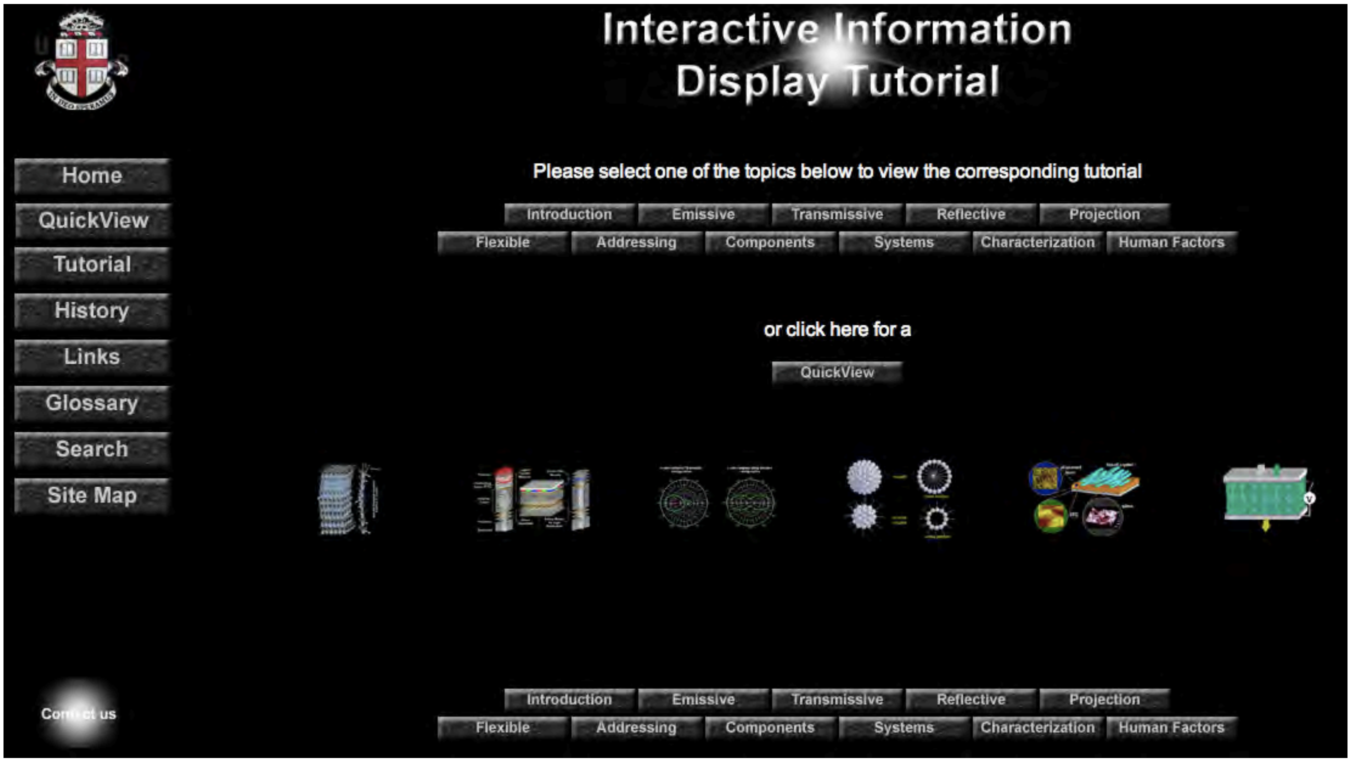
SEL EXHIBIT NO. 2037

INNOLUX CORP. v. PATENT OF SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

IPR2013-00066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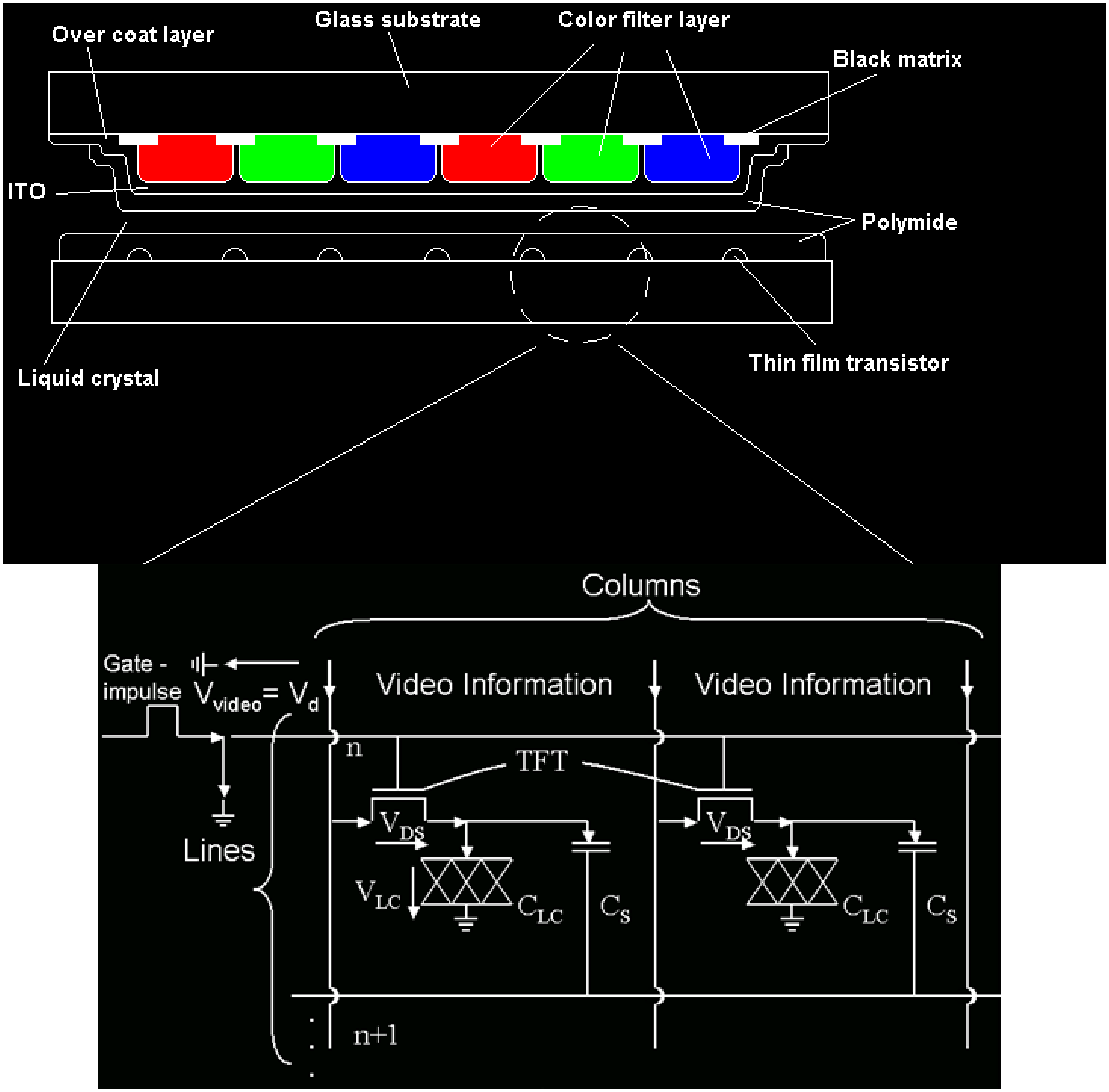
Interactive Information Display Tutorial

Addressing Schemes

Module 36: Active Matrix Addressing

36.1. Basics of Active Matrix Addressing Technology

Addressing displays with direct drive or passive means cannot provide the resolution or gray scale of high performance displays. The active matrix substrate enables high resolution and controllable gray scale. The figure below shows the first schematic of an active matrix substrate. Many more schematics and a more in depth understanding will follow. The circuit below shows the TFT circuit and cross section



FETs, created using thin film technology. The primary function of the FETs is to act as a non-linear switch at each pixel. To render a gate conductive, a positive gate pulse, V_g, is used. The FETs in the other rows are blocked by referencing the rows to ground. The video information is fed in through the columns and the conducting TFTs simultaneously. The video voltage V_d, which creates the desired gray levels, charges the liquid crystal capacitor, C_{LC}, and an additional thin film storage capacitor to a voltage V_d. This is a one row at a time operation. During the time when the capacitor is charging, the next capacitor in the succeeding line is grounded and therefore connected in parallel to C_{LC}. This can introduce distortion in the waveforms.

To render an image, the pixel switches must charge N rows in a given frame interval, T_f, therefore the individual row address time is

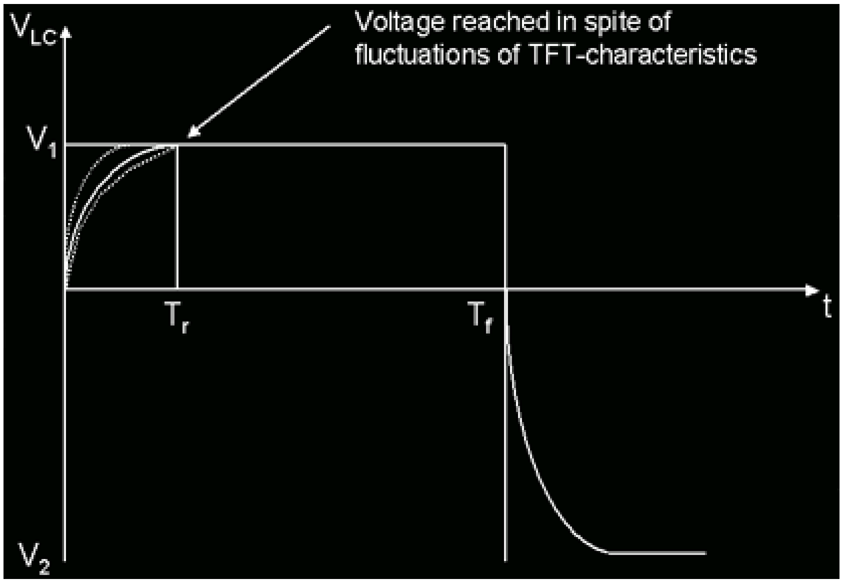
$$T_r = T_f / N$$

Now we can look at the voltage across the liquid crystal.

During the row address time, Tr, the storage capacities are charged with the time constant

$$T_{on} = (C_{LC} + C_s)R_{on} \leq 0.1\,T = 0.1\frac{Tf}{N}$$

where R_{on} represents the 'on' resistance of the TFT. The inequality enforces the condition that the voltage across the liquid crystal is only 1% below the desired voltage V_d at the end of T_r. After the time T_r, the transistor is blocked, but still maintains a finite resistance, R_{off}.



After ΔT_f the row is addressed again and the new image is rendered. During this time, the discharge of the capacitors should be minimal to provide an output luminance of the pixel as constant as possible, providing a flicker free image. The time constant for T_{off} of the discharge is given by the expression:

$$T_{on} = (C_{LC} + C_s)R_{on} \leq 0.1\,T = 0.1\frac{Tf}{N}$$

thereby ensuring only a 1% drop at T_f. By combining expressions for T_{on} and T_{off}, the following equation can be derived.

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