**SEL EXHIBIT 2023**

INNOLUX CORPORATION v. PATENT OF SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

IPR2013-00066

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRAIL AND APPEAL BOARD

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| INNOLUX CORPORATION,<br><br>Petitioner,<br><br>vs.<br><br>PATENT OF SEMICONDUCTOR ENERGY LABORATORY CO., LTD.,<br><br>Patent Owner. | No. IPR2013-00068<br>Patent 8,068,204 |

VIDEOTAPED DEPOSITION OF MILTIADIS HATALIS, PH.D.
Irvine, California
Tuesday, July 2, 2013
Volume I

Reported by:
DENISE BARDSLEY
CSR No. 11241
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PAGES 1 - 153

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Videotaped deposition of MILTIADIS HATALIS, PH.D., Volume I, taken on behalf of Patent Owner, at 3 Park Plaza, Suite 1100, Irvine, California, beginning at 9:14 a.m. and ending at 5:44 p.m. on Tuesday, July 2, 2013, before DENISE BARDSLEY, Certified Shorthand Reporter No. 11241.

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INDEX



EXHIBITS

(NONE)

Irvine, California, Tuesday, July 2, 2013

9:14 a.m.

THE VIDEOGRAPHER: Good morning.

We are on the record at 9:14 a.m. on July 2nd, 2013. This is the video-recorded deposition of Dr. Milt Hatalis. My name is Scott Slater, here with our court reporter, Denise Bardsley. 09:14:45

We are here from Veritext Legal Solutions at the request of counsel for the patent owner. 09:15:07

This deposition is being held at 3 Park Plaza, Suite 1100, in Irvine, California 92614. The caption of this case is Innolux Corporation versus Patent of Semiconductor Energy Laboratory Co., Ltd., Case No. IPR2013-00068, Patent 8,068,204. 09:15:34

Please note that audio and video recording will take place unless all parties agree to go off the record. The microphones are sensitive and may pick up whispers, private conversations or cellular interference. I am not authorized to administer an oath, I am not related to any party in this action, nor am I financially interested in the outcome in any way. 09:15:57

May I please have an agreement from all parties that we may proceed? 09:16:08

MR. MANZO: So agreed.

MR. GIBSON: I agree.

THE VIDEOGRAPHER: Thank you.

At this time will Counsel and all present please identify themselves for the record. 09:16:17

MR. MANZO: I'm Edward Manzo for the patent owner, from the firm -- law firm of Husch Blackwell, LLP. With me is my partner, Mark Murphy, from the same firm, and also with us is --

MR. SCHLITTER: Stan Schlitter from Steptoe & Johnson, also for the patent owner. 09:16:38

MR. GIBSON: Stan Gibson on behalf of the petitioner.

THE VIDEOGRAPHER: Thank you very much. Will the court reporter please administer the oath. 09:16:47

MILTIADIS HATALIS, PH.D.,

having been administered an oath, was examined and testified as follows:

EXAMINATION

BY MR. MANZO:

Q Good morning, Professor.

A Good morning.

Q I am placing before you a copy of the Shiba 09:17:11

reference, which was marked as Exhibit 1003 previously, and it bears Patent No. 5,684,555.

Is it okay with you if we just refer to that as Shiba in these proceedings?

A That will be fine. 09:17:40

Q Now, before we dig into the examination, we asked you a lot of questions yesterday morning about your background, and we're hoping that we don't need to repeat all those today and that we can rely on yesterday's testimony with regard to your background 09:18:29 and other examination on technical issues.

Is that agreeable, Counsel?

MR. GIBSON: His background is fine; I don't believe it's changed from yesterday to today. I'm not sure what you mean by rely on other 09:18:44 examination on technical issues. Certainly we don't need to cover his background again.

MR. SCHLITTER: We intend to use both the transcripts, probably, from yesterday and today and both the '413 IPR and '204 IPR if that turns out to 09:19:04 be appropriate. There are a lot of questions that relate to the same exhibits in both --

MR. GIBSON: I don't disagree with that. I just don't know what it means to use the same technical understanding, so it is just too broad of 09:19:20

a term.

If we have an objection to using something in a different one, then I don't know what that would be. At this point I'd have to see how we are using it. I don't think we need to repeat questions from yesterday. 09:19:32

MR. SCHLITTER: Okay.

MR. MANZO: Thank you.

Q Professor --

A Before we proceed, since you're not going to be asking me any more questions about my background, may I make a comment related to some of the questions you asked me yesterday, for the record? 09:19:41

Q That's somewhat unusual. 09:19:59

What are they? Technical issues?

A No, no. They are related to my experience in patent litigation. You asked me a lot of questions in those areas and you asked me, percentagewise, about the income I received from patent litigations and so on. 09:20:16

Q Sure. Why don't you go ahead.

A So --

Q Let me ask you a question.

Could you please clarify some of the issues 09:20:27

that were raised yesterday that you thought about further overnight regarding your background.

A Sure. Thank you.

You asked me a lot of questions about my litigation experience against -- a series of case against SEL, and you also asked me a lot of questions related to, percentagewise, the income I received from patent litigation work. And I was going to make a comment that compared to the experts that wrote the two response -- the two expert reports for the last two patents that I was involved, I find out that I have less litigation cases than them and that their rates are significantly higher than mine. 09:20:40 09:21:03

So I just want to clarify, that case, that some of them also work for more than one case, several cases on behalf of SEL. 09:21:24

You comment that I worked against SEL, that's because some of my clients were being sued -- not my clients, but some of the law firms were being sued by SEL, so I represented defendants in this case, or in some case. And the other experts represented SEL against some of the same clients. 09:21:42

So my litigation experience and my income is less than what it is, than the other experts. 09:22:03

Q I see.

A Thank you.

Q Thank you.

Professor, I'm placing before you a copy, also, of Exhibit 1001, which is the patent involved in this inter partes review, Hirakata U.S. Patent 8,068,204. 09:22:26

Are you familiar with that patent?

A Yes.

Q And I'm also placing before you a copy of the declaration that was filed as Exhibit 1007 in this case. 09:22:49

Could you look at that Exhibit 1007 and see if that's the declaration that you signed?

A Yes, it is. 09:23:41

Q Could you please tell me if -- I'd like to know how this declaration was prepared. And so my first question is: Did you do the search for prior art that you applied in this patent -- in this declaration? 09:24:11

A No, I did not.

Q How did you come to cite these particular references?

A I was provided, by the counsel, some prior art references, and I selected the most relevant for 09:24:27

this particular content.

Q Did you begin by reading the patent in question, Hirakata, Exhibit 1001?

A Of course. I read '204, I tried to understand what '204 -- what is the subject matter of '204, what is the objective of '204, what are the specifications and the claims of '204, and then I reviewed the pieces of prior art that I was provided and selected the ones I thought was the most relevant from that pool. 09:24:53 09:25:16

Q And your selection was based on the claims at issue; is that right?

A Correct.

Q How did you prepare for today's deposition?

A I reviewed my declaration, I reviewed the petition for the inter partes review, I reviewed the board decision, I reviewed the initial response of the patent owner, I also reviewed the request for rehearing by the patent owners, the decision of the board on the rehearing request and, of course, I review the '204 patent and the three patents that are cited in my declaration and which were accepted by the board as a basis for these hearings and the patent by Shiba, the patent by Sukegawa and the patent by Watanabe. 09:25:51 09:26:21 09:26:48

I don't remember the exact patent numbers. If you want, I can refer to.

Q No.

A It is referred to in my declaration.

Q That's fine. 09:26:59

And you met with your counsel for four days -- I'm sorry. You met with counsel for petitioner for four days in preparing for these two days of depositions?

A Correct. 09:27:15

Q In those four days did you cover both patents or did you have four days for each patent? Four days for the one and four more days for the other one?

A No, we covered both, and we did not work full time because two of those days were the weekend. 09:27:27

Q Let me start with the Shiba reference, which I think is the one you relied on primarily; is that correct? 09:28:00

A Correct. The Shiba, Sukegawa and Watanabe.

Q Does Shiba have an objective or desire to maximize the display area relative to the outside dimensions of the panel?

A Yes, it does. 09:28:49

Q Can you explain how Shiba goes about achieving that objective, briefly?

A One of the issues in making a panel -- one of the steps in making a panel is the part that assembles and seals the two counter substrates in an area which is referred to as the seal area, and that area occupies -- is all around the display and has a certain width along the transverse direction of the seal that is a distance that a lot of people tried to minimize because the whole seal area is kind of a wasted area. It is needed in order to seal the liquid crystal within, but it doesn't serve any other purpose. 09:29:20 09:29:52

If one tried to make a seal very narrow, there are problems that the seal is not very effective. If you make it very wide, you waste more area for that one. 09:30:15

So the wiring that Shiba is proposing enables the user from a narrower sealant. That's one of the objectives in Sukegawa -- sorry -- in Shiba, and that's one of the approaches that he's taking. 09:30:46

And another approach that he's taking, to reduce the dimensions of the panel.

And here I like to make a comment, since 09:31:10

you were combining the proceedings from yesterday and today, that yesterday I was making a lot of statements about the -- that someone skilled in the art would know that minimizing the waste area and trying to make as much as possible of the display area relative to the size of the glass is very relevant. 09:31:28

As you see here, it was an issue that was well known and a lot of researches attempted to maximize the size of the display relative to the size of the glass that's used to make that display. 09:31:50

So the other -- continuing for Shiba is the other approach that Shiba is introducing is means to provide signals to the display only from two sides and relative to prior art that were providing signals from four sides or three sides, and that would require more bonding area for pads and so on in these other sides. So by having two sides, that's an improvement. 09:32:24

And in order to access the pads, which are away from the areas, from the terminal regions from the pad areas that receive the signals and the power from the outside circuit board, Shiba is proposing a specific wiring that will have benefits of reduced resistance and improved manufacturing yield by 09:32:40 09:33:15

eliminating manufacturing defects, in essence by having a two-layer wiring structure.

And there may be other things. If you want, I can read more to Shiba and give you a bit of a summary. From the top of my head, I can refer to Shiba and give you more detail if I missed something, but -- 09:33:36

Q Let me ask some more specific questions.

Does Shiba aim to reduce the width of the seal region without lowering the strength of adhesion between the two substrates? 09:33:51

A That is correct, by creating a wiring in a specific way that will have more surface contact area with the sealant, one can reduce the width of the sealant, while still maintain the strength of adhesion between the two substrates. 09:34:14

Q And, finally, does Shiba also declare that his or her invention does not increase the number of manufacturing steps?

A That is correct. 09:34:42

Q Let me invite your attention to Figure 3.

And, as I see it, Figure 3 has a lower portion and an upper portion. Does that characterization seem reasonable to you?

A I can follow you. 09:35:19

Q Okay. So what, generally, is the lower portion of Figure 3?

A The lower portion is the external flexible wiring that comes and attaches to the glass, and the two pieces make contact in the terminal regions where you have the pads via anisotropic conducting field. 09:35:38

Q So you referred to two pieces. Is the first piece the lower part and the second piece the upper part? 09:36:35

A The upper part is the glass substrate that contains the display area, the wiring, the seal, the counter substrates.

Of course, not everything is shown at this level of details, but I can refer to the exact Watanabe is calling the elements. 09:36:55

Q I don't need that.

A Okay. It isn't called the array substrate, it's the glass substrate.

Q Okay. So where is the display region of this LCD depicted in Figure 3? 09:37:16

A The display region is within the seal area. The seal area is element 111, 111.

Q Do you mean that the display area is within the region circumscribed by the seal area 111? 09:37:56

A No, I mean it is inside.

111 is two lines. It's run parallel like a band. And within that band, over here, the upper left corner is the start of the display. It is the display surrounded by the 111 band. 09:38:23

Q Yes.

A So it is inside.

It extends beyond the inside line of 111.

Q And relative to what's been marked as X1, X2, X3, X4 and X5, where is the display area? 09:38:41

A X1 is the first signal lines, data signal lines, also referred to as data lines. So X1, X2, X3, X4 is the first data lines of the array. And there may be hundreds of such lines, which it starts from the X1, and then you put one next to each other 09:39:25 at specific interval, which is determined by the spacing between pixels. And depending upon the form of the display and how many lines you have, you have 640 of such lines if it's a VGA, monochrome, 640 times three if it is VGA color, and so on. 09:39:50

Q And so --

A And then these are the data signal lines. And you also have the scanning lines. The scanning lines are orthogonal to the data lines. They start from the opposing side of the display. The 201d is 09:40:20

one of the short sides of the display. The opposing side of that one is at 201c, so the scanning lines start from that side and they propagate orthogonal to the X lines, which are the data lines. And either the first or the last is the one that terminates right past X1. 09:40:57

And the first one -- the first one, probably, it goes up to where that square label 125a.

Q Okay. 09:41:20

A Stops short of that one.

Q Okay. Thank you.

So if you looked at Figure 1, for example, together with Figure 3, it is fair to say that Figure 3 is the bottom left corner of Figure 1 in a blowup view? 09:41:32

A In Figure 1 there is a rectangle drawn called A. So Figure 3 is a magnification of the content within that rectangle labeled A.

Q Good. So the display area is up and to the right of Figure 3, generally speaking, yes? 09:41:53

A Yes. It starts from this corner and propagates --

Q Okay.

A -- up and to the right. 09:42:14

Q Now, in Figure 3 is area 731 a power supply pad? That's that box off to the corner of the sealant region.

Do you see it?

A Yes, I see it. 09:42:34

Q Is that a power supply pad?

A It is the pad that provides the power to the counter substrate. It is referred in column 5, line 51, as the power supply pad 731.

And what it does is it receive a signal 09:43:24 from the common pad 751. And the common pad 751 receives the power or the signal from the external wiring 711.

And then that through wiring, that signal goes to 731, and then through a conductive means, 09:43:55 like an epoxy that contains conductive particles, 731 is making contact to the counter substrate that will be bonded to the substrate that is shown to the glass substrate 201.

The two substrates will be bonded through 09:44:34 the seal, but the seal is not conductive. The seal -- or the epoxy that will be placed on the pad 731 is a conductive one, and that will provide the connection to the ITO layer that it covers the entire surface of the counter glass substrate, which 09:44:55

is the counter electrode for the pixels.

Q Thank you.

Just generally speaking, in Figure 4, just below Figure 3, is the display region to the right and the terminal region to the left? 09:45:43

A In that cross section?

Q In that cross section, yes.

A Correct. The right, the left with respect what -- with respect to the seal, yes.

Q I was talking about left and right with respect to the page that's on, but that's also with respect to the seal. 09:46:07

So to the left of the seal, somewhat to the left of the seal, is a terminal region, correct?

A Outside, correct. 09:46:23

Q All right. That's outside. And to the right of the seal you can call inside, and that's where the display region is?

A Correct. That's where you have a specific gap between the two substrates, and the liquid crystal is contained within. 09:46:34

Q And the pad 731 that you testified about a little while ago is shown in Figure 4 about -- near the bottom about 1 inch from the left side.

Do you see it? 09:46:58

A I see it.

Q And then above that there is a substance or a part 115. Is that the -- what the patent refers to as transfer material? I think you called it an epoxy that's conductive. 09:47:16

A Correct.

Q So that transfers electrical potential to the counter substrate, which is part, it looks like, 501; is that correct? Well, the counter substrate, whatever number it is. 09:47:46

A The whole concept is 500. 501 is the glass substrate. On the counter substrate -- on the counter substrate you have the ITO layer.

Q Okay. Now, going back to Figure 3, just to confirm a few small things, is pad 731 electrically 09:48:31 in common with the line 121 dash what looks like a 1 or an I?

A I think it is a 1.

Q You think. Okay. Yes or no?

MR. GIBSON: Objection; form. 09:48:54

THE WITNESS: What do you mean "electrically in common"? It is formed by the extent -- it is the same metal. It's form is a big rectangle in the pad 731, and then the metal continues and forms that wiring 121. They are all 09:49:16

pre-made by the same material. And that material is the material of the data lines.

BY MR. MANZO:

Q Okay.

A Could be made with other material, but the preferred embodiment, it is from the data lines, it is listed. 09:49:29

Q I'm sorry. You are looking for something?

A Looking at the material that is made, like in column 6, line 25, "In the case where TFTs of bottom gate type are used as switching devices as in the above embodiment, the power supply pads 731 to 738, the common pad 751, the third wiring lines, 121-1 to 121-4, the inter-connecting pad 125a, and 125b the second wiring lines 123-1 to 123-4, and the first wiring line 127 can be formed in the same step of forming the data lines Xi." 09:50:07 09:50:43

So it is the same material. And the mask that is used has a big rectangle where it is labeled 731, it has a narrow wiring line 121, and so on. 09:51:14

So they are not different pieces, they are formed all from the same initial metal layer that was put and covered the entire substrate, at least the remaining metal that's left.

Q Okay. So I think that all I'm trying to 09:51:38

say is that they are electrically in common. They could be part of the same layer, but not be connected, right, because of masking -- strike that. That's unclear.

When a person puts down a layer of metal, it is governed by the mask; is that right? 09:52:05

MR. GIBSON: Objection; form.

THE WITNESS: Well, you put the metal and cover the entire substrate, and then you use a masking step followed by an etching step to the regions of the metal to form the different elements. 09:52:24

Some of those regions, such as the lines X1, X2, X3, X4, they are long continuous lines starting from the pad 761 and continue to the other end of the display and stopping short of the other sealant, of the opposing side of the sealant. 09:52:53

Other regions, such as the ones that I just quoted from the patent, namely, 731, 121, 751, 123, 125 and 127, they are all continuous metals and just say different ways, but all part of one continuing pattern that is connected. 09:53:29

BY MR. MANZO:

Q Fine.

A It's -- there is no any discontinuity.

From 751 you can go to all those regions and still 09:53:52

be on the same metal.

And -- so, for example, if 751 you put like 5 volts in 751, you give it the potential of 5 volts, then all that wiring in that pad will be held at 5 volts. 09:54:30

Q Okay. So if you put 5 volts on 751, there's also going to be 5 volts on 121-1 and 731 and 123-1 and 127 and 125 -- well, I'm not sure about 125a -- strike 125a -- is that correct?

A 125a is also part of it. It is a square piece of metal. 09:54:54

Q Okay.

A From Figure 3. And then there are other elements from Figure 1 that also will be at 5 volts. It will be the 732 -- well, the 732 receives -- but from 751 it will be 731, 735, 736, 737, 738, so it will be multiple pads that will receive that signal. And it continues, also, on the other side. 09:55:08

Q Professor, where is 732 -- sorry?

A You see that in Figure 1. 09:55:43

But I said strike that one because 732 receives a signal from another pad, not the 751.

Q Okay.

A But the one from 751 goes to 731 and then through the wiring 127 goes to 735, -36, -37, -38, 09:55:59

and it continues and gets connected up to 734.

Q Pardon me. Where is 734?

A You can see that in Figure 1.

Q I see.

A It's the lower right corner. 09:56:30

Q Thank you.

A The wiring 727 forms almost like a pi, a Greek pi letter and kind of surrounds the display starting from 751 back.

Q I'm not sure how it resembles the Greek letter pi. 09:57:12

A It is like a P, it is like this, that and then that.

Q Oh, with regard to the -- I -- what you're saying is that looking at Figure 1, which is a plan view, the lines 127, if they start at the bottom left, rise upward and then traverse across to the right and then traverse downward? 09:57:34

A Correct.

Q And that's what the Greek letter pi somewhat looks like? 09:57:52

A Yes.

Q Now, is it correct that lines 127 are not electrically in common with the data line pads shown in Figure 3 as 761, 762, 763 and 764? 09:58:19

MR. GIBSON: Objection; form.

THE WITNESS: You are using -- you introduced new terminology, "electrically in common," which is not -- I'm not familiar with this term. 09:58:40

BY MR. MANZO:

Q All right. Let me --

A Electrically connected or same potential? What do you mean? Touching?

Q Let me ask you a broad, open-ended question, then. 09:58:49

A Okay.

Q Is there a relationship between the power supply pad 731 and the data line pad 761, 2, 3 and 4? 09:59:04

A The common pad 751, that is connected, and, as we said earlier, the 5 volt in 751, it will be 5 volt in 731. That is controlled by the external wiring, which is labeled 821a, which is the first external wiring from the element 711 from the lower part of -- the lower part -- not the Figure 4, say Figure 3, the wirings 821a, that's the wiring that provides the signal to common pad 751. 09:59:32

Q Okay. And to the right of 821a there are further lines? 10:00:00

A Right. Other pads. Each one connected to a data line, and they receive signal from the external wirings, other external wirings. If those external wirings happen to be the same voltage as the 751, then there may be -- one of the data wiring may also be in the same voltage, but that's because the signal is received and happens to be in the same voltage. 10:00:30

So if, for example, they all get 5 volts, 5 volts will appear to all of them. Maybe the 5 volts only go to 751, and 761 get 1 volt, and 762 get 2 volts, 3 volts or 4 volts, they can all be separate, separate potentials, independently determined by the outside circuit. 10:00:44

Q Okay. So it's fair to say that pad 751, 761 through 764 are five independent pads? 10:01:02

A Correct.

Q Now --

A There are four -- as we said, there will be hundreds of these pads. There will be four pads that will have the same voltage as 751, and you will be able to see that in Figure 1. 10:01:32

Q I think you described those --

A Okay.

Q -- a little while ago. 10:01:48

A But all the other pads, they will be independent.

Q Okay. Is the sealant marked as region 113 in Figure 4?

A The sealant material -- 10:02:11

Q I just want to know the part number of the sealant.

A Yeah, 113 is the sealing material.

Q And you mentioned that in your declaration at paragraph 48, I think. 10:02:35

Could you confirm that on page 15?

A Yes. So 113 is the sealant material and 111 is the seal region; in other words, what is the projection or the regions on Figure 3 where the sealant will be applied. 10:03:04

Just clarify, the 111 and 113.

Q Going back to 111, then, in Figure 3, some of the -- well, looking at the reference number 111 -- do you see it?

A Yes, the seal region. 10:03:30

Q And just to the right of the number 111 there are these lines marked in a bracket as 127?

A Correct.

Q Now, some of those are in solid lines and some of those are in broken lines. 10:03:43

Why is that?

A The ones that are in broken lines, they are considered to be under the sealant -- under the sealant. So they will be covered by the sealant material. So, in a way, if the sealant material is opaque, you wouldn't be able to see them. So the artist kind of do them with broken lines to say that they will be there. Even if you look from the top of the glass, you won't be able to see them. If you look from the bottom side of the glass, you will be able to see them. 10:04:03 10:04:17

Q And the unbroken lines?

A And the unbroken lines, the continuous lines, those are the lines outside the sealant.

Q Now, is there anything in Figure 3 that you regard as an external connection line? 10:04:35

A Well, as we discussed, 751, 121, 731, 123, 125 and 127, they are all made by the same metal film, and that metal film is continues.

So that metal that goes all the way out to 751, or starting from 751, and that metal continues and provides a signal to all those elements. Those elements are labeled differently in order to illustrate the purpose of those things, but it's the same metal line which is continuous. So that's 10:05:07 10:05:35

metal, which is all those things are the same potential because all part of the same metal, which is continuous, is the external connection line.

Q Is there anything in Figure 3 that you regard as an auxiliary line within the meaning of the claims of the '204 patent? 10:06:03

A The purpose of the line that the patent labels 127 -- 127, column 6, line 5, it reads, "refers to wiring line 127 is drawn from the interconnect in pad 125a," and so on, and then it says, "as shown in Figure 1, the first wiring line 127 has got a longer segment, shorter side, 201d, to the second longer side, 201b and connected to the power supply pad 735 to 738 through the branch wired line. Then the first wiring line 127 is guided along the first shorter side to 201c to the first longer side 201a." 10:06:55 10:07:25

So the wiring 127, the first wiring 127, runs a very long distance.

And if we look further down column 6 in the line 37, it reads, "The first wiring lines 127 may be formed in the step of forming scanning lines Yj and the data lines Xi, respectively, thereby constituting a two-layer structure. In this case, if the layers are constantly connected to each 10:07:51 10:08:23

other, the wiring defect can be prevented and the manufacturing yield can be improved."

In that section it reads that the 127 is -- it has two layers, and one layer made by the data wiring metal, that's the upper layer, that's the auxiliary line -- sorry -- that's the external connection line that we have identified a moment ago, and the lower metal is low -- lower layer is made by the material of the scanning lines, and that's the auxiliary line. 10:08:46 10:09:04

Q Okay. So is it your testimony that the external connection line and the auxiliary line have the same number in Figure 3?

A They are overlapping one on top of the other, and they occupy the same area. 10:09:36

Now, the auxiliary line is indicated in this wiring element 127. So both auxiliary lines and external connection lines are within the element 127.

Q Okay. Professor, I'd like to spend a moment trying to understand the relationship between Figure 3 and Figure 4. 10:10:09

Do you have an understanding of any such relationship?

A I don't know what you mean. I do 10:10:50

understand what's in Figure 3 and 4 and all the other figures, and Shiba, as I studied as well.

Q Well, what is Figure 4?

A Figure 4 is a cross section along the line that in Figure 3 it shows a-a prime. 10:11:16

Q That's what the patent says, isn't it?

A I believe so.

Q Okay. So if we were to look and slice through this structure at the line a-a prime, we would theoretically see what is shown in Figure 4; 10:11:50 is that right?

A Correct.

Q Professor, I had some problems verifying that because, for example, the pad 731 in Figure 3 is not along that slice or that line from a-a prime, 10:12:24 and yet it's shown in Figure 4.

Do you see that?

A Yeah, I see that. But it is not uncommon for the artist to try to depict essential elements, that occasionally I've seen in other works that the 10:13:08 lines -- typically when you see a cross section is like a slice through one continuous straight line, but I've seen in other that the line can actually be like almost like some arbitrary shaped line in which the elements that will be along that arbitrary 10:13:33

shaped line for the purpose of the teachings are illustrating in the cross section.

That's done in order to save space so the author will not have to draw two or three or more cross sections to illustrate the relative location of the different elements to try to include them in the same figure for illustration purposes. 10:13:57

Q In your experience, don't draftsmen usually indicate that they are doing that on the plan view so you can avoid having to wonder where the cross section is taken? 10:14:25

A Well --

MR. GIBSON: Objection; form.

THE WITNESS: These documents are meant to be read by people with ordinary skill within the art. And the people use them to learn and be educated, and they already have a certain background and a certain experience that thinks that may not be clear to someone who is not skilled in the art, it is clear for them. So you point out some differences in the artwork. I don't think that would be a big issue for someone skilled in the art. 10:14:42 10:15:09

BY MR. MANZO:

Q Okay. Looking at Figure 4, can you trace a signal path from the terminal region into the 10:15:42

display region?

A Well, in this particular cross section, the -- as you point out, it doesn't -- the terminal pads, it doesn't go to the display regions, it provides a connection to the element 731. So it terminates there. 10:16:23

Outside the seal region, it shows the cross section along 751 to 123, and inside the seal region it shows transistors and different elements, everything, the pixel. 10:17:01

Q Now, before you were talking about the person skilled in the art who would understand these drawings.

What would such a person have been or how do you describe such a person as of 1997? 10:17:18

A Well, in general terms, it would be a person who has enough experience to be able to read those documents and be able to understand their meaning and be able to understand the teachings and be able to take the teaching and implement 10:17:43 structures and be able to combine different piece of arts to create new structures that contain elements from different pieces of prior art.

Q Can you describe their education and their experience in terms of degrees and whether they are 10:18:35

a circuit designer or a process design engineer?

A Well, this is an interdisciplinary field, so you have people with different backgrounds coming from different fields. You can have people with a science background, like physics and chemistry, but you can also be from material science or you can be from an engineering field, such as electrical engineering, chemical engineering. 10:19:01

And those people, they have some courses as part of their education, which is relevant to this technology. They also receive further training at the workplace, and we discussed about that yesterday, whether they are process engineers or circuit designers. 10:19:34

I believe after a few years in the field, all these peoples from different background, they will be able to understand these prior art pieces such as Shiba. 10:19:56

Q Does Figure 4 show an external connection line and an auxiliary line? 10:20:36

A No. It shows -- you asked me if it shows an external connection line and an auxiliary line. It shows an external connection line.

Q Which one is the external connection line?

A It is 751. It is connected to 731, which 10:21:12

continually is labeled 751 -- same line, different portion is labeled 121-1 and another portion, same setting, is label 731.

This is only a segment of the line, the metal wiring that is formed starting from 751. We discussed earlier about the other pieces that are formed from the same material, they are continuously -- that go under the seal, like 123 and 127, which are not shown in Figure 4 but are shown in Figure 3. 10:21:58 10:22:26

Someone skilled in the art -- 751 is shown as a single layer in this.

Q Do you see a storage capacitor in Figure 4?

A Yes.

Q Is it formed of these three layers, a electrode Cj, or C subscript j, an insulator 211 and an electrode 251? 10:23:20

A In column 4, line 7, it reads, "The storage capacitor is constituted by the pixel electrode 251 and the storage capacitor lines Cj." 10:24:31

Q Why is a storage capacitor formed or shown in Figure 4?

A Well, the artist, as we discussed earlier, is trying to depict some critical elements outside the sealant and critical elements inside the 10:25:08

sealant. So the critical elements inside the sealant is a pixel structure, and the elements -- and the storage capacitor is one element within the pixel. So the artist try to show how that storage capacitor is formed. 10:25:37

Q What factors would impact the size of the storage capacitor?

A What do you mean by that?

Q Well, for example, does the thickness of insulator 211 impact the size of the storage capacitor? 10:26:07

A The capacitance depends on the thickness of the dielectric, which is in between the two electrodes, it is actually inversely proportional to the thickness of the insulating layer between them. 10:26:31 211 is the gate dielectric and is in between the two electrodes.

So as you increase the thickness, the capacitance will decrease, the storage capacitance will decrease. 10:26:57

Q Professor, if two insulators are stacked one on top of the other, is it technically possible to remove only the upper insulator by etching without causing any damage to the lower insulator?

MR. GIBSON: Objection; form. 10:27:57

THE WITNESS: Is this part of these proceedings?

BY MR. MANZO:

Q I don't think that that's a responsive answer. 10:28:23

A No, I tried to put it within the context whether I missed something here, and I want to say something in Shiba is referring to it, and I want to put in the context of the '413 patent and the prior art that I review and try to give you a response. 10:28:38

I don't recall that something that came out as a part of the '413 and the three patents that we are referring to today and we need to provide deposition -- testimony of those three.

Q Well, with regard to the knowledge of the person ordinarily skilled in the art in 1997, if there are two stacked insulators and you needed to etch through one of them, can it be done without causing damage to the lower of the two insulators? 10:29:01

MR. GIBSON: Objection; form. 10:29:28

THE WITNESS: And can I ask you can you please point out where that question is related to the proceedings to the material that I have been called to testify here so I can put my answer in a context? 10:29:43

But I don't think the material -- that's something I have studied to give you a thorough answer today.

BY MR. MANZO:

Q So are you saying that, technically, you're not aware of that? 10:30:25

MR. GIBSON: Objection; relevance.

THE WITNESS: I'm saying that the question that you are asking is in a subject matter that I have not review and I'm not prepared to give you a response today because I don't think that question deal with any of the material that I have studied. And I have been informed that you can ask anything you wish, but I'm prepared to discuss the prior art that I have in front of me and not to give you answers -- I'll try -- but you asked me something and I asked for guidance so I can place my answer in proper context. But I do not recall this question come, that it was something that I had to deal with. 10:30:44 10:31:05

BY MR. MANZO: 10:31:25

Q Well, you're experienced with etching; is that right?

A Yes.

Q Have you tried to etch stacked insulators and just etch your way to the top level of two 10:31:45

stacked insulators without any over etching of the lower insulator?

MR. GIBSON: Objection; relevance.

THE WITNESS: I have worked with many insulators and different substrates, and I have to review my notes. If you guide me to some specifics, I may be able to give you a response, but this is a very big open-ended question that you are asking. 10:32:12

MR. MANZO: Why don't we take a short recess. 10:32:36

THE VIDEOGRAPHER: We are off the record. The time is 10:32 a.m. on July 2nd, 2013. This is the end of video number 1 of the continuing deposition of Dr. Milt Hatalis.

(Recess.) 10:32:52

(Whereupon Conrad Szuladzinski replaced Scott Slater as the.)

THE VIDEOGRAPHER: This is the continuation of the deposition of Milt Hatalis. My name is Conrad Szuladzinski, and I am the videographer. And we are back on the record at 11:13 a.m. 11:13:38

BY MR. MANZO:

Q Professor, in paragraph 48 of your declaration, which is Exhibit 1007, you referred to wiring lines with a two-layer structure. And you've 11:14:39

referred to the passage, I think, at column 6, earlier this morning about the two layers; is that right?

A Yes.

Let me add, two-layer structure that are overlapping, but there is an insulating layer in between and which is partially connected. 11:15:06

Q Can you describe how the two layers are created and form the line that you're talking about, please, and include -- if you would, explain why you conclude that there is insulation there. 11:15:35

A Okay. Column 6, line 36, is our section where it reads, "Moreover, the first wiring lines 127 may be formed in the step of forming the scanning lines Yj, and the data lines Xi." 11:16:22

So if we go to different sections of the patent trying to understand what are those two layers are formed and what occurs in between them, you go to column 4 at line 1, it reads, "Each scanning line Yj is used as the gate dielectric of a TFT 221." 11:17:07

Then you go further down in column 4, line 12, it says, "As shown in Figure 4, this scanning lining Yj and the storage capacitor line Cj are formed on the glass substrate 201. The scanning 11:17:31

line Yj itself is used as the gate dielectric of the TFT 121. A gate dielectric 211, having a laminated structure of silicon oxide and silicon nitride, is formed on the gate dielectric Yj."

So in these sections it talks about right on top of the glass substrate, you are forming the scanning lines so you leave portions of the film that was deposited onto the glass substrate to form the different wirings and the scanning lines, and capacity lines is a set of lines, and the portion of the wiring on 127, as we read earlier, is formed at that time. And this is the lower layer. 11:17:55 11:18:19

Q Made of?

A The material which is used to make this scanning lines. And the sentence at column 4, line 15, which reads, "Gate dielectric having a laminated structure of silicon oxide and silicon nitride is formed the gate dielectric." 11:18:42

It shows that after the scanning line is put down and is patterned to form different elements that remain, then the dielectric is formed and the dielectric is deposited by, typically, some sort of a CPT technique that it covers the entire substrate. 11:19:02

And then the -- then, based on the sections of column 6, line 31 that reads, "If the layers are 11:19:36

proximately connected to each other" -- that section means that after the gate dielectric has been formed, some step is occurring to open contact holes on top of the gate material, the scanning line material. And then we put down the material of the data lines. 11:20:09

And then that material has been patterned to form the data lines and the upper layer of the wiring 127.

So what you have is the lower layers, made of the scanning line material, you have the gate dielectric 211 in between, you have openings in the gate dielectric, and then you put down the data line material and you pattern that one and it forms the upper layer. 11:20:31 11:20:58

Q In creating the gate dielectric that you read about, the gate dielectric 211, and the specification at column 4 says, at line 16, "silicon oxide and silicon nitride," is there control over where those regions -- where those dielectrics end up? 11:21:29

MR. GIBSON: Objection; form.

THE WITNESS: Well, what do you mean by "control"?

BY MR. MANZO: 11:21:37

Q Is there a masking step or patterning?

A During the deposition or after the deposition?

Q Yes.

MR. GIBSON: Objection; form. 11:21:51

THE WITNESS: These are two different things. During deposition, there is no masking step. Deposition is a high-temperature step so the material goes everywhere and covers the entire substrate. It is a masking step and an etching step 11:22:07 that will follow the deposition process.

And if one wants to create the -- what is referred to in column 6, the -- if one is to enable the layers to be partially connected, so someone skilled in the art says if the layers are constantly 11:22:30 connected, if so, if someone wants to build a double-layer structure, then you have -- you need to create an opening in the gate dielectric to -- at least one opening to enable the partial connection.

BY MR. MANZO: 11:22:49

Q How do you know that the dielectric is not etched away from the lower layer? What is the teaching?

A What do you mean "lower layer"?

Q From the lower layer of lines 127. 11:23:06

A Well, you have a masking step, right? And the masking step protects the great majority of the surface area where the dielectric layer will remain and only leaves exposed the portions of the area where you want that oxide and nitride film to be removed so it will expose the underlying layer of 127 so that the upper layer of 127 will come down the hole and touch the lower layer. And, by doing that, will create the partial connection that's referred to in column 6. 11:23:32 11:24:02

In that etching process you need to remove the entire gate dielectric, so you need to remove both the silicon oxide and the silicon nitride so the lower metal layer that were made by the scanning line metal is exposed. So then the upper layer metal when it is deposited, it will touch it, it will make direct contact with it. 11:24:23

Q Are you -- forgive me, Professor, but now I'm even more confused.

You put down the scanning line layer and then you define lines? 11:24:53

A Correct.

Q And then you put down nitride and oxide as dielectrics, and then you etch, correct?

A Then you do a photo step and you pattern 11:25:12

the regions that you want to etch.

Q Okay.

A Define the regions that you want to etch.

Q Now, does this reference, Exhibit 1003, tell you whether you want to etch or not -- whether you want to mask or not mask the nitride and oxide over line 127? 11:25:26

A Well, it refers to a means to make a partial connection. That means the upper layer is touching some points, but not in all points, of the underlying layer. 11:25:52

Q Okay. Is there any other support for that, other than the word "partial" or "partially"?

A Well, someone skilled in the art, as we were discussing yesterday, will know if there are two layers and there is an insulating layer in between. We spent quite a bit of time yesterday to discuss that connection is done, someone skilled in the art will know that you have two layers, two metal layers and an insulating layer in between, like an insulator has been sandwiched by the two metal layers, then you open contact holes; in other words, depicted in the prior art. 11:26:17 11:26:34

Q But --

A That was something was well known in the 11:26:57

art.

Q Well, Professor, how do we know that, according to this patent, the dielectric should be left on top of the first formed part of lines 127 and not stripped away during the etching step? 11:27:16

There are two choices. Let me pause. Aren't there two choices, you can put the dielectric down and either leave it there or you can take it away, right?

And you've chosen one way, and I'm saying why is it that way instead of the other way? 11:27:40

A I mean, what do you mean by leave it there or take it away?

Q Okay. So the question is, you're citing this paragraph in the middle of column 6 to say that there is a two-layer structure, two conductors? 11:27:54

A Right, separated by an insulating layer, because in the sequence there is that layer that comes in between them. There is a specific order with which the layers are laid down. 11:28:08

Q Okay. And there will be insulator on top of the bottom layer --

A Correct.

Q -- during the process of forming this?

Now, you advise that there is also a 11:28:23

masking and etching step. And it seems to me that you are presuming that these lines 127 will be masked so that the nitride and oxide will remain there, or so that you'll just mask and etch contact holes instead of striping them away completely. 11:28:44

And my question to you is, where does that come from out of this reference?

MR. GIBSON: Objection; form.

THE WITNESS: What do you mean by striping completely? 11:29:03

BY MR. MANZO:

Q Well, you said that --

A There's no masking step?

Q Well, you said that there is a masking step. 11:29:11

A Right.

Q And you leave -- you put a mask over the parts you want to remain before you etch. And then you etch, and then you remove the mask and you have, still intact, the parts that you wanted to have 11:29:22 remaining; is that correct?

A I tried to visualize a structure that -- or the steps that need to occur to create what the inventor here is trying to teach. And the inventor is trying to teach a structure in which the two 11:29:42

layers are partially connected to each other.

The inventor does not teach that you form 127 where the two layers are in direct contact and overlapping over the entire length of the line. So I'm trying to see how one will create a structure which are constantly connected. 11:30:07

If I understand your reasoning, you tried to somehow create both the partial connection and, at the same time, remove the entire dielectric. And if you remove the dielectric, then the lines will not be constantly connected. 11:30:29

Q How will they be connected, hypothetically?

A Well, I'm trying to understand your structure. You say you remove the gate dielectric completely. 11:30:46

So in your response that I studied it was a drawing where the two metals were overlapping a hundred percent over that distance of the drawing that you had indicated there, and that drawing does not show that the layers are constantly connected. 11:31:08 They show that they are connected over the entire length of the line.

I'm trying to understand how you can remove the entire dielectric and still be able to get the partial connection. 11:31:27

Q All right. So I understand your answer to mean that if you remove the entire dielectric, you would not have partial connection, which the patent refers to, the Shiba patent refers to at column 6, lines 39 or 40, and, instead, you would have a complete full connection between the two conductive layers of lines 127; is that right? 11:31:49

MR. GIBSON: Objection; form.

THE WITNESS: Well, you start discussing another hypothetical way of making it, and I'm trying to understand your hypothetical way, and I was asking you questions. 11:32:37

And now you're telling me I give you answers, I was meaning mostly within the context of a question that was asking you, what do you mean by removing the dielectric and how that removal will then satisfy the partial connection. 11:32:57

So I'm still trying to understand your -- what is the structures you are proposing is an alternative to the structures that I have proposed and which was well known in the art of how to connect two layers separated by an insulating layer, and the connection typically involves formation of contact holes and establishing a contact where the metal -- the upper layer will go down the hole and 11:33:18 11:33:44

touch the lower metal.

BY MR. MANZO:

Q Well, thank you for your explanation, but your explanation presumes that there is insulation between the two layers. And the part of the Shiba reference that you've cited for that is not in this discussion in the middle of column 6, lines 36 to 42, it is somewhere else, and it is talking about other parts of the structure. 11:34:05

And since there is a masking and etching step, you are presuming that the masking and etching step is such that as to leave the insulator on top of 17 between the two layers, and I'm suggesting that maybe it doesn't work that way. 11:34:30

And all I'm asking you is what is the support for you saying that there is insulation between those two conductive layers? Because I don't see it between lines 36 or -7 and 42. 11:34:50

A You make a long statement, so let me start from the first aspect or first topic of your statement. And you state, "Your explanation presumes that there is insulation between the two layers," so let's focus just on that part. 11:35:14

Q Okay.

A I read sections in -- from Shiba that list 11:35:34

the order with which the layers are put down, and I said that following those steps, it will lead to an insulating layer between the wiring formed from the scanning line material and any wiring formed between the data line material. And you seem to even question that par. 11:36:07

Why you say presume? You're reading differently in the specifications that I do? You're questioning even the presence of the dielectric. When the dielectric goes down, it goes everywhere. It's not that it's put selectively in some regions, it is not put putting everywhere. So the dielectric is everywhere, on top of anything that is formed from the scanning line material. 11:36:28

Q I understand that. 11:36:52

Now, according to what I think you said, there will be a masking and etching step --

A Okay.

Q -- is that right?

A Yeah, so we agree that on top of the scanning line material there is dielectric. 11:37:06

And I think we are agreeing that now there will be a masking step and an etching step.

Are we on the same page, wavelengths?

Q Let's say I follow you. And my question is 11:37:24

really this, now we're getting to the heart of the question --

A Okay.

Q -- the question is, where does the mask go?

I appreciate that there is masking. And here's my point. If I want to mask over there someplace to my left, it doesn't mean that I'm also going to mask over here, someplace to my right. 11:37:38

And -- can we agree with that?

MR. GIBSON: Objection; form. 11:37:57

THE WITNESS: Masking step means that you leave what's known as the photoresist layer, which is an organic material that is photosensitive and which is patterned by exposure and followed by a developing step. So through that whole process, part of the organic material, the photoresist, remains and protects anything which is underlying it. 11:38:17

And the region that did not contain the photoresist, that will be exposed, whether it be the chemical -- whether it be wet chemical means or dry chemical means -- those regions that will not be protected by the photoresist will be exposed to the etching. 11:38:33

BY MR. MANZO: 11:38:47

Q Good. Now, what part of Shiba tells you that photoresist should cover the dielectric on top of the scan line material being used to make the lower layer of lines 127?

A Well, you need to create a connection that will -- at the end will be a partial connection. That 127 -- the lower layer of 127 will be partially connected to the upper layer of 127; that in the two regions where the two layers overlap, the connection will be a partial one. 11:39:18 11:39:39

Isn't that what is reading on column 6, line 40? "The layers are partially connected to each other."

Q Okay. So you are relying on the word "partially"? 11:39:58

A I'm relying on the word "partially," and also relying on whatever we talk yesterday from, say, Sukegawa, which was another piece of prior art which also been used in these proceedings to show that someone skilled in the art will know that you have two layers separated by dielectric and you want to establish a connection between the two layers, you -- the means to do so is to open contact holes. 11:40:12

And when doing so, you establish two parallel lines that are separated by a dielectric. 11:40:39

Every now and then the two lines are attaching each other, so the two lines have the same potential, they form a lower resistance line than if you just have one or the two. And Shiba says that, furthermore, you also gain additional advantage, if you say that one of the layers has a wiring defect, let's say there is a particle that it creates an opening, creates a discontinuity in that portion, the other layer, it is at a different level, it will continue carrying the signal and will bypass the defect portion. 11:41:02 11:41:24

Q May I ask you also about other possibilities?

Does the passage -- the paragraph at column 6, beginning at line 35 -- sorry -- 37 that you've cited, the moreover paragraph -- 11:41:46

A Yes.

Q -- is it possible that that means that there are lines 127 formed of two different layers and that they are side by side, running in parallel, except occasionally crossing over one another? 11:42:02

MR. GIBSON: Objection; form.

THE WITNESS: Well, if we look at the Figure 3, I don't think your statement is supported by the drawings in Figure 3. 11:42:42

We see that all the lines of 127 originate from the pad 125a, I think 125a is referred to -- pad 125 is referred to as inter-connecting pad.

And at column 6 it reads, line 5, "A first wiring line 127 is drawn from the inter-connecting pad 125a." 11:43:28

And we discussed earlier that some of those lines are in dotted lines and some of the lines are continuous lines. So 127, as you pointed out, it refers to those lines as -- with an element which characterizes 127, that wiring is characterized by one number, 127. 11:43:50

And the process that we read on column 6, line 127, the moreover passage, it says that 127 can be made as a two-layer lines where the two layers will be partially connected. 11:44:15

I cannot see any support in the drawing or in the package to say that some lines are made with one material and some other lines made with another material. 11:44:36

BY MR. MANZO:

Q When is a --

A Go ahead.

Q May I ask a question?

A Yes. Go ahead. 11:44:49

Q When is the pixel electrode 251 made in this sequence?

A Whatever is formed after the formation of the gate dielectric, because we have information of the storage capacitor element, which was described, and I read that section earlier, and we have that Figure 4 -- if you are referring to the -- to other layers, can you be a little bit more specific as to what layers you're referring to? 11:45:55

My answer is it is after the gate dielectric. 11:46:34

Q Can you --

A After the gate dielectric, it's not quite clear.

Q Can you tell whether it's before or after the lower layer of 127 is established? 11:46:49

A It definitely is after the lower level of 127, because we see, in Figure 4, the lower level of 127 being -- which is made with the same material and the scanning lines Yj, which are already laid down, above that layer, the scanning line, you have the gate dielectric element 211. And Figure 4 shows the pixel electrode to be above the 211. 11:47:18

So, clearly, it is made after the lower level of 127 has already been formed. 11:47:44

Q Can you tell whether it's before or after the second level of 127 is formed?

A I cannot find any passage in the specifications in the text to list the order. And if you do have such passages, please point it out to me so I will not be wasting your time. 11:49:15

Q I'll ask my colleagues to jump into that --

A Sure.

Q -- if there is a citation in Shiba that they are aware of. I don't think that they are, but we'll see. 11:49:34

Meanwhile --

A While your colleague is looking for that, if I might make a comment in your previous question?

Q Yes. Which previous question? 11:50:04

A You, hypothetically, discussed that the wirings can be formed as separate lines that run in parallel, and each line may be formed in different layers; is that what --

Q That is a hypothesis. 11:50:19

A Hypothesis.

And I said the record does not support that.

Q Okay.

A And I want to point out another piece of 11:50:28

evidence in the record that does not support it.

Q Please.

A Sure. So if we look at Figure 6, it is one we have not referred to so far.

Q Yes, Figure 6. 11:50:43

A In Figure 6 you see on the right-hand side a set of parallel lines which are grouped as a bracket that says "127."

Q I see several side-by-side lines 127.

A Right. And some of them are under the 11:51:08 sealant and some are inside of the sealant, to the left of the sealant.

And those lines are made -- a single-layer line made from the data line material, because those lines are above the insulating layer 211. And they 11:51:31 are all grouped together.

If you were to have a structure where some of the lines will be made by the data line material and some of the structures will be made from the scan line material, then the mask step, it will have 11:51:54 some data line -- lines and it will be -- but not all of them.

So if we count the lines of 1 to the 7 in Figure 3, and if we count the lines in Figure 6, I think they are the same. 11:52:28

So it shows that as many lines as you have in the planar section view, you have in the cross-sectional view, which means that the masking step for when you pattern the data line material, it includes all lines. 11:52:55

And, likewise, if you pattern the scanning line material, you pattern all lines, so then the wiring 127, as shown in Figure 3 and in Figure 6, they all constitute one -- cannot be referred with one numeral, 127. 11:53:15

Q Okay. So in Figure 6 you pointed out that all the lines 127 sit on top of the gate dielectric or the insulator 211; is that right?

A That is what is shown.

Q Okay. And you don't see a lower layer there, do you, of conductor 127? 11:53:39

MR. GIBSON: Objection; form.

THE WITNESS: Well, Shiba talks about multiple embodiments and, particularly, this line 127, it says -- line 30 -- column 6, line 31, "the first wiring line 127 can be formed in the same step for forming the data lines Xi." 11:54:04

So that particular embodiment in Figure 6 depicts the embodiment that is made with first -- with the material of the data lines. 11:54:49

But further down in column 6, in line 34 it says that, "further, depending on the kind of TFTs, the aforementioned wiring lines can be formed in the same step performing the scanning lines Yj." That's another embodiment. 11:55:16

And continuing the same column 6, line 37, we'll go into the passage that reads, "Moreover, the first wiring lines 127 may be formed in the step of forming the scanning lines and the data lines."

So someone skilled in the art will see 11:55:36 there are three different embodiments that are disclosed by Shiba that you can make them with the scan line material, the data line material or as a two-layer structure that you use both materials.

BY MR. MANZO: 11:55:49

Q The wirings 127 are part of the same layer or layers as 125a, I think you testified, and those -- that connects to lines 123-1 in Figure 3? And those, I think you said, are also a part of the same layer as 751 and 731 and 121-1. 11:56:59

Do you recall that testimony?

A Well, I read you from Shiba. This is what Shiba is teaching --

Q Okay.

A -- that all these elements are made from 11:57:22

the same metal layer.

Q So pad 751 will be made at the same time in the same way as what you've described; is that correct?

MR. GIBSON: Objection; form. 11:57:34

BY MR. MANZO:

Q Or put it a different way, would pad 751 be made differently?

A Well, the pad is -- we refer to the pad as a region. And in that region, like in 127 region, 11:57:56 you may have one layer or multiple layers; for example, we see 127 have multiple layers.

Now, the 751 will include, as a minimum, the material made by the data lines as shown here in the preferred embodiment of Shiba. 11:58:31

Q Are you referring to a figure there or -- when you say "here," what do you mean?

A I'm looking at the passage that we read earlier.

Q Okay. The column 6 "Moreover" passage? 11:58:48

A No. A little bit above that one in column 6, line 27 reads, "The power supply pads 731 to 738, the common pad 751, the third wiring lines 121-1 to 121-4, the inter-connecting pad 125a, and 125b the second wiring lines 123-1 to 123-4, and the first 11:59:26

wiring line 127 can be formed in the same step of forming the data lines Xi."

So all those regions are formed in the same step as forming the data lines.

Now, the "moreover" passage below in the same column 6, it shows that the 127 can be made as a two-layer structure. 11:59:47

So the thing in Shiba is that all these regions are made from the data line materials, that some regions, some elements, can you made as a two-layer structure. 12:00:19

Q And in the paragraph from which you were reading in column 6, do you see a reference at line 37 to "not increasing the number of manufacturing steps"? 12:01:11

A I see that.

Q Is that important, in general, to semiconductor manufacturing?

A Do not increase the number of manufacturing steps keeps cost down. 12:01:29

Q So more manufacturing steps means more cost; is that right?

MR. GIBSON: Objection; form.

THE WITNESS: In general, unless your additional manufacturing steps improve yield or 12:01:48

improve performance, and they may be worth the additional thing because you may make a better product which you sell it at the premium, so it doesn't mean that you -- ideally, if you can get advantages in yield and in performance without 12:02:06
increasing the manufacturing steps, you get the best of both worlds.

So, for example, the wiring structure 127 being a double-layer structure, it reduces the defects and also increases the resistance -- sorry, 12:02:51
decreases the resistance. Excuse me. Decreases the resistance.

Shiba teaches giving the signal to the counter electrode is very critical, and those points are looked at very -- at distances far away from the 12:03:20
terminal parts.

So having a wiring that will distribute the signal to the counter electrode in such a way that it will be able to modulate the potential of the counter electrode fast is essential for 12:03:40
high-performance displays.

And he lists examples of different driving things that can be implemented because the wiring structure that he has is a low-resistance structure.

BY MR. MANZO: 12:04:05

Q Just to be clear, does this two-layer structure for wiring lines, or line 127, according to Shiba, result in additional manufacturing steps or not?

A It says, "If the layers are partially connected to each other, the wiring defect can be prevented and the manufacturing yield can be improved" -- are you referring to that part? 12:04:19

Q No.

A "The structure of the present invention, therefore, does not increase the number of manufacturing steps"? 12:04:40

Q That's the part.

That's at column 6, line 32, approximately.

A I don't believe it increases the manufacturing steps. 12:05:03

Do you have evidence that it does?

Q I just wanted to see if you have that understanding, Professor.

A It is my understanding, based on the teaching of Shiba, the drawings and the specifications and what I thought, was someone skilled in the art will also understood at the time of the invention that the double-layer structure can be implemented without increasing complexity, 12:05:19 12:05:36

without adding additional manufacturing stems.

I do not see evidence in the record that shows the opposite will be true.

Q Very well.

A little while ago you referred to Figure 6. 12:07:01

A Yes.

Q Does Figure 6 show that the protective overcoat 241 is above the lines 127?

A This is what is depicted in Figure 6. And 241, column 4, line 29, it specify what it is and, quote, protective overcoat 241 made of silicon nitride is arranged in the TFT 221 and around the pixel electrode 251. 12:07:27

And that's the second insulating film. 211 is the first insulating film in the sequence of fabricating this structure. 12:08:23

Q Professor, could you turn to paragraph 69 of your declaration.

Does paragraph 69 indicate that a person of ordinary skill would modify Shiba in some way? 12:09:30

A The paragraph 61 says the person with ordinary person with skill in the art can modify Shiba to form pads that will include a transparent conducting film, such as indium tin oxide, because 12:10:39

that material is well known to resist oxidation and, thus, will result in reliable connection.

Two-layer structure has already been taught by Shiba --

Q Yes. Go ahead. 12:11:10

A -- within the context of forming the wiring lines 127.

So two-layer structures have been shown in some portions of display to be advantageous. Extending the teaching of Shiba, one can view the 12:11:34 pad 751 as a two-layer pad and use different layers to gain the advantages of improved reliability.

Q I just want to try to understand that better. Does the pad 751 have already the two layers formed from the scan line material used to 12:12:16 make the lines Y and the data line material used to make the lines X? And are you now changing one of those or putting something on top of that?

MR. GIBSON: Objection; form.

THE WITNESS: Well, Shiba is teaching that 12:12:39 751 is a single layer and that element 127 is a double layer.

Shiba does not say that the 751 has a lower layer made of the scanning line and an upper layer made of the data lines. That's something that 12:13:06

someone skilled in the art can implement based on the teaching, but Shiba does not disclose that part.

BY MR. MANZO:

Q Okay. So how would you form the two-layer pad structure, according to paragraph 69 of your declaration? How would a person of ordinary skill in the art do that? 12:13:26

A Someone ordinarily skilled in the art will have a two-layer structure in 751 where the lower layer is made -- still is made with the data line material, but the upper layer is made by the indium tin oxide layer. 12:13:54

Q Now, would there be dielectric on top of the data line material?

A Yes, there is this dielectric of 241, I believe -- yes, 241. So there will be openings in that layer 241. So the pad -- so the indium tin oxide can make a contact to the metal layer or, as we discussed several times, there is the data line material and then there is the insulating layer 241 and there is the indium tin oxide layer. So you can put the 751 down, you put the 241 down, you have openings, and then you put the ITO layer. 12:14:15 12:15:13

Alternatively, you -- so that's one way to make the structure. 12:15:44

Q Would this require an additional step of adding indium tin oxide at that location on pad 751?

A There is already indium tin oxide used as the pixel electrodes.

Q Are you saying no additional step would be needed? 12:16:12

A You asked me earlier about the order of the pixel electrode, and I did not find evidence in the specifications, and I asked for your help to point me in that direction, at least where the ITO is relevant to- -- to the data line material. 12:16:40

There is a layer- -- there is a pixel electrode layer and there is openings in 241 that are created and there is a data line material. And so you have all the steps there in making the structure. 12:17:11

Q I don't think that answers my question.

Are you saying that this modification to Shiba to include ITO on top of the pad 751 can be done without adding additional steps? 12:17:53

A Someone skilled in the art will conclude that those steps can be made without adding steps.

Shiba is not clear how the pixel electrode layer -- when the pixel electrode layer is formed. So depending upon where the pixel electrode is 12:18:22

formed, you don't even -- you change nothing in the process, or depending on where the pixel electrode layer is formed, you change the ordering with some of the -- the order with which some of the steps are formed. But you not add in additional manufacturing steps, you just simply change the order. 12:18:40

And I did not see evidence in the specification. I asked for your help, and I did not see whether you have a clear answer where is the pixel electrode base in the teaching of Shiba in the specifications. 12:18:58

Q Just so I understand your testimony of the declaration, in paragraph 48, you said that the wiring lines 127 can include a two-layer structure of an auxiliary bottom line that's conductive and you've testified that there would be dielectric on top of it with openings, and then an upper conductive layer formed by the data line material that is partially connected through these openings to the scan line material forming the lines 127. 12:20:35 12:21:01

That's what I understand from your testimony so far.

Is that correct -- is that understanding correct?

A Well, the auxiliary lines at the bottom will be made by the scan line material. They will 12:21:54

be insulating layer on top of that with openings.

In the second upper conductive layer they will form the external connection lines that will be made by the data line material.

Q Okay. So that's your testimony. And I think that -- 12:22:22

A This is what I described in paragraph 48.

Q Okay. And I think I understand your testimony.

And then I asked you here a little while ago whether that structure also applies to the pad 751, and you indicated, I thought, that it does not, and you referred to the bit in column 6, I think, where the patent says that the pad is made of the same material in the data line material X; is that correct? 12:22:32 12:23:03

A Well, paragraph 48, and the portions we discussed earlier from the specifications, refers to wiring lines 127 being double-layer lines. So within that context there are two points I want to make. One is that the patent is saying that it is double-layer structures, consisting of the scan line material and data line materials applies to 127, at least this is what is disclosed in the preferred embodiment of Shiba. 12:23:33 12:23:59

And the other elements, 751, 121, 125, are referred to as a single-layer structure.

The paragraph 38 and the context in the teaching of Shiba, there is something -- there is a general teaching that emerges out of the construction of 127. 12:24:26

And the general teaching of the construction of 127 is that two-layer structures are advantages. If you can form them without adding steps and if you gain advantages, that will improve the manufacturing yield, will reduce defects. 12:24:43

So there is a specific teaching for a specific wiring, but there is also a general teaching that someone skilled in the art will see that can apply to maybe other structures. 12:25:05

The general teaching is that the structure can be made, in general, with two layers. And the specific teaching for making the wiring 127 applies to wiring lines 127.

One can do that exact sequence of layers to other parts or it can change and use different layers to make other parts and use other materials which already used in the manufacturing process and mix and match the layers in order to gain advantages. 12:25:29 12:25:53

After all, there are three layers that are reported in Shiba, the three conductive layers. There is the conductive layer made of the scanning line material, there is the conductive layer made of the data line material and there is a conductive 12:26:12
layer made with the transparent indium tin oxide.

So you can mix and match which layers you want to use to make a two-layer structure in order to gain some advantages in that particular region that you want to implement that two-layer structure. 12:26:31

In forming a long wiring line, just as in 127, to provide signals to these counter electrode pads, which are distributed along the periphery, far away from the common pad 751, it makes sense, as Shiba specifically disclosed, that that wiring has 12:26:55
been made with the data line and the scanning line materials. But the general teaching of making two-layer structure is there.

So in the common pad region, someone skilled in the art will see that you can maintain 12:27:17
the data line material from Shiba and introduce the pixel electrode above it in order to gain advantages in corrosion protection.

Q Would a person ordinarily skilled in the art want to consider and weigh the disadvantages, if 12:28:25

there are any, of a process sequence in which the indium tin oxide is added on top of pad 751 after the formation of the protective overcoat 241?

MR. GIBSON: Objection; form.

THE WITNESS: And what are these disadvantages? 12:29:29

BY MR. MANZO:

Q Well, if there are any, would they have to be weighed?

MR. GIBSON: Objection; form. 12:29:52

THE WITNESS: I did not see any disadvantages. If you have see something, if you have evidence of -- that there is a disadvantage, can you elaborate so I can answer your question?

BY MR. MANZO: 12:30:02

Q Well, Professor, I'm not the expert here testifying. You're the expert at this, and I'm just trying to understand and explore the testimony you've given and the consequences of it.

So if I ask some dumb questions, I'll hope that you'll forgive my ignorance. Maybe my questions are not sensible and maybe they are, but together we are trying to arrive at the truth, so let me press on. 12:31:03

A Let me comment that, first, your questions 12:31:44

are not, what you say, dumb questions, I do not find your questions to be dumb. And I agree with you that we need to derive to the truth of the matter and I understand that you may also have experts that help you in understanding those structures that may have more knowledge and skill than you, as an attorney, may have on the subject matter. So I think some of your questions may be guided by information you receive by the experts, so I am -- in some of my questions towards you, I'm looking for things that you or your colleagues or your experts see and read in the specifications so then I can respond and provide comments to those evidence that they maybe see. 12:32:10 12:32:34

And it was my testimony earlier that I do not see any disadvantages. If you have any information for such disadvantages that you have formulated yourself or your colleagues or your experts, please point it out to me so we can discuss them and then we'll derive to the truth, as you said. 12:32:57 12:33:13

Q Well, let me try.

Looking at Figure 4 of Shiba, we have a gate dielectric layer 211 that you've pointed out, right? 12:33:49

A Yes.

Q Now, I see number 211 at the right-hand side of Figure 4. Let me just ask one question for now before we break. Can you tell how far to the left in Figure 4 that layer 211 extends? 12:35:26

A From the drawing?

Q Yes. Or, if you want to consult any other part of the specification, that's fine also.

A Well, if you have evidence that will help me, we'll save time. If you want to direct me to something, to some point you would like to make -- 12:36:00

Q Well, frankly, you know, I almost need a microscope or magnifying glass to tell this.

I just wonder if, in your expertise, maybe you know the answer and can help me with that. 12:36:18

A Well, Figure 4 is kind of crowded picture, and 211 is labeled on the right. And you asked me how far it extends to the left, if I understand your question?

Q Right. Yes. 12:36:41

A In my analysis I use Figure 6 where it is a bit more clear where 211 is on -- with respect to the sealant. I presume you would like to find out where 211 is relevant to the sealant, because the sealant is towards the left. Is that what you're 12:37:13

trying to --

Q Yes.

A And I can see it clearly in Figure 6. And I would assume that apply to the other side.

Q In Figure 6, just to be clear, the display region is on the left-hand side of Figure 6 and the terminal portion is on the right-hand side? Do I have that correct? 12:37:32

A Figure 6 is one of those sides that does not have a terminal portion. 12:37:48

Q Oh.

A As you see from Figure 1, the terminal portions are on two sides, and there are two other sides that did not have terminal portions. I believe that applies to the side that does not have a terminal portion. 12:38:02

Q Okay. So to rephrase, in Figure 6 does the left-hand side of the sealant represent the display -- part of the display area and -- let's just end the question there. 12:38:26

Perhaps that's a little unartful. Let me rephrase it.

In Figure 6, is the display area generally to the left of the sealant 113?

A By "display area," I presume you are 12:38:42

referring to the array where you have the pixel and the electrodes, and the answer is, yes, it is to the left of 113, and you can see where the two substrates, 200 and 500, because the sealant 113 that contains and seals the liquid crystal that is the -- within the display area. 12:39:06

Q Okay. So based on that, you've indicated that Figure 6 shows the dielectric 211 extending from the array area of the display area beyond the sealant to a region outside the sealant, yes? 12:39:43

A That's correct.

Q And would that tell you that in Figure 4 of the same orientation or configuration for that region 211, dielectric 211 persists or exists?

A I think it is shown in Figure 4. 12:40:15

Q I'm sorry. Did you say, "I think it is shown in Figure 4" or did you say "I think it is so in Figure 4"?

A "It is shown."

Q Okay. 12:40:58

A Earlier in this questioning you said that you had trouble seeing 211 to the left, and then I refer you to the Figure 6, which I said would equally apply to Figure 4. And then we agree that it is shown clearly in Figure 6. And I'm looking at 12:41:16

Figure 4. Without the help of magnifying lens, I believe it is shown that it is there and extends all the way out to the edge.

Q Okay. Well --

A And it is below element 751. 12:41:40

MR. MANZO: Maybe we can stop here for lunch.

THE VIDEOGRAPHER: This is the end of tape 1. We are off the record at 12:41 p.m.

(Recess.) 01:29:32

THE VIDEOGRAPHER: This is the beginning of tape 2. We are back on the record at 1:30 p.m.

BY MR. MANZO:

Q Professor, did you discuss your testimony with anybody over the lunch hour? 01:30:21

A No.

Q Okay. We were talking, before the recess, about including a transparent conductive film, such as ITO, for the top layer of pad 751.

Do you remember that? 01:31:00

A Yes.

Q And I believe you rely on Sukegawa for that motivation; is that correct?

A Yes.

Q I just want to make clear that we're in 01:31:17

agreement that Shiba does not refer to using a transparent conductive layer for this specific purpose; is that right?

A Shiba is teaching wirings that can be made or structures that can be made as two layers, where each layer has been formed from a different material. The particular embodiment discussed in Shiba in the common pad region, 751, it depicts only a single layer, which is made of the material of the data lines. 01:31:42 01:32:15

Q Are the data lines and the scanning lines made of different materials or are they the same material?

A Made at two different times. It is two different deposition process, and they are separated by a dielectric layer 211, as we discussed earlier. 01:32:38

I do not recall, and please help me if you recall, where the materials of the data lines and scanning lines are referred explicitly what they are in Shiba. 01:33:43

Q Maybe I can rephrase, whether you recall any indication in the Shiba patent of whether the data lines and the scanning lines are different in material.

A My recollection and a brief scan, they are 01:35:47

referring them as scanning line and a data line, but do not go into detail what material constitutes each line.

If you are asking me in general --

Q Let me ask you in general. 01:36:04

A -- what material are used, they can be the same or they can be different.

For example, in Sukegawa that I'm using there is specific mentioning of what material they can be used, and they also provide a list of 01:36:36 additional materials of -- and the list includes chromium, molybdenum, aluminum, tantalum, to name a few.

Q I understand your answer, but focusing specifically on Shiba, then you're not aware of any 01:37:21 specific teaching in Shiba, are you, of using different materials for the X lines and the Y lines?

A My recollection, and I cannot find -- I cannot find any mentioning right now what are the materials for the scanning lines and data lines. 01:37:48

I see a reference to another component, the light shielded matrix layer, which is used to make -- which is made from chromium on the other substrate, the 500 substrate, but I do not see a reference on material for the scanning lines and 01:38:16

data lines.

So I cannot tell you if they are the same or different or what is the material based on Shiba, unless you have portions that you want to guide me.

Q I don't have an indication myself. 01:38:34

Is there any suggestion that the data lines or the scanning lines are made of ITO in Shiba?

A No. They are not -- they are not referred as made of ITO. ITO, it refers -- specifically for the use of the pixel electrode and the counter 01:39:02 electrode.

In general, you will not form scanning lines and data lines for a large display. And I believe this is a 14-inch diagonal display. You will not form long lines, such as the scanning lines 01:39:35 or data lines, using ITO. Those long lines will be resisted.

Q Okay.

A In Shiba it mentions somewhere that ITO is a high-resistance material and only use it for the 01:40:06 counter electrode and the pixel electrode.

So you not form long lines with ITO, but you can certainly form a second layer, because in that case you only have to transverse the thickness of the layer. You do not -- actually, the length 01:40:37

that you're transversing through that layer is very, very small.

And the cross section of that area will be large, because it will be the cross section of the sum of all the openings in that area. 01:40:58

Q All right. So do you agree that the only mention of transparent conductive layer in Shiba is as pixel electrodes 251?

A And as a counter electrode 541, column 4, line 42. 01:41:47

Q Anything else?

A Not in this preferred embodiment, not in this embodiment.

Q Well, I don't mean just in this embodiment. I'm talking about in the whole patent. 01:42:14

A I mean, in the embodiment described in the specifications. The patent provides a description of certain embodiments. And out of that examples, there is a teaching that is conveyed to the persons of ordinary skill in the art, and that teaching go 01:42:45 beyond the specific details and specific structures used in the specific -- in the particular embodiments used to illustrate.

Q Okay. So you don't find any such teaching in the description of embodiments or anywhere else 01:43:12

in this patent?

A What teaching?

Q Of using a transparent conductive layer for anything other than a pixel electrode or the electrode 541, the counter electrode; is that right? 01:43:37

A Well, what I found is that in -- there are three conductive layers. One conductive layer is the transparent pixel electrode that is mentioning to be used as the pixel electrodes and the counter electrodes. But I also found -- find, and someone 01:44:19 skilled in the art also finds, the teaching that you can use multiple layers out of these three layers, and there is a specific example between two such layers that you can make a double-layer structure using the existing conductive layers. 01:44:50

So though a specific embodiment -- there is no specific embodiment that utilizes the pixel electrode -- sorry -- utilizes the transparent conductive layer specifically for other purposes, the general teaching of combining existing layers to 01:45:12 form conductive structures is there.

And in light of other prior art, such a combination of layers will be obvious.

Q Excuse me for a second.

There is so much that we covered yesterday 01:47:59

about Sukegawa, that it would be just covering the same ground over and over again, which I don't think we want to do.

If we can use yesterday's testimony on this topic, it will shorten this deposition a lot. 01:48:18

MR. GIBSON: I don't think you need to ask the same questions again. I don't have any issue with that. I assume that we'll have the same ability when we take your experts on these too.

MR. MANZO: Right. 01:48:36

MR. GIBSON: With that understanding, I think you can use any of the questions from yesterday relating to Sukegawa in this petition as well, with the understanding we'll have the same ability to do that. 01:48:48

MR. SCHLITTER: We'll be accommodating.

MR. MANZO: Okay. Thank you.

Q Now, do you remember Sukegawa, Professor?

A I do.

Q And just to refresh, Sukegawa, in Figure 1B, for example, shows that the transparent conductive layer 8 is directly on top of the upper metal layer wiring 7, right? 01:49:24

A Yes. May I have Sukegawa reference?

Q There is the figure. 01:49:56

A Are you planning to cover that --

Q Here is a copy of Sukegawa patent that was marked as Exhibit 1005 in this proceeding.

MR. GIBSON: Thank you.

BY MR. MANZO: 01:50:12

Q And my question was just to refresh your recollection, I think, that 8 is directly on top of 7, as shown in Figure 1B.

A 8 is laid over 7.

Q Okay. Now, if a person of ordinary skill in the art were to modify Shiba, in light of Sukegawa, to provide a transparent conductive layer over the common pad 751 of Shiba, would the ITO be provided -- or would the transparent conductive layer be provided directly on the common pad 751? 01:50:47 01:51:19

A Well, as we discussed quite extensively yesterday, on top of the layer 7 there are two layers, 8 and 9. One is the transparent conductive layer and the other is the insulating layer 9.

There are two and only two possible ways that one can lay down those films on top of 7. 01:51:49

You can put 8 to touch 7 and 9 over 8 or you can put 9 above 7 and 8 above 9.

So if one wants to take those two processing options and import those in Shiba to 01:52:22

modify Shiba terminal pads, common pads, 751, they can be modified in any one of those two ways. I don't think it's been limited to one or the other because the goal is to have the ITO layer be the layer that will be in between the flexible printed circuit board and the external connection line. 01:52:57

Whether you put 8 on top of the external connection line and then you have the passivation layer and then form the opening or vice versa, you have the passivation layer, form the opening and then put the transparent conductive layer, to someone skilled in the art, both options will be obvious and whichever they choose to do, they will be equally valid for the particular embodiments that they wish to -- particular products that they wish to make. 01:53:24 01:53:42

Maybe there are some specific reasons for that particular product to choose one or the other, but they are equally valid -- they are equally sound approaches, and they are both obvious. 01:54:01

Q Okay. I understand. Is there anything in Sukegawa that suggests flipping the order of layers as between 8 and 9 with respect to layer 7?

MR. GIBSON: Objection; form.

BY MR. MANZO: 01:54:38

Q I'll rephrase the question.

Is there anything in Sukegawa that suggests that the person ordinarily skilled in the art could deposit layer 9 directly on top of layer 7 and then put transparent conductive film 8 on top of 9, 01:55:16
presumably after 9 were etched? Is that actually taught in Sukegawa?

A Well, you see that teaching when you have to connect 2 to 7 and you have 3, which is insulating layer in between. 01:55:46

So in connecting 2 and 7, and you have an insulating layer in between, you opening the contact holes and you establish regions where the upper layer will touch the lower layer.

So if you have, again, two layers, an 01:56:20
insulating and a conducting, that you want to lay over another conducting layer, isn't that obvious in light of the underlying structure, namely, between 2, 3 and 7, isn't that structure similar to 7, 8, 9, flipping the sequence of the orders and putting the 01:56:49
opening -- and doing the etching to form the opening first versus last?

They are teaching in Sukegawa -- how to connect lines, two conducting lines, with an insulating layer in between is within Sukegawa, and 01:57:13

that's no different connecting 7, 8 -- combining 7, 8 and 9.

I did not recall if the claims in Sukegawa are broad enough that it can cover both embodiments.

Q In Sukegawa, are layers 2 and 7 made of the same material? 01:59:16

A In the detailed description of the preferred embodiment, it reads -- on column 4, line 10, it reads, "a chromium film is an opaque conductive film that is deposited to a film thickness of 149 nanometer on the entire subsurface of the glass substrate 1 by spattering process followed by being patterned to form a lower layer metal wiring 2." 01:59:59

So there is a specific disclosure that the lower wiring is chrome. And then further down in column 4 on line 46 it reads that another chromium film is opaque conductive film, is deposited to a film thickness of 140 nanometers so as to cover the inter-layer insulation film 3. 02:00:18 02:00:51

So in this preferred embodiment, they are both described to be as chromium. That is another section on column 8, at line 55 that it reads, "While the present invention has been explained with reference to the preferred embodiment, the invention 02:01:25

is not restricted only to such embodiments, but various modifications are possible within a range not departing the purpose of the present invention. For instance, the lower layer metal wiring and the upper layer metal wiring are made of chrome, but, 02:01:52
instead, a single layer or a composite layer, such as made of aluminum, tantalum, molybdenum and tungsten may be used. Further, the materials for the lower layer metal wiring and the upper layer wiring may not always be identical." 02:02:18

So this paragraph in this section in the first sentence it says that multiple -- that variations and modifications can be implemented, and switching the order with which 8 and 9 falls within the scope of Sukegawa will result in the same 02:02:57
benefits.

And the second sentence gives an example that is referring to switching the materials used for the wirings 2 and 7, or changing the materials or -- referring to the selection of materials that 02:03:31
could be used to form wirings 2 and 7.

Q Thank you. Just to make sure that I understand you, it is your testimony that switching 8 and 9 relative to 7 is suggested by the first sentence in column 8 beginning at line 55? Is that 02:04:05

what you said?

A I said the invention is not restricted only to such embodiments.

So there are several embodiments described in Sukegawa, and this sentence say that the invention is not restricted only to such embodiments, but various modifications are possible. 02:04:25

So it is my testimony that someone skilled in the art, switching the order of 8 and 9, it will have been obvious, particularly because making a connection between 8 and 7 with the layer 9 in between 8 and 7, you simply replicate the process sequence that is used in connecting 2 and 7 where 3 is in between. 02:04:49

Q Forgive me if I'm taking a bit of time to formulate my next question, but I'm skipping a lot in light of yesterday's testimony. 02:06:50

MR. GIBSON: That's always appreciated.

THE WITNESS: Let me take a one-minute break. 02:07:09

MR. MANZO: Sure.

THE VIDEOGRAPHER: Off the record at 2:07 p.m.

(Recess.)

THE VIDEOGRAPHER: Back on the record at 02:14:36

2:14 p.m.

BY MR. MANZO:

Q Professor, I invite your attention to the '204 patent.

I may have asked you similar questions yesterday, but if you look at Figures 4A and 4B, do you see that the ITO 114 is not covered anywhere by the resin inter-layer film 113? 02:15:11

A I see that in Figure 4A and 4B.

Q Is there any advantage to that that you recognize? 02:15:56

A Such as?

Q Well, I'm just trying to understand what you recognize.

A As I said, there are two layers that need to be placed over 403. One way is to put the resin inter-layer film first, then create -- form the openings, and then put 114, as shown here. 02:16:38

Q Would a person ordinarily skilled in the art in 1997 have recognized an advantage to doing it one way or the other way? 02:17:19

A Figure 4A shows us one way and Figure 1B in Sukegawa they are referring shows a different way. These are the two possible ways to implement them.

It is my opinion, and reading the 02:17:51

specifications of both patents, neither inventor wanted to limit to one or the other. They described a particular embodiment.

Now, what someone skilled in the art chooses to do will depend upon a lot of details that 02:18:13
will be applicable to the selection, to the flow in manufacturing lines that they have.

As I said a number of times, there are only two options, and inventors of one do it one way in their preferred embodiments, and perhaps inventors 02:18:41
of a later patent choose to do different from the earlier patent, maybe perhaps to show it is different, but I tried to explain that someone skilled in the art, both ways are obvious.

So even before the '204, both ways were 02:19:08
obvious. And the '204, as I said -- within the context of '413 yesterday, the '204 does not claim any advantages for that part. '204 is not describing the advantages of having the ITO on top of the inter-layer resin film, it doesn't try to 02:19:36
make that as a claim invention.

If you read the specifications, and I'm sure you have read it a number of times, over many, many columns, the inventors discuss these adjustment layers, what materials, what shape, what to extend, 02:20:00

how to connect them, or to form one continuous, so there are a lot of discussion about the adjustment layers. So -- and as far as this terminal connection, there is only a very brief reference to it, and that is in example 3 in column 8 in line 53 to 55 that reads, "Referring to Figure 4A, the external connection lines 403 are electrically connected to an FPC (flexible printed circuit) 107 through contact holes provided in the resin inter-layer film 113 through ITO (indium tin oxide) film 114," period. That's the only reference I have found. And guide me if there are others that refer to this connection. 02:20:24 02:21:00

And in these four brief sentences here -- four brief lines, in this entire sentence, I do not see any claim advantages. And even the level of details is -- of how to form it is not explained. There is no order with what the layers are put down, it doesn't list that you have to list -- put down the resin inter-layer film first and the indium tin oxide on top of it. 02:21:25 02:21:53

That description, that language, as I said yesterday and I'm saying it again now, it is broad enough that covers both implementations of connecting ITO and the layer 403. 02:22:19

Perhaps the inventors wanted to have it broad enough so it would cover both embodiments, but to someone skilled in the art, that is broad and covers many embodiments.

Similar to Sukegawa does not disclose the other embodiments, that the inventors of '204 didn't choose to create an embodiment like the one in Figure -- like the one in Figure 1B of Sukegawa. Choose to have one, but then have enough -- have a language which is broad enough that cover both. 02:22:52 02:23:17

I'm not expert in writing patents. I don't know what the advantage or disadvantage of broad language, but that's the only reference I found for that particular connection.

Q Thank you. 02:23:36

Looking a little more at Sukegawa and the Figure 3 pages, Figures 3A through E, in Figure 3D would you agree that the -- I think you agreed yesterday that the sealant is between structure 100 and structure 200. 02:24:38

A The edge of 200.

Q Okay. And that would be to the left of the left edge of the tape carrier package 300, correct?

A Correct.

Q Would you agree that the tape carrier 02:25:02

package 300 could not extend between structures 100 and 200, for at least the reason that it's much too thick?

A I do not know what you mean by the reason at least it is too much thick. 02:25:29

Q That the tape carrier package 300 is much too thick and it would introduce a very large gap between 100 and 200.

A The tape carrier package 300 comes down onto 100 after 200 already has been formed. So the 02:25:54 sequence of which comes first is very specific. You fabricate the wirings and the transistors on 100, you bring 200, you seal it, you fill it with liquid crystal, and then you build 300.

By the time 300 comes to -- and applied 02:26:22 onto 100, 200 has already been formed.

Q Okay. Now, looking at Figure 3E, I invite your attention to the space marked 14 between the tape carrier package parts 31 on the right side of 14 and the structure on the left side of 14. 02:26:55

And do you see that the upper layer wiring 7 has been removed in the region 14?

A That is another embodiment in Sukegawa, and I did not rely on that embodiment for my analysis. But I see in this embodiment that you are referring 02:27:20

in Figure 3 what you just described.

Q Would that normally be done by an etching step before layer 8 is deposited?

A You're asking me the details of fabricating the embodiment shown in Figure 3? 02:27:57

Q Yes. Just with regard to removing that bit of the upper metal layer 7 in that particular spot.

A For building that particular embodiment, it is obvious that if you want to add a layer and remove portions of it, you do that before you cover 02:28:39 it by another layer, so the answer is yes.

Q Okay. Now, as between Figure 2C, about which you did testify in your declaration, comparing Figure 2C and Figure 3E, assuming that all the dimensions are the same and all the materials are 02:29:09 the same, please make those assumptions, does Figure 3E present the higher resistance between the copper foil 31B and the left side of layer 2?

MR. GIBSON: Objection; form.

THE WITNESS: What are you referring to? 02:29:50 Left side of layer 2?

BY MR. MANZO:

Q The part on the left side of the drawing, the left side of 2.

A Okay, the end -- the far left of the 02:30:03

drawing?

Q Yes.

A At the end.

Q At the metallic layer or the wiring layer 2. 02:30:13

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Well, Professor, do you understand what I'm asking?

A No, I think I understand. Don't worry, I think I understand what you're asking. 02:30:41

Q Okay.

A I just want to make sure I didn't misunderstood anything.

If one compares Figure 2C and Figure 3E, and assuming all the dimensions are identical, as you highlighted, and we measure the resistance between the flexible printed circuit board and the far left of wiring 2 in Figure 3 and compare that to the far left of Figure 2C, Figure 2C will have a lower resistance. 02:30:55 02:31:43

Q Is that because part of the upper metal wiring has been removed?

MR. GIBSON: Objection; form.

THE WITNESS: The two wirings in Figure 2C 02:32:00

are forming a parallel path for the signal to go, so you have element 7, what is continuing to the left without any gaps, and that will have a lower resistance compared to the Figure 3E where a portion of the 7 has been removed and you only have 8, which is known to have a lower resistance than 7. 02:32:37

BY MR. MANZO:

Q Thank you.

A But, as I said, I did not use Figure 3 in my analysis, I used Figure 2C in my analysis. 02:33:05

Q Yes. Thank you.

A And what you just described, as you admitted, a double layer structure to the left of the flexible printed circuit board, it creates a lower resistance structure, because I think there was a discussion in one of the responses that said that that part does not create any -- does not have any effect from the resistance. 02:33:33

And these discussions that we have, it is good to clarify that we both agree that the resistance to the left of the flexible printed circuit board is lower by having the two wires running parallel. 02:33:50

Q Well, thank you. I thought that my questions were just questions rather than testimony 02:34:48

on my part.

But that's something that counsel for the petitioner can talk to you about, after the deposition.

MR. GIBSON: Not during the deposition. 02:35:08

THE WITNESS: I think we are all here to clarify the records.

BY MR. MANZO:

Q Professor, in making a liquid crystal display device, are there technical reasons why a person ordinarily skilled in the art would want to avoid covering indium tin oxide with a protective layer? 02:36:34

A What do you mean by "technical reasons"? I mean process compatibility reasons or performance of the system reasons, or you group them all into one broad category? 02:37:35

Q I don't want to restrain your answer in any way by narrowing the scope of your answer.

A I'm trying to understand the scope of your questions. 02:38:01

I'm not aware of technical reasons of covering ITO with an insulating layer, will that create problems as far as compatibility with the processing steps. 02:38:25

You can coat an ITO layer with a passivation layer.

In the pixel electrode region, that what used to be the case, it used to be that the ITO electrode was covered by a passivation layer. 02:38:43

I believe in some of the earlier implementation of the active matrix liquid crystal displays, that in those displays, the voltage you had to apply on the pixel electrode to create a certain twist of the liquid crystal was high because 02:39:16 the twist of the liquid crystal was a function of the strength of the electric field. And by having the pixel electrode lower than the passivation layer, increase the -- increase the layers between the ITO and the counter electrode. You have the gap 02:39:46 and then you also have the passivation layer, so the electric field was lower.

To reduce the voltage and, hence, to increase the electric field people either start removing the passivation layer by creating an 02:40:11 opening on the pixel electrode or by flipping the order and putting the pixel electrode on top of the passivation layer.

That what comes in my mind at the end of these two long days is technical reasons and 02:40:32

advantage/disadvantage, putting them on top of each other, it refers to the electric field on top of a pixel electrode in the array and how that's related to the voltage of the -- that it is -- the electric field, how the electric field is related to the voltage you put to the pixel electrode, and I believe that is mentioned in one of the patents that are used in some of the other inter partes that have used. I don't recall exact which one now, but I think that's what it was referred to. 02:40:58 02:41:20

Q Okay.

A If you have something else in particularly that you want to do, please relate more specific and I will remember.

Q I think you already answered this, but you said that the protective layer can be placed over the ITO? 02:41:39

A In the pixel electrode region, there could be a protective layer on top of the ITO. That protective layer will reduce the electric field that will go. So either one has -- if you want to operate the lower voltages, lower power, you either have to create an opening on top of the pixel electrode and remove that dielectric or put the ITO on top of the dielectric. 02:42:01 02:42:28

Q What about the strength of the composite in terms of one material adhering sufficiently well to the material below it?

MR. GIBSON: Objection; form.

THE WITNESS: Are you talking about the passivation layer, like passivation layer, say, 9 in Sukegawa? 02:42:56

BY MR. MANZO:

Q Yes.

A Well, like depending on like 9 adhering better to ITO or ITO adhering better to 9? I don't quite understand your question. 02:43:09

Q That's fine. We'll just move on.

In Sukegawa is it true that to avoid a risk of corrosion, Sukegawa uses double coverage over the upper level wiring 7, where the double coverage is the transparent conductive film 8, together with the protective insulation film 9? 02:43:38

A In the parts of 7 that are not exposed in order to make a contact to the flexible printed circuit or be used for testing, are you referring to that portion, the portion which is to the left of the left opening or the vertical edge of the left opening? 02:44:25

Q Yes. 02:44:47

A Yeah, both layers are used for protection.

Q Yes, okay. Thank you.

A But reversing the order will equally provide both layers in that region.

Q Well, do you agree that Sukegawa discloses that the transparent conductive film 8 needs to be formed directly on top of the upper metal layer wiring 7 in order to avoid corrosion? 02:45:51

MR. GIBSON: Objection; form.

THE WITNESS: 8 needs to be formed above 7, but whether 8 is directly above 7 or you have 9 in between 7, I do not find any evidence in Sukegawa to say that one is better than the other one and that one should be avoided in favor of the other. 02:46:25

If you do have that, please guide me to that part and I will remember it. 02:46:50

BY MR. MANZO:

Q I'm not aware of Sukegawa discussing the option of putting 9 directly on top of 7, and that the only disclosure I'm aware of in Sukegawa is that the ITO 8 is on top of the wiring 7. 02:47:18

Are you aware of any other specific affirmative teaching in Sukegawa otherwise?

A I think I read the part in column 8, line starting at 55, that "while the present invention 02:47:57

has been explained with reference to the preferred embodiments, the invention is not restricted to such embodiments, but various modifications are possible within the range not departing the purpose of the present invention." 02:48:17

So that would have been one set of choice that one could form.

Q Where does that sentence say that you can put 9 on top of 7?

A It says, "various modifications are possible." 02:48:49

Q But it doesn't say what they are.

A It lists one example as far as the visualization, so rely on what someone skilled in the art will consider whether certain modifications will become obvious in light of the teachings in Sukegawa. 02:49:12

For example, Sukegawa teaches that layers 8 may have pinholes and layers -- and pinholes in layer 8 may lead into corrosion of the underlying layer 7. 02:49:40

So if we put 9 directly above 7, and 8 above 9 and create the openings, that will be one way to remove the effect of the pinholes in 8 from the effect of 7. 02:50:17

Q Well, that may be one possibility, but Sukegawa actually does something different, doesn't he or they, if you know?

A Again, in the particular embodiments -- in the particular embodiments that he lists, but to someone skilled in the art, other modifications may also be obvious. 02:50:34

And I discussed earlier that having 9 above 7 and 8 above 9, it will simply duplicate the structure that is listed below, namely the connections between 2 and 7. 02:51:03

Q Okay. But just to make perfectly clear, do you agree with me that there is no figure that shows that in Sukegawa?

A The figures list specific embodiments in the paragraph I read -- 02:51:18

Q We'll get to the text next. I just want to ask you about the picture first.

So do you agree that there is no picture showing this change in order? 02:51:39

A No, the pictures list specific embodiments, and that's a different embodiment.

Q All right. Now, turning to the text of Sukegawa, do you find a specific suggestion beyond column 8 saying you can make modifications where it 02:52:01

says one of the modifications you can make is to put 9 on top of -- sorry, you can put 8 on top of 9? Is that anywhere in here specifically?

A It has been two long days, so if you give me time, I will read it again to find out supporting evidence. And I have to reframe my mind again to the claims if they suggest that part. 02:52:29

If you want me to look at it again, I will take the time to look at it again. I --

Q Sure. That's fine. How long would you like? 02:52:57

A I don't know what is my mental capability right now, but, I don't know.

Q Should we take a recess while you do this review and come back in a few minutes? 02:53:27

A Sure.

Q Okay.

THE VIDEOGRAPHER: Off the record at 2:53 p.m.

(Recess.) 02:53:34

THE VIDEOGRAPHER: Back on the record at 3:13 p.m.

BY MR. MANZO:

Q So, Professor, have you found that specific citation, if there is one? 03:13:33

A I found several sections in which Sukegawa is teaching the advantages of placing ITO directly on insulating layer. And by doing the placement of the ITO directly on the insulating layer, pinholes within the indium tin oxide layers will not affect the reliability of any underlying metal layer, because below the indium tin oxide layer there will be an insulating layer. 03:14:44

Those portions are discussed with reference to the different embodiments of Sukegawa, so the teaching in Sukegawa -- so within Sukegawa there is a teaching that it is advantageous to place the transparent conductive film 8 that will be exposed directly on the surface of an insulating layer. 03:15:14

So it will take someone with ordinary skill in the art to place 8 on top of 9, given the teachings within Sukegawa that such a placement will create a more robust structure because it will solve the problem of the pinholes. 03:15:46

Q Okay. So where are those citations, please? 03:16:15

A So in column 6, lines 23 to 38, starting from the part that reads, "Accordingly, even if the transparent conductive film 8 in the terminal portion contains a defect or even if it is used in a 03:18:57

high humidity atmosphere, the upper layer metal wirings, 7-1 and 7-2 are not exposed to the external air and protected against corrosion," and continues, "in that embodiment, the transparent conductive film 8 is shown to be formed directly on insulating layer." 03:19:24

That insulating layer is not subject to any corrosion because it does not react. It is already an oxide or nitride.

So it shows that if I place the transparent conducting film on an insulating film, and even if there are pinholes, those pinholes will not cause any corrosion. 03:19:46

Q Professor, isn't that discussing Figure 3E, and they are talking about the part of layer 8 where there is no layer 7 underneath it to be corroded by pinholes? 03:20:16

A I think that's the essence of the teaching, you place the transparent conductive layer that will be exposed not directly on top of a metal, so if there are pinholes, you will not expose the underlying metal into it. 03:20:39

So you it will take ordinary skill in the art that if you reverse the order with which 8 and 9 are laid down, you will gain that advantage by 03:21:06

having the 8 on top of an insulating layer throughout the surface. And the same thing has also been taught in another embodiment where, again, the placement of the transparent conductive layer directly on top of an insulating layer and not above the metal, it results in this improved reliability. 03:21:32

Q Okay. Is there a further citation that you located?

A Yes, let me -- so it is column 7, line 48, and I'm quoting, "Also in this embodiment, the transparent conductive film 8 exposed through the aperture portion of the protective insulating film 9 is formed directly on the surface of the inter-layer insulating film 3 under which the upper layer metal wire 7 is not present in the same manner as in the first embodiment. Accordingly, if the transparent conductive film 8 in the terminal portion contains defect or it is used in a high humidity atmosphere, the metal wiring 7 is not exposed to the external atmospheric and can be protected against corrosion." 03:22:44 03:23:05 03:23:21

So in both these embodiments, Sukegawa teaches the advantages of placing the transparent conductive layer directly onto an insulating layer, which, by itself, would be resistant to corrosion and will not be affected if there are any pinholes 03:23:46

in the transparent conductive layer.

So it will take somebody with ordinary skill in the art to see that reversing the order 8 and 9, that will result in such advantages because 8 will be on top of an insulating layer and any pinholes will not affect the underlying layers. 03:24:13

Q Anything else? Are those all the ones you found?

A And there is another embodiment it is placing the ITO on top of the glass where it is an insulating layer. So there are three embodiments within Sukegawa that discuss the advantages of placing the ITO on an insulating layer. It gives two examples of what are those insulating layers. One is the insulating layer 3, another is the glass substrate. 03:24:34 03:25:00

So I will take ordinary skill in the art to reverse the order of 8 and 9 and place 8 above 9 to get the benefits of placing the transparent conductive layer on to an insulating substrate. 03:25:23

Q Thank you.

A If I may, outside of Sukegawa, that has also been disclosed in other prior art references that I have reviewed as part of this proceeding. It was well known at the time of the invention that the 03:25:48

placement of the ITO on the upper surface of the passivation film would result in some advantages as far as the corrosion concerns.

Placing the IT on top of 9, particularly the time that the '204 was filed was certainly not 03:26:23
an innovation. I'm not sure what was the priority day, but even by Sukegawa is better than the '204 and Sukegawa is listed as a reference in '204 so I'm sure that the artist have to put a reference -- sorry, a drawing that will not be exactly the same 03:27:09
as the one depicted by Sukegawa.

But, as we discussed and I testified a number of times already, the language in '204 is broad that covers both structures.

Q If there are advantages to putting the ITO 03:27:40
layer 8 above layer 9, can you think of any reasons why Sukegawa did not illustrate that in Figure 3E, for example, or even in Figure 2C?

A Perhaps Sukegawa wanted to avoid having an 03:28:14
embodiment that would look like other prior art pieces that had ITO above the layer 9.

Q You don't have those references here today, do you?

A No. You may have it.

If you look at the prior art, Moriyama, you 03:28:55

will see that the ITO layer is the upper layer and it has been placed on top of an insulating film.

Do you happen to have Moriyama with you?

Q No.

A I'm sure my counsel can try to generate it. 03:30:04

Q Is it correct that in the column 7 citation you gave us, Sukegawa --

A Which line?

Q At line -- well, I think you cited 48 to 57. 03:31:37

Is the transparent conductive layer on top of the oxide layer 3 or, rather, the nitride layer 9?

A Well, in the particular embodiment discussed in this section, it is form the 03:32:18 inter-layer insulating film 3, but the benefit of placing at here on top of an insulating film will apply independently of what is that insulating film, whether that will be the 3 or the 9. Because they are -- both 3 and 9 will not be affected if there 03:32:56 will be a pinhole in the transparent conductive layer, none of them will be reacting and corroding.

Q I understand.

In your citation at column 6, lines 23 to 38, is that also talking about placing the ITO film 03:33:23

on top of the oxide 3, rather than on top of the nitride 9?

A Inter-layer insulating film 3 is a composite film that includes an oxide, silicon oxide film and silicon nitride film. It is column 4, line 22. It reads, "a composite film of a silicon oxide film and a silicon nitride film to form an inter-layer insulating film 3 is formed." 03:34:12

So both 3 and 9 contain silicon nitride, so it's not that one is better than the other one. 03:34:38

Q But is it the case that in the Figure -- sorry -- in the column 6 passage you mentioned, Sukegawa is talking about the transparent conductive layer over the insulator 3?

A In this particular embodiment. But the advantages of having 8 on top of 9 will be the same as having on top of 3. 03:35:42

Q I understand what you're saying.

Do you agree that there is no embodiment in Sukegawa where 8 is over or on top of 9, specifically? 03:36:19

A There is no drawing, but the teaching for creating and modifying the embodiment discussed, the preferred embodiment we discussed, is there. And Sukegawa teaches that various modifications are 03:36:56

possible. And placing 8 above 9 is one such obvious modification or possible modification.

It would be better to say obvious and possible. Even better, an obvious possible modification. 03:38:18

Q The passage that you're citing does not say, specifically, to have an embodiment with layer 8 over layer 9, does it?

A The passages I described teach the benefits of having ITO on top of an insulating layer. They use an example. They have two examples, two different insulating layers, and those are two different insulating layers. 9 would have been an obvious modification. 03:39:04

Q I understand what you're saying. That doesn't mean I agree with you, but I understand what you're saying. 03:39:35

I want to ask you some questions about the '204 patent. I believe you have a copy in front of you. 03:40:01

I think that the first claim that is challenged is claim 31; is that right?

A I have to refer to my declaration.

That's correct.

Q Okay. Well, let's look at claim 31, then. 03:41:31

That appears at column 17, lines 35 through 63, or 62.

Do you have that before you?

A I do.

Q Good. 03:41:56

Actually, let's, instead, turn to claim 54. That starts at column 19, line 62 and extends down through column 20, line 31.

Do you have that before you now?

A I do. 03:43:10

Q Okay. Good.

And if you read through this claim, I think that you'll find the use of the word "over," for example, at column 20, line 3 --

A Okay. 03:43:37

Q -- which calls for a first conductive line over the substrate.

And these questions are much like the ones I asked you yesterday about the sequence.

So does the word "over" imply a sequence here as between the substrate and the first conductive line? 03:43:46

A It means that the first conductive line is formed over the substrate, that the substrate preexists the first conductive line. 03:44:08

Q Okay.

A You cannot form the substrate over the first conductive line.

Q Does the next claim element, a first insulating film over the conductive line, call for the first conductive line to be in existence first with respect to the first insulating film? 03:44:25

A That's correct.

Q And, correspondingly, or similarly, does the next claim element at column 20, line 5, which recites, "a second conductive line over the first insulating film," does that require the existence of the first insulating film to be in existence prior to the second conductive line? 03:44:46

A Yes. 03:45:09

Q Does the next paragraph of the claim similarly have a sequence implicit in it? That one calls for a, quote, transparent conductive layer over a first region of the second conductive line, closed quote. 03:45:37

Does that mean that the transparent conductive layer is placed after the second conductive layer -- sorry, the second conductive line is established?

A The transparent conductive layer is formed 03:45:58

after the first region of the second conductive line is formed.

Q And the next claim element, must the flexible printed circuit be placed over the first region of the second conductive line, does that mean that the second conductive line must be formed first before the flexible printed circuit is put there? 03:46:18

A That's correct.

Q And next, where it says that a sealant -- strike that. 03:46:38

It says, quote, a sealant over a second region of the second conductive line, closed quote.

Does that language imply that the second conductive line must have a second region which is established before the sealant is placed there? 03:46:55

A That is correct.

In all these cases, we relay the sequence of two elements. And the only thing we can say from each individual sentence is which comes first and which comes second. 03:47:24

If we take certain of these sentences as a group to relay the sequence of more than two elements, then in some sections an explicit order of which comes first, second and third also appears.

The fact that there is a sequence between 03:47:58

two different elements, it does not imply inherently the sequence of more than one -- more than two elements. I don't know if I'm making myself clear.

Q Okay.

A But please continue. 03:48:24

Q Okay. The next one is on line 14 and that calls for a conductive layer over the substrate.

Does that mean the substrate must exist before the conductive layer is placed over it?

A Yes. But, for example, in this particular 03:48:38 sentence, a conductive layer over the substrate, we can only say the relationship, the order, between those two elements; for example, that sentence by itself, it does not, for example, relate the conductive layer with any of the previous elements 03:49:05 that were discussed, for example, to know how the conductive layer -- maybe start again.

That sentence, "a conductive layer over the substrate," it only implies an order that the conductive layer is formed after you have the 03:49:41 substrate. But that sentence alone does not relay the conductive layer, it does not relay the order with which the conductive layer was placed over the substrate in relationship to any of the other elements that we are already discussed. And we 03:50:05

discussed a number of elements that are over the substrate. For example, we had the first conductive line over the substrate, we had the first insulating film over the first conductive line, hence the first insulating film is also over the substrate. The second conductive line over the first insulating film also, which means that the second conductive line is also over the substrate. 03:50:24

So this is three other elements, first conductive line, first insulating film, second conductive line, that are also over the substrate. And here we have, in this line 14, another element over the substrate. 03:50:38

So I'm just trying to clarify that the order, in using the word "over," is implied only between those two elements that are used in that sentence. 03:50:56

If we want to derive the relationship or the order among multiple layers, we have to look in more than one of those statements and see if that such relationship can be established in a unique way or there are multiple ways that can be established. 03:51:17

Q Looking at the subparagraph beginning at line 21, which reads, "Wherein the second conductive line and the flexible printed circuit are in 03:52:13

electrical contact through the transparent conductive layer."

Is there an implied sequence there that tells us that the contact -- that tells us anything about the contact? 03:52:38

MR. GIBSON: Objection; form.

THE WITNESS: What do you mean?

MR. MANZO: Strike the question.

Q Let's move on to the next claim element.

The next claim element says, "Wherein the second conductive line and the transparent conductive layer are in direct contact through an opening in the second insulating film." 03:53:04

Does the opening in the second insulating film provide the ability for the second conductive line and the transparent conductive layer to have direct contact? 03:53:27

MR. GIBSON: Objection; form.

THE WITNESS: Whether it provides the ability for the second conductive line and the transparent conductive layer to have direct contact or, alternatively, between the vertical walls of the opening, the second conductive line and the transparent conductive layer are in direct contact depends upon how you construe the word "through." 03:54:00 03:54:24

That sentence alone is subject to the construction of the word "through."

We can look at the earlier sections above and we can try to derive a sequence of layers and we can try to see if one of those two possible outcomes for the construction of the word "through" can be revealed. If the word "through" can be construed as -- as you said, whether the opening provides the ability to have direct contact, which I guess it would be construed as being because of the opening, or that the contact existed between the opening, the vertical -- the edges of the opening, the vertical walls of the opening. 03:55:02 03:55:44

And if we do the analysis as we have started doing it, an expert will -- not an expert, someone with ordinary skill in the art will see that there is no specific order that is described, rather a broad language is used that -- to describe the relationship between the second conductive line, the flexible printed circuit and the second insulating film. 03:56:03 03:56:41

Both the second insulating film and the transparent conductive layer, they are both over the second conductive line. They do not list the order which one is above what. 03:56:59

MR. MANZO: I think we have to change the video disk.

THE VIDEOGRAPHER: This is the end of tape 2. We are off the record at 3:57 p.m.

(Recess.) 03:57:18

THE VIDEOGRAPHER: This is the beginning of tape 3. We're back on the record at 4:11 p.m.

BY MR. MANZO:

Q Professor, I think you were in the middle of analyzing claim 54. 04:11:32

Had you finished your answer about whether the opening referred to at column 20, line 25 is the structure that permits the second conductive line to have direct contact with the transparent conductive layer? 04:12:17

A What I wanted to say and is not quite captured in my last statement, in the last sentence of my previous statement, is that based on the different limitations listed above for the different elements, one cannot see an order between the 04:13:36 transparent conductive layer and the second insulating film.

Both are over the second conductive line, but the language is broad and does not express or implies a specific order. In that -- in the context 04:14:11

of such a broad language, the word "through" cannot be construed in a unique way.

Q Looking at Figure 4A, would you agree that the second conductive line shown in this figure is in direct contact with the transparent conductive layer, which is 114, only because of the existence of the opening in the resin inter-layer film 113? 04:15:01

MR. GIBSON: Object to the form.

THE WITNESS: In the particular Figure 4A in this particular embodiment in this particular way of fabricating and constructing the structure, this is true, but the language used in the claim -- and, if I may add, the language that is in the text of the specifications within '204, and, in particular, the section that I read to you earlier within the example 3, column 8, lines 53 to 55, the language is broad and is not limited to just one embodiment. 04:16:22 04:16:55

BY MR. MANZO:

Q That language says, "Referring to Figure 4A, the external connection lines 403 are electrically connected to an FPC (flexible printed circuit) 107, through contact holes provided in the resin inter-layer film 113 through ITO (indium tin oxide) film 114." 04:17:31

Is that what you're citing? 04:17:58

A Exactly.

Q And you agree -- let me ask.

Do you agree from the very first words of that sentence that it is referring to Figure 4A, where it says, quote, Referring to Figure 4A, closed quote? 04:18:20

A Right. But that language, if I may ask, how is it different from the Figure 1B of Sukegawa? Isn't that language here that the "external connection lines 403 are electrically connected to an FPC (flexible printed circuit) 107 through contact holes providing the resin inter-layer film 113 through an ITO (indium tin oxide) film 114"? 04:18:39

Doesn't that language describe exactly what it is in Sukegawa? 04:18:59

Q I don't think so, no, but that's what we're going to let the board decide.

A No, I understand.

But if we -- we agree that Figure 4A shows something. 04:19:15

Q Yes.

A I don't think we disagree with that part.

Q Good.

A Okay. Now, referring to the text that describes the "external connection lines 403 are 04:19:23

electrically connected to an FPC (flexible printed circuit) 107 through contact holes providing the resin inter-layer film 113 through an ITO (indium tin oxide) film 114," and I say that that sentence, someone with ordinary skill in the art will see 04:19:50
exactly that part. That's how someone ordinarily skilled in the art will describe the connection between the external connection lines and the flexible printed circuit board by looking at the Sukegawa, and that's the only reference I find in 04:20:07
the specifications that is relevant to construe the word "through," Figure 4A and that sentence.

And I said that sentence is exactly what is described in Sukegawa if we just change the numerals to the ones used by Sukegawa. 04:20:42

I understand that the words should be -- could be construed in light of specifications, but in this case, the specifications themselves contain a very broad language.

And if there is any other section in the 04:21:29
specifications that you read something else in relationship to the order of the different layers, in particular the second insulating film and the transparent conductive layer, please bring out to me so I can review that section in case I have already 04:21:47

miss it.

Q Give me a moment to consider what you said.

A moment ago you said we could substitute the -- we could change the numerals to refer to Sukegawa and change the sentence that's in column 8. 04:24:27

Can you go ahead and do that for us so that this sentence would describe Sukegawa?

A The external connection lines 31 are electrically connected -- strike that.

The external connection lines 7 are 04:25:36 electrically connected to a FPC (flexible printed circuit) 31 through contact holes provided in the resin inter-layer film 9 through ITO (indium tin oxide) film 8.

If I may add, that sentence even captures 04:26:16 better Figure 2C of Sukegawa than Figure 4A that it is referring to, because at least the flexible printed circuit through contact holes.

And that's what we see in Figure 2C of Sukegawa, we see the openings in 9. 04:26:38

And then says "through an ITO," and we see that in Sukegawa.

Q In the '204 patent, looking and the Figure 4A or 4B, is there a sealant on only the second insulator and not on the ITO? Do you see that? 04:29:13

A This is what is depicted in Figure 4A.

Q And do you agree that the ITO is formed after the second insulator?

A Based on Figure 4A?

Q Yes, based on Figure 4A. 04:29:45

A Okay.

Q Do you agree?

A This is what is shown.

Q Okay. And I think, as you just discussed or we've just discussed for a while, Figure 4A shows 04:30:01 an opening in that film 113 so that the external connection lines 403 can contact the conductive layer 114; is that right?

A Looking at Figure 4A in the way that the -- this particular embodiment is drawn, this is right. 04:31:07

Q And you agree that in Figure 4A the sealant 105 is not on top of the ITO 114, but, instead, it is separated from it; is that correct?

MR. GIBSON: Objection; form.

THE WITNESS: In this particular embodiment 04:31:49 shown in Figure 4A, this is what it shows, but the claims do not provide any limitation on the placement of the sealant with respect to the ITO, or I do not recall such a limitation.

BY MR. MANZO: 04:32:11

Q Do you agree that the '204 patent reduces the height difference that is caused by the formation of the auxiliary line, which is the first conductive line 401 and the external connection line, which is the second conductive line 403? 04:32:31

MR. GIBSON: Objection; form.

THE WITNESS: The objective of '204 is to address the issue of unevenness around the seal area and provide certain -- several embodiments of how to do so, depending upon the construction of the wiring 04:33:28 used in making the external connections.

BY MR. MANZO:

Q Okay. Do you agree that the '204 patent uses adjustment layers to keep a relatively constant seal height -- strike that. 04:33:49

Do you agree that the '204 patent uses adjustment layers to preserve a relatively constant spacing between the substrate and the counter substrate even though an external connection line and an auxiliary line, one above the other, pass 04:34:11 underneath the sealant between those two substrates?

A Well, the '204 patent alleges, as innovations, the use of the adjustment layers to preserve a relatively constant spacing between the substrate and the counter substrate, even though an 04:35:13

external connection line, auxiliary line, one above the other pass underneath the sealant between those two substrates.

And it's my understanding it's the purpose of these proceedings to determine if these are, indeed, new innovations worthy of issuing a patent or not. 04:35:30

In my analysis, I found prior art that meet exactly the same -- provide similar structures -- actually, same structures to solve that problem. 04:36:00

Q Is it true that you did not find any adjustment layer in the Shiba patent for attacking that problem?

A Shiba does not address the issue of the spacing between the two substrates, but the prior art reference which I utilized, namely, the Watanabe patent, address that issue. 04:36:27

So Shiba, in view of Watanabe, teach or render obvious these substrate gap adjustment layers. 04:37:32

Q In Shiba, you have spoken about a transparent conductive layer, right?

A (No audible response.)

Q Do you recall that we talked about a transparent conductive layer in Shiba? 04:38:07

A There is a transparent conductive layer disclosed in Shiba.

Q Is there any disclosure or teaching or suggestion in Shiba that the transparent conductive layer should not extend to the second region that is defined by the claims at issue here? 04:38:22

MR. GIBSON: Objection; form.

BY MR. MANZO:

Q Well, Professor, I think your counsel wants me to point you to the particular claim, so let me modify my question. 04:39:44

Do you see that claim 54 refers to a first region and a second region of the second conductive line?

MR. GIBSON: Which claim? 04:40:05

MR. MANZO: 54.

MR. GIBSON: Thank you.

THE WITNESS: Yes.

BY MR. MANZO:

Q Okay. So I'm asking whether there's any teaching, suggestion or other specific motivation in Shiba that the transparent conductive layer should not extend to the second region defined in claim 54 of the '204 patent? 04:40:44

MR. GIBSON: Objection; form. 04:41:23

THE WITNESS: I use Shiba, in view of Watanabe, and I also use Shiba, in view of Sukegawa.

So if we consider Shiba in both of the prior art references, so Shiba, in view of Sukegawa, and Shiba, in view of Watanabe, as I indicate in my declaration, one skilled in the art will modify the common pad of the -- which is shown in Shiba to include the transparent conductive layer so that it can -- above it, so that it can gain the advantages of the corrosion protection -- protection from the corrosion that the transparent conductive layer offers. 04:42:08 04:42:45

In the pad region, this is where the metal is exposed, the underlying metal below the transparent conductive layer is exposed. And it is -- and is subject to corrosion. And the common pad 751 is far outside the sealant region, as shown in Figure 3, because you have the wiring 121 next to 751, and that wiring 121, which is before the sealant, is all under the passivation layer. So all that wiring is already protected by the passivation layer. 04:43:18 04:44:05

The only part of the wiring that will be exposed and subject to corrosion is the part of- -- is the part labeled 751, which is exposed through 04:44:34

the slit 243. That part will be modified in view of Sukegawa.

Someone with ordinary skill in the art will not be motivated to protect wirings that have already been protected by the second insulating film by adding additional piece of metals, such as ITO, the same way that they will do it in the terminal pad region. 04:45:08

And in view of Sukegawa -- sorry. Strike that. 04:45:26

In view of Watanabe, which addresses the issue of the gap spacing, the person with ordinary skill in the art will also understand that adding additional metal will create a bigger step in the gap region -- in the sealant region. 04:46:10

So you asked me whether there is it any teaching, suggestion or other specific motivation in Shiba that the transparent conductive layer should not extend to the second region defined in claim 54 of the '204 patent. And in my answer I said that someone with ordinary skill in the art based on the teaching of Shiba, in view of Watanabe and Sukegawa, will place the transparent conductive layer only in the terminal region in the common pad 751 and will not extend it into the second region under the 04:46:44 04:47:18

sealant, because you will not result in any additional advantages and may, rather, create a bigger step.

BY MR. MANZO:

Q Thank you. 04:47:50

If you were to look at claim 54 again, at line 23, I think, the claim talks about electrical contact. And at line 25 it talks about direct contact.

Do you see that? 04:50:24

A I see that.

Q Are those two the same to a person of ordinary skill in the art?

A A direct contact implies a direct physical contact, that the two layers touch each other. 04:51:53

An electrical contact can occur between two elements, even if they're not touching each other, in other words, even if they are not in direct contact. But if each touch a third element, third object, they can be in electrical contact without 04:52:18 being in direct contact by -- through this other material or object.

So in the case it says line 22, the second conductive line and the flexible printed circuit are in electrical contact through the transparent 04:52:46

conductive layer, that implies that the flexible printed circuit is not touching directly the second conductive line, but rather, in between there is another material and that other material is the transparent conductive layer. 04:53:07

So an electrical connection, which means that the layers have to be in the same potential and current can flow through them, can be established through the transparent conductive layer.

In the other section, the direct contact, it means that the two layers physically touching each other. 04:53:27

And we had a lengthy discussion yesterday about an electrical contact is established when you have the passage of current, and that will require some sort of an excitation source, some sort of a voltage difference, such as those provided by an external board through the flexible printed circuit. 04:54:09

Q Professor, if you have a television set, the kind that runs off of AC power rather than a battery, and it's plugged into the wall socket, would you say that the television set is not in electrical contact with the wall socket until the on/off switch is turned on on the TV set? 04:56:52

MR. GIBSON: Objection; form. 04:57:20

THE WITNESS: You have a television set and you have a wire, a cable, that is plugged to the socket on the wall --

BY MR. MANZO:

Q The power supply cord. 04:58:23

A The power supply cord.

Before you turn on the power switch, the television set will not consume any power. There will be no current flowing into the television set, no current will flow out of the wall to power any 04:58:43 electronics because the switch will prevent the flow of the current.

Q So does that mean that until the switch is turned on, the TV set is not in electrical contact with the wall socket? 04:59:13

MR. GIBSON: Objection; form.

THE WITNESS: The cable, which is plugged in, is physically attaching the external cable. A potential along the cable line is established to be the same as that of the -- of the outlet. And 04:59:49 somewhere there is a switch and that switch is off.

Now, from the streets and into the circuit of the television there is no electricity that has been sent. The cable is at the same voltage as the outlet, like 110, 20 volts, and then there is a 05:00:31

switch that is opened. And the circuit within the television apparatus is isolated.

And when you turn on the switch, electricity flows. And when you turn off -- and power is consumed. And when you turn off the switch, current stops to flow. 05:01:08

BY MR. MANZO:

Q So --

A But the means to flow the current in and out of the television set exists. 05:01:24

Q And --

A Whether -- it is controlled by the switch. You have the ability to flow current in and out of the television through the switch.

Yesterday we were discussing in the context of Sukegawa when you have a continuous passivation film, and I have explained that before the opening in the passivation film there is no ability to flow currents in or out because the whole system was coated with insulations, there was no, in this context, a magical switch that you can turn on or off, so I don't know what you're trying to lead -- where you're trying to lead with your line of questioning. 05:02:18 05:02:45

I am trying to be as explicit as possible 05:03:07

in my answers.

Q And we appreciate that, Professor.

Just going back to the TV set, you've talked about the circuits in the TV set.

Is the power cord of the TV set in electrical contact with the wall socket once it's plugged into the wall socket without regard to the state of the on/off switch in the TV set? 05:03:21

MR. GIBSON: Objection; form.

THE WITNESS: So if I understand your question well, you're asking me, the switch is off -- you asked me without regard to the state of the on/off switch. So if the switch is on, electricity flows to the TV set through the cable, so in that case everything is electrically connected, electricity flows. If the switch is off, that's what needs to be addressed. 05:04:13 05:04:40

If the switch is off, no electricity flows inside the TV set; however, at the moment you -- starting from the moment where the switch -- where the cable is not plugged. Okay? We now have a cable which is not plugged in the wall. Let's assume that the TV is also in the off position. And now we're plugging in the cable -- we're going to plug the cable. 05:05:16 05:05:41

The voltage on the two leads of the cable, the voltage difference is zero. There is no voltage potential difference on the volt -- on the cable that's not plugged to anything. It is a long cable with a zero volt across it. Two cables who equally 05:05:59
have zero volt across them, if they are made of the same material. They are not some weird effects, you may recall from physics, that if two metals are made of different materials, you may have other phenomena. 05:06:19

But in this case you have two copper wires that you have in the cable that is plugged into the wall, assuming the two plugs. If we measure the voltage difference before we plug them in, that voltage difference is zero. 05:06:34

Once we are plugged in and we have means to access the voltage difference between the two cables, we will see that there is a voltage difference between them. They both have obtained voltage that is supplied by the outlet. So the 05:06:52
cable became electrically connected the moment you plugged it in, into the TV wall, because the electricity flew, current flew and established a voltage difference between the two cables.

But from the switch inwards, the circuit is 05:07:15

isolated and no electricity can flow, no potential difference still exist inside the circuit, and that will continue until you press the on switch in the on state.

BY MR. MANZO: 05:07:40

Q Professor --

A Thank you.

In the morning we were discussing a hypothetical structure in Shiba.

Do you recall that? You were saying about 05:08:14 the presence of the dielectric layer 211 in between the two wirings -- the two layers of wiring 127? Do you recall that?

Q Yes. We were discussing dielectric and the wiring in 127, and we had a discussion about whether 05:08:39 there's dielectric there or not.

A Right.

And you allege that there may be a means that the two structure, the two layers will be formed that will physically attach each other 05:09:05 because the dielectric layer will not be there.

Do you recall that?

Q Yes.

A And I have asked you whether there is evidence, and you did not -- I did not recall you 05:09:20

showing me such evidence other than the allegations that that -- somehow it is possible. If I recall, I did not see evidence to point out that this dielectric layer somehow is removed.

Q Did you want to amend your answer? 05:09:43

A No. What I would like to do is provide you evidence that this layer is not removed, and I want to back that evidence from the statements within Shiba why that is not occurring. If you're interesting (sic) to obtain that evidence from 05:10:09 Shiba, I will tell you that this hypothetical structure has not been taught on Shiba. In contrast, Shiba teaches away from that hypothetical structure that you allege that may exist.

Q Where is that teaching? 05:10:30

A If we go to Shiba, column 7, line 45, it reads, "Since the wiring line 127 is constituted by a plurality of narrow lines as shown in Figure 6, the protective overcoat 241 and the gate dielectric 211 are directly connected to each other through the 05:11:11 gap between the narrow lines. As a result, there is a removal of the first wiring line 127 together with the sealing agent 113 is reduced. Accordingly, the degree of freedom of selecting material of the sealing agent 113, depending on the adhesion 05:11:36

capacity, can be increased."

In other words, this section --

Q That's the end of the quote?

A Yes.

Q Okay. Go ahead. 05:11:53

A I read from line 46 to line 54.

Q Thank you.

A In that section Shiba is teaching the value of maintaining the gate dielectric 211 in this region, and the benefit of that one, it provides 05:12:17 better adhesion, protection for the first wiring 127 and the overcoat 241.

So here Shiba says the gate dielectric 211 serves a function. And the hypothetical structures that you allege may exist will weaken the adhesion 05:12:54 of the overcoat and of the first wiring line 127 and, thus, will compromise the selection of the materials that could be used for the sealing agent 113.

Q Where does this paragraph talk about 05:13:42 adhesion? Oh, are you referring to line 34, adhesion capacity?

A Are we in the same column 7?

MR. MURPHY: 54.

BY MR. MANZO: 05:14:01

Q Oh, a 54. Sorry.

The last line of that paragraph, you mentioned adhesion capacity. Is that the part you're --

A Well, that's the adhesion capacity of the sealing agent, but let me explain. 05:14:11

You have some structure on the glass and now you're going to bond that glass to another piece of glass and you're going to be using this sealing agent 113. 05:14:34

Q Yes.

A But that process you may come down or you may move it or you may not place in the right location and then you have to remove it and reapply it again. 05:14:53

And as it reads in line 54, the risk or removal of the first wiring line 127 together with a sealing agent 113 is recused. This means that when you remove the sealing agent 113 to reposition the second glass in order to align the color filters 05:15:24 with the right pixels, you're running the risk of removing from the substrate the wiring 127 and the overcoat 241.

If the sealant adheres very well to 241 and 241 adheres to 127, if you remove the sealant, you 05:15:47

will tear those lines apart and you're causing a manufacturing defect.

241 is anchored to the substrate through the gate dielectric 111. If you are removing the dielectric 211, you create a bigger step for the overcoat 241 to go all the way down to the substrate. 05:16:13

Furthermore, you may undercut the wirings 127, and then will you start compromising how the wiring 127 adheres onto 211, because even portions around the edges of 127 may be exposed because the 211 may be undercut when you try to remove it. 05:16:35

So removal of 211 will create a lot of risks in weakening the way that the 241 and 127 adhere into the substrate and will make the placement of the counter substrate a very dangerous operation. 05:17:07

But if you leave it intact, and the process I said that someone with ordinary skill in the art will opt to do to create contacts only on top of the -- in selected areas on top of the underlying layer, you will not remove the layer 211 from that entire region and, yes, it will be -- the structure will not be compromised. 05:17:36

Q Thank you for that clarification. I think 05:18:02

we'll take a recess now, please.

THE VIDEOGRAPHER: Off the record at 5:18 p.m.

(Recess.)

THE VIDEOGRAPHER: Back on the record at 5:31 p.m. 05:18:17

BY MR. MANZO:

Q Professor, just to conclude, a little while ago you were talking about what happens if you need to move the counter substrate relative to the substrate. 05:31:52

Do you remember that?

A I was just explaining the passage from column 7.

Q Okay. And the question we want to ask you is with regard to the wiring that's under the sealant -- 05:32:02

A You mean 127?

Q Yes.

-- if that wiring -- strike that. 05:32:23

With regard to that wiring 127, is that wiring more likely or less likely to be ripped out, as you said, if it is indium tin oxide or metal?

MR. GIBSON: Object to the form.

THE WITNESS: As I explained earlier, there 05:32:56

is no reason why to form that wiring with 127. The indium tin oxide will result in a high resistance, so your question is a little bit not relevant because you will not form that wiring with indium tin oxide, it will be very resistive, it will serve no purpose. 05:33:30

BY MR. MANZO:

Q Well, hypothetically, if -- let's modify the question, then. So make it hypothetical so that in one case it is metal that is not covered with ITO and in the other case it is metal that is covered with ITO. 05:33:45

Is one more likely to be ripped out than the other when the counter substrate has to be moved relative to the substrate? 05:34:05

MR. GIBSON: Object to the form.

THE WITNESS: Even if, hypothetically, one includes ITO, based on your statement, that will still be under the protective overcoat 241.

The issue is not so much if you have or not have ITO, which I explained I see no reason to have ITO there, but the issue is whether you have or not have the gate dielectric 211. 05:34:36

As I explained, Shiba teaches away from removing the gate dielectric 211 from that region 05:35:01

because that will weaken the structure. And if you weaken the structure by removing the gate dielectric 211, whether you have or do not have the ITO, the structure has already been compromised and it will be very weak based on the approach you discussed the morning. 05:35:24

So I'm trying to say Shiba teaches a way of removing the gate dielectric 211 and Shiba acknowledges that ITO is a highly resistive material so you would not use ITO to create a wiring line that runs long distance. And Shiba acknowledges that the length of the first wiring line is very long because it has to distribute the power to the pads that in the opposing long side to the side where the power is supplied since the wiring line has to be low resistance. 05:35:56 05:36:20

In my testimony I have only described modifications in Shiba that will result in current flow transverse to the thickness of the Shiba -- sorry -- transverse to the thickness of indium tin oxide, hence the presence of the layer will not add resistance, because that layer is so thin. 05:37:34

But you're referring to a line that is very long. And I did not find the rationale anywhere in Shiba to add that line -- to the transparent 05:38:15

conductive layer in the first wiring line.

BY MR. MANZO:

Q Okay. Well, let me ask you hypothetically, assuming that the dielectric 211 is present in the lines and one wire is ITO, hypothetically, and another wire is another metal. 05:38:39

Is the sealant adhesion different for the two wires?

MR. GIBSON: Object to the form.

THE WITNESS: I don't think I can answer this hypothetical question because it all depend upon how you put the ITO, what stresses you have in the ITO layer and what is the passivation -- this protective overcoat 241, what is the gate dielectric on top of which the ITO will be deposited and what is the sticking coefficient or the adhesion between the ITO and these layers. 05:39:29 05:39:55

And then the same analysis has to be done for the other wire, which is made by another metal to convert them. 05:40:21

For example, you can put a wire down that it -- a metal down to form a wire, and if you have a lot of stresses built in that material during the deposition process or if the thermal expansion coefficient of that metal is such that when you are 05:40:42

putting all these other layers and you're hitting the structures, you build a lot of stresses in the structures, you may compromise the adhesion.

So it's not a straightforward answer. You can have each the same material that as you go through different deposition conditions and different annealing conditions, you can modify the stresses in the metal layer, and those ones may affect the way that layer interacts with the overcoat and the underlying coating, so there are a lot of unknowns in your hypothetical example. 05:41:03 05:41:36

Some layers, for example, aluminum and chromium, adhere very well. So there are layers that are known to have good adhesion. But even chromium, if you make it too thick, it will have a lot of stresses and the adhesion will compromise. So a lot of factors affecting that. 05:42:03

BY MR. MANZO:

Q Thank you.

What is the adhesive property of ITO relative to chromium and aluminum, which you did mention? 05:42:57

A You mean the sticking coefficient of -- I think it is called sticking coefficient of I- --

Q ITO? 05:43:32

A Yeah. I have to work from memory, I don't know exact numbers, but I know, for example, chromium is a very good adhesion to silicon dioxide layer, and most likely it will be better than ITO. I just don't remember exact numbers or relative rating of the two. I know some are better than others. 05:43:55

MR. MANZO: Thank you, Professor. We have no further questions.

MR. GIBSON: I do not have any questions. 05:44:19

THE VIDEOGRAPHER: We are off the record at 5:44 p.m. This concludes today's testimony given by Dr. Hatalis. The total number of media was 3 and will be retained by Veritext LLC.

(TIME NOTED: 5:44 p.m.)

I, MILTIADIS HATALIS, PH.D., do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made any corrections as appear noted, in ink, initialed by me, or attached hereto; that my testimony as contained herein, as corrected, is true and correct.

EXECUTED this _____day of _____, 2013, at _____, _____.
(City) (State)

_____
MILTIADIS HATALIS, PH.D.
Volume I

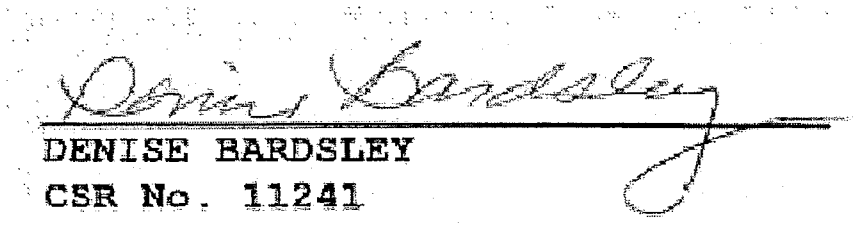
I, the undersigned, a Certified Shorthand Reporter of the State of California, do hereby certify:

That the foregoing proceedings were taken before me at the time and place herein set forth; that any witnesses in the foregoing proceedings, prior to testifying, were placed under oath; that a true and correct record of the proceedings was made by me using machine shorthand which was thereafter transcribed under my direction; further, that the foregoing is an accurate transcription thereof.

I further certify that I am neither financially interested in the action nor a relative or employee of any attorney of any of the parties.

IN WITNESS WHEREOF, I have this date subscribed my name.

Dated: 8 July 2013



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|---|---|---|---|
| **03:32:56** 114:20 | **03:56:03** 123:15 | **04:39:44** 132:10 | **05:07:40** 141:5 |
| **03:33:23** 114:25 | **03:56:41** 123:20 | **04:40:05** 132:15 | **05:08:14** 141:10 |
| **03:34:12** 115:5 | **03:56:59** 123:25 | **04:40:44** 132:20 | **05:08:39** 141:15 |
| **03:34:38** 115:10 | **03:57:18** 124:5 | **04:41:23** 132:25 | **05:09:05** 141:20 |
| **03:35:42** 115:15 | **04:11:32** 124:10 | **04:42:08** 133:5 | **05:09:20** 141:25 |
| **03:36:19** 115:20 | **04:12:17** 124:15 | **04:42:45** 133:10 | **05:09:43** 142:5 |
| **03:36:56** 115:25 | **04:13:36** 124:20 | **04:43:18** 133:15 | **05:10:09** 142:10 |
| **03:38:18** 116:5 | **04:14:11** 124:25 | **04:44:05** 133:20 | **05:10:30** 142:15 |
| **03:39:04** 116:10 | **04:15:01** 125:5 | **04:44:34** 133:25 | **05:11:11** 142:20 |
| **03:39:35** 116:15 | **04:16:22** 125:10 | **04:45:08** 134:5 | **05:11:36** 142:25 |
| **03:40:01** 116:20 | **04:16:55** 125:15 | **04:45:26** 134:10 | **05:11:53** 143:5 |
| **03:41:31** 116:25 | **04:17:31** 125:20 | **04:46:10** 134:15 | **05:12:17** 143:10 |
| **03:41:56** 117:5 | **04:17:58** 125:25 | **04:46:44** 134:20 | **05:12:54** 143:15 |
| **03:43:10** 117:10 | **04:18:20** 126:5 | **04:47:18** 134:25 | **05:13:42** 143:20 |
| **03:43:37** 117:15 | **04:18:39** 126:10 | **04:47:50** 135:5 | **05:14:01** 143:25 |
| **03:43:46** 117:20 | **04:18:59** 126:15 | **04:50:24** 135:10 | **05:14:11** 144:5 |
| **03:44:08** 117:25 | **04:19:15** 126:20 | **04:51:53** 135:15 | **05:14:34** 144:10 |
| **03:44:25** 118:5 | **04:19:23** 126:25 | **04:52:18** 135:20 | **05:14:53** 144:15 |
| **03:44:46** 118:10 | **04:19:50** 127:5 | **04:52:46** 135:25 | **05:15:24** 144:20 |
| **03:45:09** 118:15 | **04:20:07** 127:10 | **04:53:07** 136:5 | **05:15:47** 144:25 |
| **03:45:37** 118:20 | **04:20:42** 127:15 | **04:53:27** 136:10 | **05:16:13** 145:5 |
| **03:45:58** 118:25 | **04:21:29** 127:20 | **04:54:09** 136:15 | **05:16:35** 145:10 |
| **03:46:18** 119:5 | **04:21:47** 127:25 | **04:56:52** 136:20 | **05:17:07** 145:15 |
| **03:46:38** 119:10 | **04:24:27** 128:5 | **04:57:20** 136:25 | **05:17:36** 145:20 |
| **03:46:55** 119:15 | **04:25:36** 128:10 | **04:58:23** 137:5 | **05:18:02** 145:25 |
| **03:47:24** 119:20 | **04:26:16** 128:15 | **04:58:43** 137:10 | **05:18:17** 146:5 |
| **03:47:58** 119:25 | **04:26:38** 128:20 | **04:59:13** 137:15 | **05:31:52** 146:10 |
| **03:48:24** 120:5 | **04:29:13** 128:25 | **04:59:49** 137:20 | **05:32:02** 146:15 |
| **03:48:38** 120:10 | **04:29:45** 129:5 | **05:00:31** 137:25 | **05:32:23** 146:20 |
| **03:49:05** 120:15 | **04:30:01** 129:10 | **05:01:08** 138:5 | **05:32:56** 146:25 |
| **03:49:41** 120:20 | **04:31:07** 129:15 | **05:01:24** 138:10 | **05:33:30** 147:5 |
| **03:50:05** 120:25 | **04:31:49** 129:20 | **05:02:18** 138:15 | **05:33:45** 147:10 |
| **03:50:24** 121:5 | **04:32:11** 129:25 | **05:02:45** 138:20 | **05:34:05** 147:15 |
| **03:50:38** 121:10 | **04:32:31** 130:5 | **05:03:07** 138:25 | **05:34:36** 147:20 |
| **03:50:56** 121:15 | **04:33:28** 130:10 | **05:03:21** 139:5 | **05:35:01** 147:25 |
| **03:51:17** 121:20 | **04:33:49** 130:15 | **05:04:13** 139:10 | **05:35:24** 148:5 |
| **03:52:13** 121:25 | **04:34:11** 130:20 | **05:04:40** 139:15 | **05:35:56** 148:10 |
| **03:52:38** 122:5 | **04:35:13** 130:25 | **05:05:16** 139:20 | **05:36:20** 148:15 |
| **03:53:04** 122:10 | **04:35:30** 131:5 | **05:05:41** 139:25 | **05:37:34** 148:20 |
| **03:53:27** 122:15 | **04:36:00** 131:10 | **05:05:59** 140:5 | **05:38:15** 148:25 |
| **03:54:00** 122:20 | **04:36:27** 131:15 | **05:06:19** 140:10 | **05:38:39** 149:5 |
| **03:54:24** 122:25 | **04:37:32** 131:20 | **05:06:34** 140:15 | **05:39:29** 149:10 |
| **03:55:02** 123:5 | **04:38:07** 131:25 | **05:06:52** 140:20 | **05:39:55** 149:15 |
| **03:55:44** 123:10 | **04:38:22** 132:5 | **05:07:15** 140:25 | **05:40:21** 149:20 |

**e**