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Advanced Multilayer Amorphous Silicon Thin-Film Transistor Structure: Film Thickness Effect on Its Electrical Performance and Contact Resistance

Alex KUO, Tae Kyung WON[1], and Jerzy KANICKI*

Organic and Molecular Electronic Laboratory, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109, U.S.A.
[1]*Applied Komatsu Technology America Inc., Santa Clara, CA 95054, U.S.A.*

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We report the intrinsic and extrinsic electrical characteristics of advanced multilayer amorphous silicon (a-Si:H) thin-film transistor (TFT) with dual amorphous silicon nitride (a-SiN_X:H) and a-Si:H layers. The thickness effect of the high electronic quality a-Si:H film on the transistor's electrical property was investigated; with increasing film thickness, both field-effect mobility and subthreshold swing show improvement and the threshold voltage remain unchanged. However, the contact resistance increases with the a-Si:H film thickness. Using the two-step plasma enhanced chemical vapor deposition process, we fabricated TFT's with acceptable field-effect mobility ($\sim 1\,cm^2\,V^{-1}\,s^{-1}$) and threshold voltage ($<1.5\,V$) with enhanced throughput. [DOI: 10.1143/JJAP.47.3362]

KEYWORDS: amorphous silicon thin-film transistor, dual layer, thickness effect, contact resistance

1. Introduction

As the active-matrix liquid crystal display (AM-LCD) industry begins to introduce large-size and high-pixel-density displays, the demand for a high performance amorphous silicon thin-film transistor mounts. In order for the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) to remain competitive in the flat-panel display industry, it is necessary to realize transistors with a high field-effect mobility and a low threshold voltage while being able to be fabricated at a high deposition rate.[1)] These qualities allow the possibility of manufacturing large displays with low power consumption at relatively low costs. Fabricating high performance a-Si:H TFT requires a high electronic quality a-Si:H film, as the electrical characteristics of a TFT is intimately related the electronic quality of the a-Si:H film.[2)] Even though a high electronic quality film can be achieved by lowering its plasma-enhanced chemical vapor deposition (PECVD) rate, doing so increases the overall device fabrication time. In the AM-LCD industry, the inverted staggered back-channel-etched type transistor structure is preferred over the tri-layer type transistor structure because of its reduced photolithography steps and improved source/drain contact quality.[3)] This structure requires the deposition of a thicker amorphous silicon film for better control of the back channel etch step.[4)] However, a thicker amorphous silicon film for TFT means longer deposition time, which also leads to a lower production output and higher overall costs for the AM-LCD industry.[5)] The PECVD time can be shortened by increasing the deposition rate of the film, but doing so degrades the mobility and threshold voltage of the transistor.[6)] Similarly, the gate insulator amorphous silicon nitride (a-SiN_X:H) should exceed 4000 Å to reduce the gate leakage. Also its PECVD rate needs to be low in order for the a-Si:H TFT to have a high electronic quality a-SiN_X:H/a-Si:H interface for optimum threshold voltage, subthreshold swing, and electrical stability.[7)] It is therefore desirable to search for a compromise between device electrical performance and production throughput by depositing thick a-SiN_X:H and a-Si:H films in the shortest possible time without degrading the overall electrical characteristics of the a-Si:H TFT. One potential solution is depositing two amorphous silicon films as the active layers of the TFT: a thin layer of a low deposition rate film near the gate insulator interface in order to obtain high electronic quality a-Si:H film near the electron conduction channel, and a thick layer of high deposition rate film in the back channel to be used as the sacrificial layer during the etch back process. The a-SiN_X:H deposition is also separated into a two-step process: a thin layer of low deposition rate film near the high electronic quality a-Si:H film for optimum electrical performance and stability, and a thick layer of high deposition rate film near the gate metal to reduce gate leakage current.

The concept of double a-Si:H layer structure for TFT was first proposed by Takeuchi and Katoh for the purpose of reducing a-Si:H TFT photo-response.[8,9)] Characteristic of dual amorphous silicon TFT was explored further by Kashiro *et al.*, and it was concluded that the field-effect mobility is highly sensitive, and linearly proportional (up to 15 nm), to the thickness of the high electronic quality a-Si:H layer.[10)] A reduction in the thickness of the high quality film allows the defect states from the low quality film to interfere with the band bending at the a-SiN_X:H/a-Si:H interface, which causes the TFT's mobility to decrease. Tsai *et al.* investigated the effect of a low electronic quality film deposition rate on the overall electrical performance of the a-Si:H TFT.[11)] and concluded that with the increasing deposition rate the TFT's field-effect mobility decreases for the same reasoning as proposed by Kashiro. From these results it is clear that dual a-Si:H layer TFT's electrical performance can suffer due to the inclusion of the low quality film away from the a-SiN_X:H/a-Si:H interface. However, previous studies report only on the extrinsic characteristics of the a-Si:H TFT, which do not take source/drain contact resistances into consideration; yet it is well known that the presence of significant contact resistance can mask the true electrical characteristics, or the intrinsic characteristics, of an a-Si:H TFT.[12)] Moreover it is not clear how the film thickness of a high quality a-Si:H affects the intrinsic and extrinsic properties of the advanced multilayer a-Si:H TFT structure. Our present work analyzes in some

*E-mail address: kanicki@umich.edu

details the advanced multilayer a-Si:H TFT with dual a-Si:H and dual a-SiN_X:H layers. We extract the electrical behaviors of the a-Si:H TFT and analyze the effect of a high quality amorphous silicon film thickness on the overall transistor performance by evaluating its intrinsic and extrinsic electrical characteristics. Based on our experimental results, we can i) quantify the effect of a high electronic quality a-Si:H thickness on the transistor's field-effect mobility, threshold voltage, subthreshold swing, and contact resistance, and ii) identify a minimum thickness of a high electronic quality a-Si:H layer required for the TFT to exhibit promising device electrical performance without unnecessarily extending the PECVD time. To our best knowledge this study is the first full analysis on the thickness effect of a high electronic quality amorphous silicon film, which include both the intrinsic and extrinsic properties of the transistor, on the dual a-Si:H and a-SiN_X:H layers transistors.

2. Experimental Methods

We fabricated back channel etched type inverted staggered transistor[13] with patterned chromium gate (2000 Å thick) consisting of two layers of a-SiN_X:H and two layers of a-Si:H (Fig. 1): PECVD was used to deposit 3500 Å of nitrogen-rich hydrogenated a-SiN_X:H at ~1800 Å/min (G2), 500 Å of a-SiN_X:H deposited at ~1000 Å/min (G1), 100–600 Å of a-Si:H deposited at ~600 Å/min (A1), 1100–1600 Å of a-Si:H deposited at ~1200 Å/min (A2), and 700 Å of phosphorous doped amorphous silicon (n+ a-Si:H). The active island was dry-etched ($SF_6 : Cl_2 : O_2 : He$ in 6 : 24 : 20 : 5 ratio) using a LAM 9400 TCP-RIE. Source and drain metallization includes the deposition and definition of sputtered molybdenum. Since the phosphorous from the n+ layer diffuses into the amorphous silicon film in the back channel etch TFT, it is necessary to perform dry over-etch to remove a fraction of the amorphous silicon film in order to reduce the leakage current between the source and drain;[14] we dry-etched ($HBr : Cl_2$ in 1 : 1 ratio) 700 Å of A2 in the channel region of the transistor using the LAM 9400 TCP-RIE. All patterning steps were performed using contact photolithography via a MA-6 mask aligner. The bi-layer a-SiN_X:H surface roughness (RMS value) above the gate dielectric is about 1.1 nm. Both films have slightly different film stoichiometry, but are both N-rich (N/Si > 1.3); the Si–H content in the gate dielectric deposited at the lower rate is rather small (<0.5%). Total hydrogen content in the silicon nitride deposited at the higher rate (~36 ± 4%) is significantly larger in comparison to the film deposited at the lower rate (~28.5 ± 1.5%). The Tauc optical gap for the film deposited at higher and lower rates is about 4.6 and 5.2 eV, respectively. Table I shows the plates fabricated with different A1 and A2 a-Si:H thicknesses, denoted from here on as t_{A1} and t_{A2} respectively. It is important for readers to remember that the t_{A2} values presented are the deposited thicknesses, not the final A2 thicknesses in the channel region of the TFTs after the back channel etch. Electrical measurements were conducted using HP 4156 at the room temperature, and the detail of experimental techniques has been discussed elsewhere.[13]

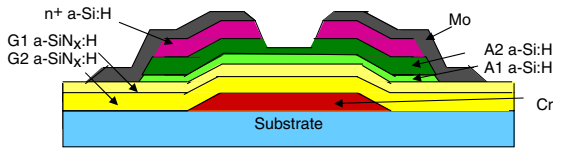

Fig. 1. (Color online) Schematic cross-section of a-Si:H TFT used in this work.

Table I. A1 and A2 a-Si:H film thicknesses of the substrates used in this study.

Plate ID	t_{A1} (A)	t_{A2} (A)	
		As deposited	Channel region
Var-1	100	1600	900
Var-2	200	1500	800
Var-3	300	1400	700
Var-4	400	1300	600
Var-5	500	1200	500
Var-6	600	1100	400

3. Parameter Extraction Methodology

Since the goal of this study focuses on the change in a-Si:H TFT performance with respect to t_{A1}, it is imperative that we develop accurate parameter extraction techniques that represent the true TFT electrical behaviors. Changes observed, if any, should be solely due to the differences caused by electrical properties change originating from varying t_{A1}, not artificial effects contributed by the parameter extraction method. We use two different methods of extrinsic parameter extraction, which does not take contact resistance of a-Si:H TFT into consideration, to minimize the possibility of introducing artifacts: linear[15,16] and conductance[17] methods. When extracting the a-Si:H TFT parameter via the linear method, a line fits the experimental data points of the I_D–V_{GS}, or transfer, characteristic in the linear regime (Fig. 2) or the $I_D^{1/2}$–V_{GS} characteristic in the saturation regime (Fig. 3); the data range selected is between 10–90% of the maximum drain current. The fitting line represents metal–oxide–semiconductor field-effect transistor (MOSFET) square law equations:

$$I_{D\text{-LIN}} = \frac{W}{L} C_{INS} \mu_{FE1\text{-LIN}} (V_{GS} - V_{T1\text{-LIN}}) V_{DS\text{-LIN}}, \quad (1)$$

$$I_{D\text{-SAT}}^{1/2} = \left(\frac{W}{2L} C_{INS} \mu_{FE1\text{-SAT}}\right)^{1/2} (V_{GS} - V_{T1\text{-SAT}}), \quad (2)$$

where W, L, and C_{INS} symbolize the a-Si:H TFT channel width, length, and gate insulator capacitance, respectively. Field-effect mobility values in the linear and saturation regime are denoted as $\mu_{FE1\text{-LIN}}$ and $\mu_{FE1\text{-SAT}}$; similarly threshold voltage values in each regime of operation are represented by $V_{T1\text{-LIN}}$ and $V_{T1\text{-SAT}}$. The symbols V_{GS} and $V_{DS\text{-LIN}}$ are the gate and drain biases with respect to the source terminal of the TFT. From the equations above it is clear that from the slope of the fitting line to the transfer characteristic we can extract the field-effect mobility values, and the x-intercept yields the threshold voltage.

The second method of parameter extraction is based on the conductance of the a-Si:H TFT. We begin by defining the linear regime channel conductance ($\sigma_{CH\text{-LIN}}$) of the device from the square law current equation:

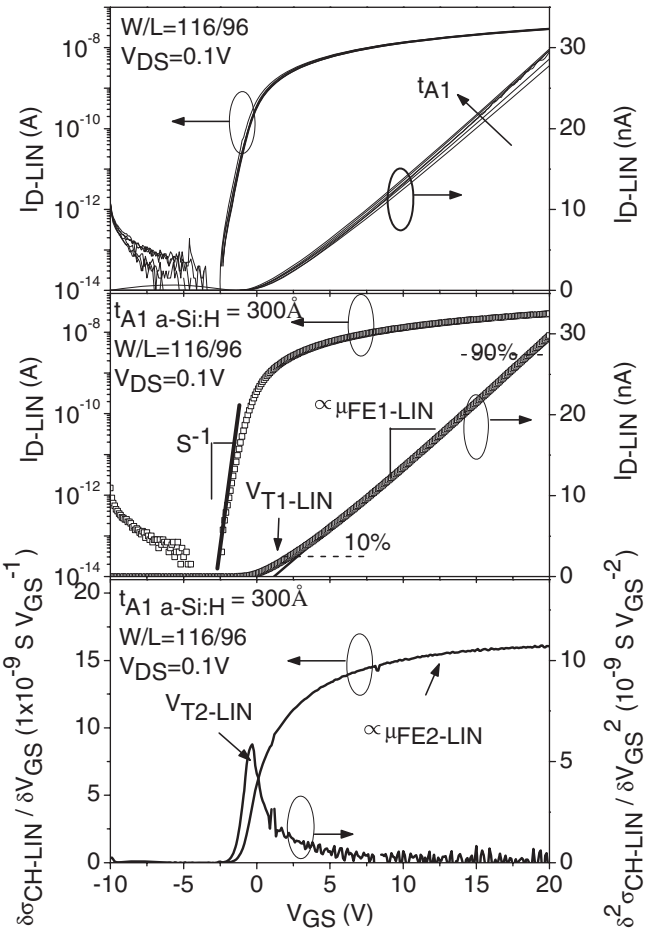

Fig. 2. Linear regime transfer characteristics of the a-Si:H TFTs with different A1 and A2 a-Si:H thicknesses (top). Experimental data points are intentionally displayed as thin lines to show the variations among different transistors. Demonstration of the parameter extraction using the linear method for TFTs with t_{A1} of 300 Å is also included: figures represent data points collected and lines represent fitting equations. Demonstration of the parameter extraction using the conductance method: calculated $\delta\sigma_{\text{CH-LIN}}/\delta V_{\text{GS}}$ and $\delta^2\sigma_{\text{CH-LIN}}/\delta V_{\text{GS}}^2$ curves for TFTs (bottom) used in this experiment.

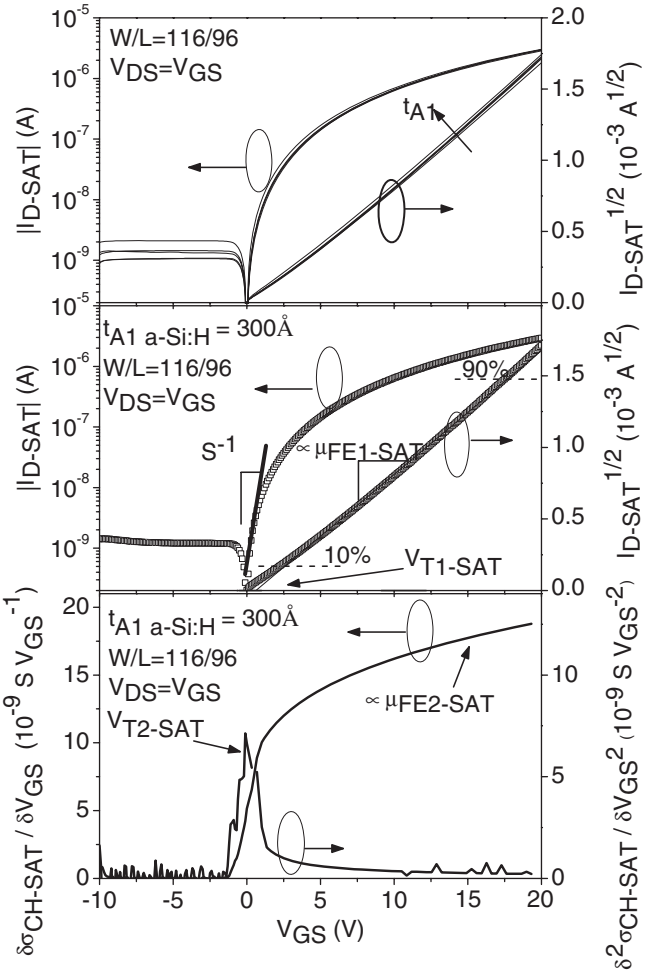

Fig. 3. Saturation regime transfer characteristics of the a-Si:H TFTs with different A1 and A2 a-Si:H thicknesses (top). Experimental data points are intentionally displayed as thin lines to show the variations among different transistors. Demonstration of the parameter extraction using the linear method for TFTs with t_{A1} of 300 Å: figures represent data points collected and lines represent fitting equations. Demonstration of the parameter extraction using the conductance method: calculated $\delta\sigma_{\text{CH-SAT}}/\delta V_{\text{GS}}$ and $\delta^2\sigma_{\text{CH-SAT}}/\delta V_{\text{GS}}^2$ curves for TFTs (bottom) used in this experiment.

$$I_{\text{D-LIN}} = \frac{W}{L} C_{\text{INS}} \mu_{\text{FE2-LIN}} (V_{\text{GS}} - V_{\text{T1-LIN}}) V_{\text{DS-LIN}}, \quad (3)$$

$$\sigma_{\text{CH-LIN}} \equiv \frac{\delta I_{\text{D-LIN}}}{\delta V_{\text{DS-LIN}}} = \frac{W}{L} C_{\text{INS}} \mu_{\text{FE2-LIN}} (V_{\text{GS}} - V_{\text{T1-LIN}}), \quad (4)$$

where $\mu_{\text{FE2-LIN}}$ is the linear regime field-effect mobility. To obtain the field-effect mobility we take derivative of the channel conductance with respect to the gate bias (Fig. 2):

$$\frac{\delta\sigma_{\text{CH-LIN}}}{\delta V_{\text{GS}}} = \frac{W}{L} C_{\text{INS}} \mu_{\text{FE2-LIN}}. \quad (5)$$

It should be clarified that two separate field effect mobility notations are used for the same square law equation to distinguish the difference in extraction method: $\mu_{\text{FE1-LIN}}$ in eq. (1) is a constant value with respect to V_{GS} and $\mu_{\text{FE2-LIN}}$ from eq. (5) varies with gate bias. Threshold voltage extraction from the conductance method ($V_{\text{T2-LIN}}$) is done by taking derivative of eq. (5) with respect to V_{GS}, and defining the maximum value as the threshold voltage. This choice is based on the fact that channel conductance changes with gate bias, as shown in Fig. 2. By defining threshold voltage as the maximum value on the $\delta^2\sigma_{\text{CH-LIN}}/\delta V_{\text{GS}}^2$ plot,

we incorporate a physical origin to the threshold voltage parameter as the specific point where the maximum change in channel conductance with gate bias occurs.

Field-effect mobility extraction in the saturation regime ($\mu_{\text{FE2-SAT}}$) also begins with the square law current equation:

$$I_{\text{D-SAT}} = \frac{W}{2L} C_{\text{INS}} \mu_{\text{FE2-SAT}} (V_{\text{GS}} - V_{\text{T1-SAT}})^2. \quad (6)$$

Since $V_{\text{DS-SAT}} = V_{\text{GS}} - V_{\text{T1-SAT}}$ and $dV_{\text{DS-SAT}} = dV_{\text{GS}}$, the channel conductance in the saturation regime is

$$\sigma_{\text{CH-SAT}} \equiv \frac{\delta I_{\text{D-SAT}}}{\delta V_{\text{DS-SAT}}} = \frac{W}{L} C_{\text{INS}} \mu_{\text{FE2-SAT}} (V_{\text{GS}} - V_{\text{T-SAT}}), \quad (7)$$

and the change in channel conductance with respect to the gate bias is

$$\frac{\delta\sigma_{\text{CH-SAT}}}{\delta V_{\text{GS}}} = \frac{W}{L} C_{\text{INS}} \mu_{\text{FE2-SAT}}. \quad (8)$$

Figure 3 shows the extractions of field-effect mobility from the $\delta\sigma_{\text{CH-SAT}}/\delta V_{\text{GS}}$ plot and threshold voltage ($V_{\text{T-SAT}}$) from

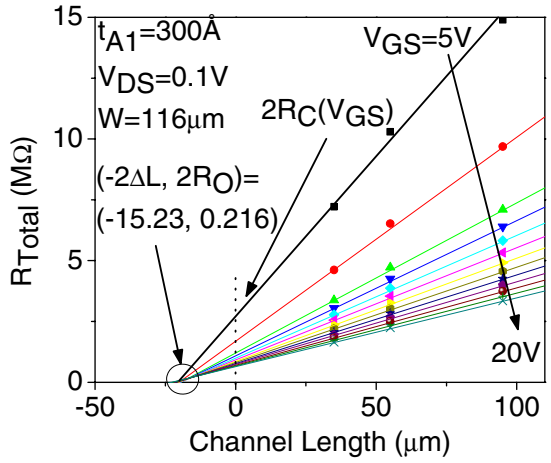

Fig. 4. (Color online) Example of the R_{TOTAL}, r_{CH}, $R_C(V_{GS})$, R_0, and ΔL values extraction using TLM.

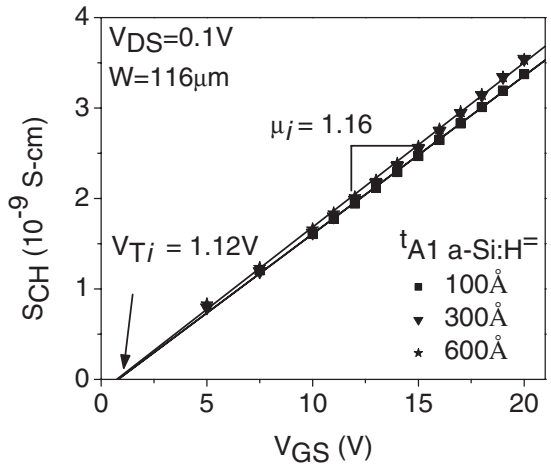

Fig. 5. Extraction of a-Si:H TFTs (t_{A1} = 100, 300, 600 Å) intrinsic mobility and threshold voltage by using channel conductivity versus gate voltage plot: symbols and lines represent experimental data and the best-fit line, respectively. Values of intrinsic mobility and threshold voltage shown belong to TFT with t_{A1} of 600 Å.

the $\delta^2\sigma_{CH\text{-}SAT}/\delta V_{GS}^2$ plot. Both $\mu_{FE2\text{-}LIN}$ and $\mu_{FE2\text{-}SAT}$ values are extracted from the conductance curves at the maximum conductance value; in both cases maximum values occur at $V_{GS} = 20$ V. Subthreshold swings for the linear and saturation regimes of operation are defined as the inverse values of the steepest slopes of the respective I_D–V_{GS} semi-log plots.

For the intrinsic parameter extraction, we use the transmission line method (TLM) described by Kanicki *et al.*[18] Detail description of the method will not be repeated here; instead we show examples of the data obtained by utilizing TLM in Figs. 4 and 5, plus the equation for total resistance (R_T) of a-Si:H TFT during the linear regime of operation:[18]

$$\begin{aligned} R_T &= \frac{V_{DS}}{I_D} \\ &= r_{CH}(V_{GS})L + 2R_C(V_{GS}) \\ &= \frac{L}{W\mu_i C_{INS}(V_{GS} - V_{T\text{-}i})} + 2R_C(V_{GS}). \end{aligned} \tag{9}$$

In eq. (9) $r_{CH}(V_{GS})$, $R_C(V_{GS})$, μ_i, and $V_{T\text{-}i}$ represent the channel resistivity, total contact resistance, intrinsic mobility, and intrinsic threshold voltage, respectively. From Fig. 4, we can obtain the values of $r_{CH}(V_{GS})$ and $R_C(V_{GS})$ for a given gate voltage from the slope and the y-intercept, respectively, of a fitted line for the total resistances of the transistors with different channel lengths. The minimum contact resistance (R_0) and the effective channel length change (ΔL) are extracted from the intersection of all the R_T fitted lines. Channel conductivity, $S_{CH}(V_{GS})$, is equal to the inverse value of the channel resistivity. One point worth noting is that due to the geometry of the TFT near its source and drain contacts, the actual transistor channel length is not the masked channel length L, but $L + \Delta L$. From plotting the channel conductance values with respect to the gate bias, and performing a linear fit to the data points, we can extract the intrinsic mobility and threshold voltage values respectively from the slope and the x-intercept of the best-fit line (Fig. 5).

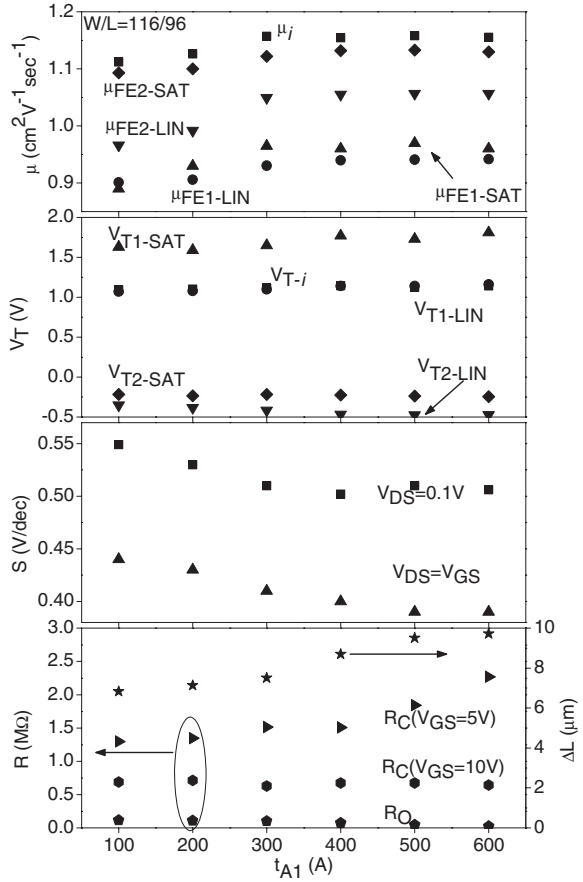

Fig. 6. Intrinsic mobility and threshold voltage, and linear and saturation regimes field-effect mobility, threshold voltage, subthreshold swing, contact resistances, and channel length deviation values for a-Si:H TFTs with different A1 thicknesses investigated in this work.

4. Results and Discussion

From the linear regime transfer characteristics of the a-Si:H TFTs shown in Fig. 2 (top), there is a slight increase in drain current with t_{A1}. The same trend can be seen from the saturation regime transfer characteristics from Fig. 3 (top). Changes in extrinsic threshold voltage and subthreshold swing, however, are inconspicuous from observing the I–V characteristics. Figure 4 shows the values of $R_C(V_{GS})$, R_0, $S_{CH}(V_{GS})$, and ΔL of the a-Si:H TFT with t_{A1} = 300 Å. Both

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