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Paper 11
Entered: April 30, 2013

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INNOLUX CORPORATION[1]
Petitioner

v.

SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
Patent Owner

Case IPR2013-00065(SCM)
Patent 7,923,311 B2

Before SALLY C. MEDLEY, KARL D. EASTHOM, and KEVIN F. TURNER, *Administrative Patent Judges.*

TURNER, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

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[1] *See* Paper No. 10 (Petitioner's Mandatory Notice updating the Board as to its name change from "Chi Mei Innolux Corporation," which Petitioner also refers to as "formerly Cheimei Innolux Corporation," to "Innolux Corporation" as the real party-in-interest in this proceeding). The caption, as it appears above, will be employed in all future correspondence.

I. BACKGROUND

Petitioner, Chimei Innolux Corp. ("CMI")[2], filed a Petition[3] to institute an *inter partes* review of claims 23, 24, 26-40, 42-44, 46, 49, 50, 53, and 54 of U.S. Patent 7,923,311 B2 ("the '311 Patent")[4] owned by Semiconductor Energy Laboratory Co., Ltd. ("SEL"). *See* 35 U.S.C. § 311. In response, Patent Owner, SEL, filed a Preliminary Response.[5] The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a):

> THRESHOLD – The Director may not authorize an inter partes review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

Pursuant to the defined threshold under 35 U.S.C. § 314(a), the Board institutes an *inter partes* review of claims 23, 24, 26-40, 42-44, 46, 49, 50, 53, and 54 of the '311 Patent.[6]

A. The '311Patent

The '311 Patent describes a thin film transistor (TFT) and a method for forming the same (EX 1001, col. 1, ll. 7-10). According to the '311 Patent, numerous problems were associated with prior art methods of crystalizing

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[2] While we acknowledge the name change of Petitioner (*see* footnote 1), we continue to refer to that party as "CMI" for purposes of this Decision.
[3] *Petition for Inter Partes Review of U.S. Patent No. 7,923,311 Under 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 Et Seq.* (Nov. 26, 2012).
[4] Based on a terminal disclaimer filed during the prosecution of the application for the '311 Patent, the patent has now expired (Pet. 5, 8).
[5] *Patent Owner Preliminary Response Under 37 C.F.R. § 42.107* (Feb.2 6, 2013).
[6] A second request for *inter partes* review of claims 9-11, 15, 17-19, 48, 51, and 52 of the '311 Patent was filed concurrently with the instant Petition (IPR 2013-00064), where a Decision on that petition is being sent out concurrently.

amorphous silicon layers used in devices (*Id*. at col. 1, ll. 14-44). According to the disclosure of the '311 Patent, the later crystallization by laser irradiation of semiconductor materials in the channel region and the activation of the ohmic contact region of the source and drain provides improvements in electrical conductivity and avoids the prior art problems (*Id*. at col. 1, l. 52 - col. 2, l. 4).

Figures 3(D) and 3(F), which follow, illustrate portions of the method used to fabricate the TFT:

FIG.3(D)

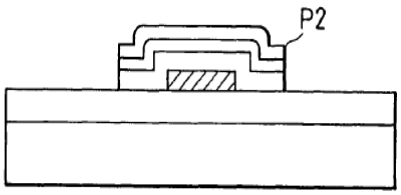
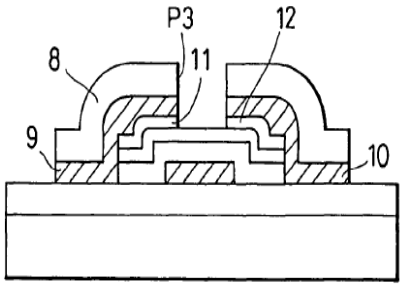


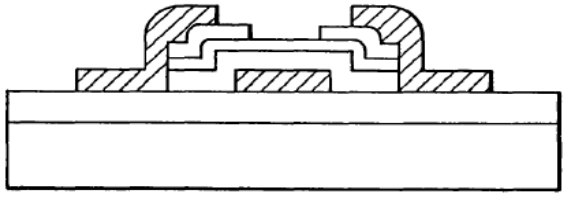
FIG.3(F)



A metal layer is deposited on a silicon dioxide layer on a glass substrate and patterned to form a gate electrode, with a gate insulating film, a first semiconductor film, and an N-type semiconductor film deposited thereon (*Id*. at col. 5, l. 55 – col. 6, l. 43). A photoresist (P2) is used to pattern those layers to form a TFT island (*Id*. at col. 6, ll. 44-52; Fig. 3(D)). A conductive layer is deposited on the TFT island, with a photoresist (8, P3) applied thereon (*Id*. at col. 6, ll. 53-62; Fig. 3(F)). Source and drain electrodes (9 & 10) are formed by etching of the conductive layer, using the photoresist (P3), with source and drain regions (11 & 12) being formed from the N-type semiconductor film by the same etching process (*Id*.).

In one embodiment, a wet etching process may be applied to the structure as illustrated in Figure 3(F) so that the distance between the source and drain regions (11 & 12), in the channel region, is less than the distance between the source and drain electrodes (9 & 10), as illustrated in Figure 3(G):

FIG.3(G)



Thereafter, a passivation film is applied to cover the source and drain electrodes, the source and drain regions, and the channel formation region (*Id*. at col. 7, ll. 1-9; Fig. 3(H)). In addition, pixel electrodes may be formed over the passivation film, which may form an electrical connection to the source or drain electrode (*Id*. at col. 7, ll. 50-53).

B. Illustrative Claim

Illustrative claim 23 follows, with emphasis applied:

> 23. A method of manufacturing a display device including a thin film transistor over a glass substrate, the method comprising the steps of:
>
> forming a resist on a conductive layer wherein said conductive layer is formed on an N-type semiconductor film, said N-type semiconductor film is formed on a first semiconductor film, and said first semiconductor film is formed over a gate electrode with a gate insulating film comprising silicon nitride interposed therebetween;
>
> etching a portion of said conductive layer to form source and drain electrodes using said resist;
>
> etching a portion of said N-type semiconductor film to form source and drain regions without removing said resist wherein a channel forming region is formed in said first semiconductor film between said source and drain regions; and

forming a passivation film over at least said source and drain electrodes and said channel forming region after removing said resist,

wherein each of the source and drain regions has a bottom surface in contact with the first semiconductor film, each of the source and drain electrodes has a bottom surface in contact with corresponding one of the source and drain regions, and the conductive layer is overetched using said resist so that a distance between opposed ends of the bottom surfaces of the source and drain electrodes is larger than a distance between opposed ends of the bottom surfaces of the source and drain regions.

C. Related Proceedings

The '311 Patent is involved with several other related CMI patents in several other *inter partes* review filings before the PTAB, and also in infringement litigation styled as *Semiconductor Energy Laboratory Co., Ltd. v. Chimei Innolux Corp., et al.*, SACV12-0021-JST (C.D. Cal.) (filed Jan. 5, 2012) [hereinafter the CMI Case]. (*See* Pet. 1-2; Prelim. Resp. 4). Defendants in that case filed a motion on October 22, 2012 to stay that litigation pending the outcome of this instant proceeding (EX 2002), where that request for a stay was granted on December 19, 2012.

CMI also discusses the prosecution, litigation, and reexamination of related U.S. Patent No. 6,756,258 (EX 1010, "the '258 Patent"), where the '258 Patent claims priority to the same Japanese patent application (JP 03-174541) that the instant '311 Patent does (Pet. 9).

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