Attorney Docket No. 0756-8108

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	
Hongyong ZHANG et al.	
Serial No.: 11/898,833	
Filed:	September 17, 2007
For:	ELECTRO-OPTICAL DEVICE AND
	THIN FILM TRANSISTOR AND
	METHOD FOR FORMING THE
	SAME

) Confirmation No.: 4620

) Examiner: Michael Lebentritt

) Group Art Unit: 2829

TERMINAL DISCLAIMER

Honorable Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

DOCKE

I, Dr. Shunpei Yamazaki, having a place of business at Semiconductor Energy Laboratory Co., Ltd., 398 Hase Atsugi-shi, Kanagawa-ken, 243 Japan, state that I am authorized to sign on behalf of the assignee of this invention and that the Assignment referred to below has been reviewed and certify that, to the best of my knowledge and belief, the entire right, title and interest in the above-identified application is in the name of Semiconductor Energy Laboratory Co., Ltd. by virtue of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 6166, Frames 0166-0168.

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6,124,155 and 6,797,548 are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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In making the above disclaimer, Semiconductor Energy Laboratory Co., Ltd. does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 to 156 and 173 of U.S. Patent Nos. 6,124,155 and 6,797,548, as presently shortened by any terminal disclaimer, in the event that they later expire for failure to pay a maintenance fee, are held unenforceable, are found invalid by a court of competent jurisdiction, are statutorily disclaimed in whole or terminally disclaimed under 35 CFR 1.321, have all claims cancelled by a reexamination certificate, are reissued, or are in any manner terminated prior to the expiration of their full statutory term as presently shortened by any terminal disclaimer.

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05/18/2010 Date

Name: Shunpei Yahrazaki Title: President Company Name: Semiconductor Energy Laboratory Co., Ltd.

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AMENDMENT

Honorable Commissioner of Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action dated November 6, 2009, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 17 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

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Listing of Claims:

1. (Currently Amended) A method of manufacturing a display device including a thin film transistor, the method comprising the steps of:

forming a gate electrode over a glass substrate;

forming a gate insulating film comprising silicon nitride [[on]] over said gate electrode;

forming a first semiconductor film comprising amorphous silicon over said gate electrode with said gate insulating film interposed therebetween;

forming an N-type semiconductor film on said first semiconductor film;

patterning said first and N-type semiconductor films using a first photomask;

forming a conductive layer on at least the patterned N-type semiconductor film;

etching a portion of said conductive layer to form source and drain electrodes using a resist formed by a second photomask;

etching a portion of the patterned N-type semiconductor film to form source and drain regions by dry etching using said resist wherein a channel forming region is formed in said first semiconductor film between said source and drain regions; and

forming a passivation film over said glass substrate to cover at least said source and drain electrodes, said channel forming region, a part of a surface of said source region not covered by said source electrode and a part of a surface of said drain region not covered by said drain electrode after removing said resist,

wherein each of the source and drain regions has a bottom surface in contact with the first semiconductor film, each of the source and drain electrodes has a bottom surface in contact with corresponding one of the source and drain regions, and a distance between opposed ends of the bottom surfaces of the source and drain

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electrodes is larger than a distance between opposed ends of the bottom surfaces of the source and drain regions.

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2. (Original) The method of manufacturing a display device including a thin film transistor according to claim 1 wherein said N-type semiconductor film contains phosphorous.

3. (Original) The method of manufacturing a display device including a thin film transistor according to claim 1 further comprising a step of overetching said conductive layer using said resist so that a distance between said source and drain regions is shorter than a distance between said source and drain electrodes wherein said overetching of said conductive layer is performed by wet etching.

4. (Original) The method of manufacturing a display device including a thin film transistor according to claim 1 wherein each of said source region and said drain region partly overlaps said gate electrode.

5. (Original) The method of manufacturing a display device including a thin film transistor according to claim 1 further comprising a step of irradiating at least said channel forming region with a laser for crystallization.

6. (Original) The method of manufacturing a display device including a thin film transistor according to claim 1 wherein said passivation film comprises silicon oxide.

7. (Original) The method of manufacturing a display device including a thin film transistor according to claim 1 wherein said channel forming region comprises intrinsic amorphous silicon.

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