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United States Patent [19]

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Kwasnick et al.

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- [54] **THIN FILM TRANSISTOR STRUCTURE WITH IMPROVED SOURCE/DRAIN CONTACTS**
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- [73] Assignee: **General Electric Company**, Schenectady, N.Y.
- [21] Appl. No.: **825,218**
- [22] Filed: **Jan. 24, 1992**

Related U.S. Application Data

- [63] Continuation of Ser. No. 593,419, Oct. 5, 1990, abandoned.
- [51] Int. Cl.⁵ **H01L 27/01; H01L 27/13; H01L 29/78**
- [52] U.S. Cl. **257/766; 257/383; 257/770; 257/57**
- [58] Field of Search **357/4, 23.7, 41, 2**

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[57] ABSTRACT

Minimum line spacing is reduced and line spacing uniformity is increased in thin film transistors by employing source/drain metallization having a first relatively thin layer of a first conductor and a second relatively thick layer of a second conductor. The second conductor is selected to be one which may be preferentially etched in the presence of the first conductor whereby the first conductor acts as an etch stop for the etchant used to pattern the second conductor portion of the source/drain metallization. This etching is preferably done using dry etching. Dry etching typically provides substantially better control of line width than wet etching. The etching of the second conductor can be done with a dry etch process which etches the photoresist at substantially the same rate as the second conductor whereby the second conductor is provided with a side-wall slope of substantially 45° which improves the quality of passivation provided by subsequent deposition of a conformal passivating layer.

8 Claims, 11 Drawing Sheets

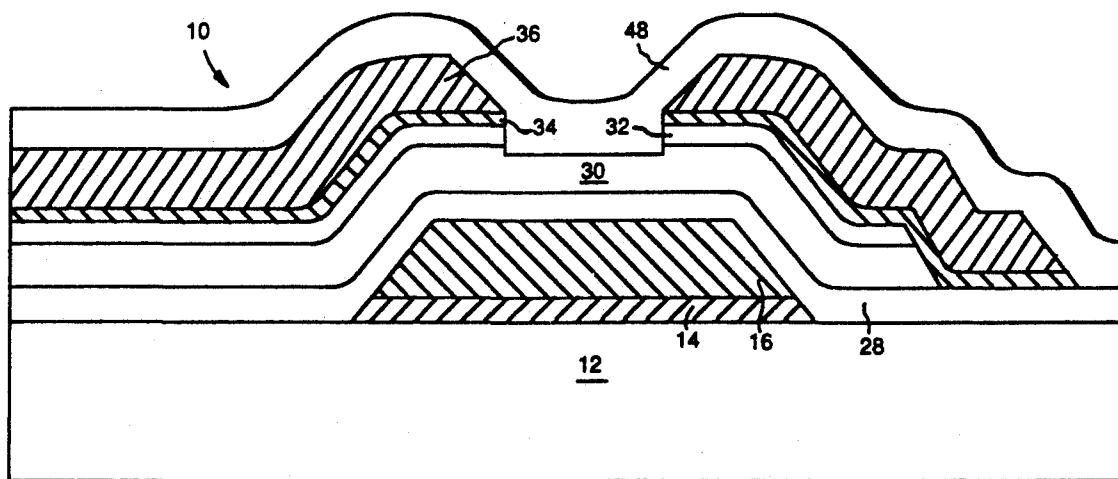


FIG. 1

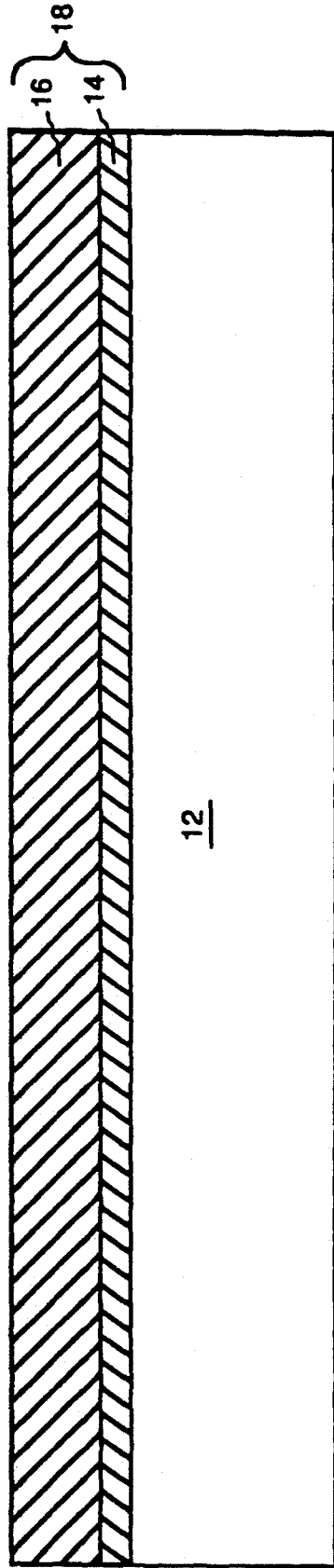


FIG. 2

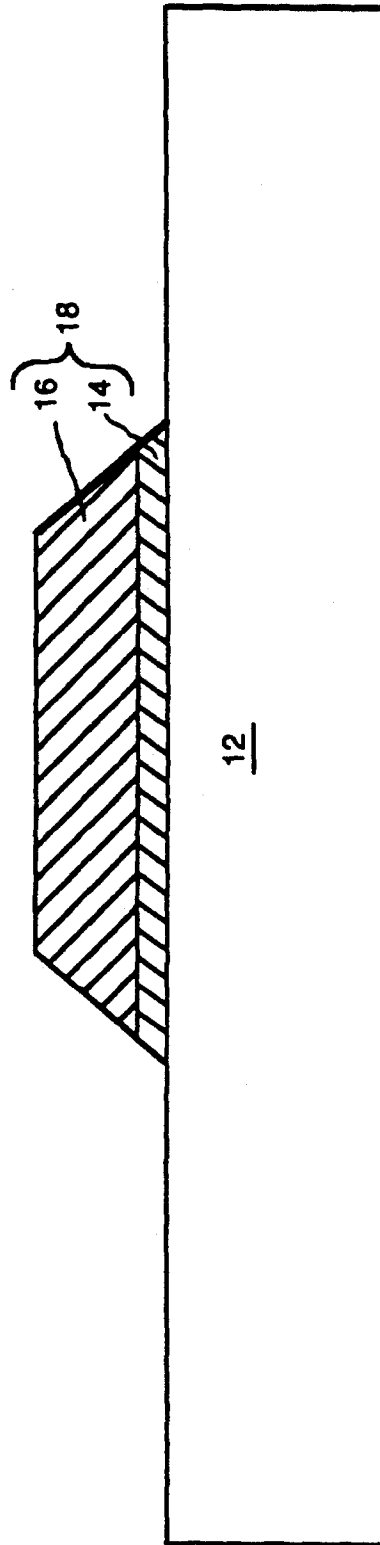


FIG. 3

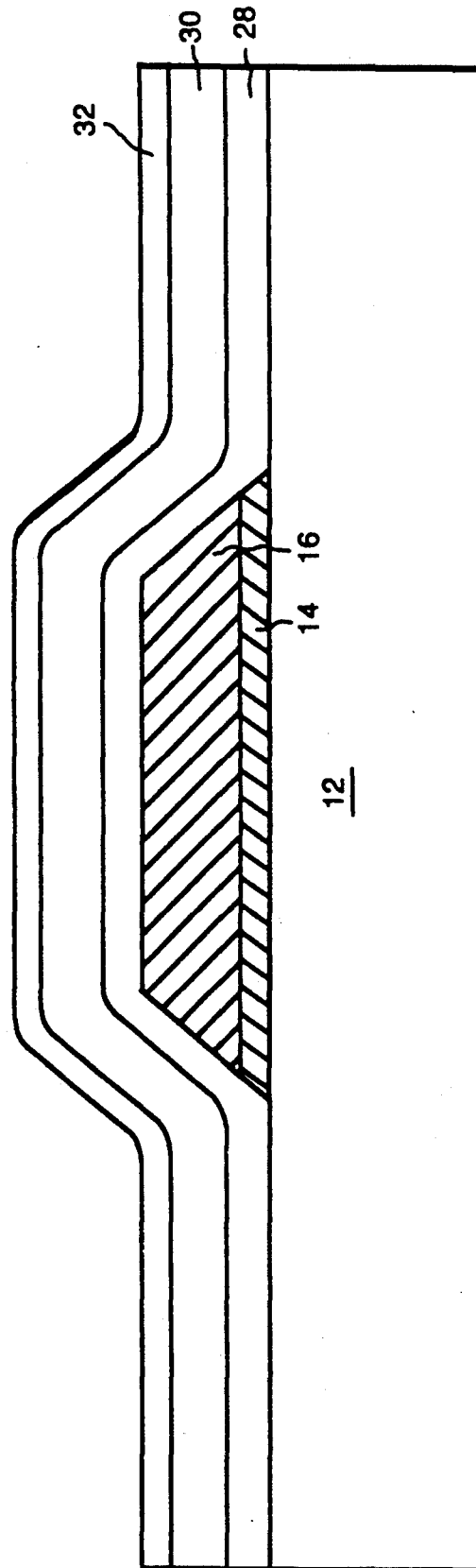


FIG. 4

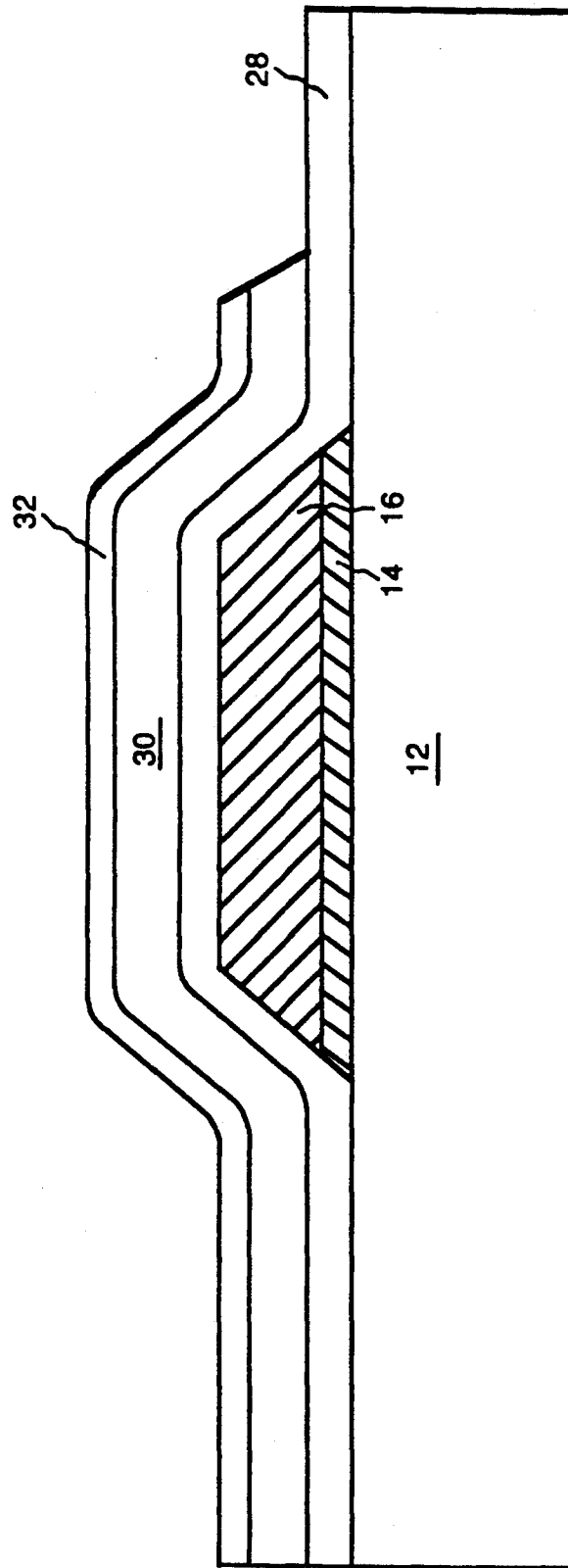
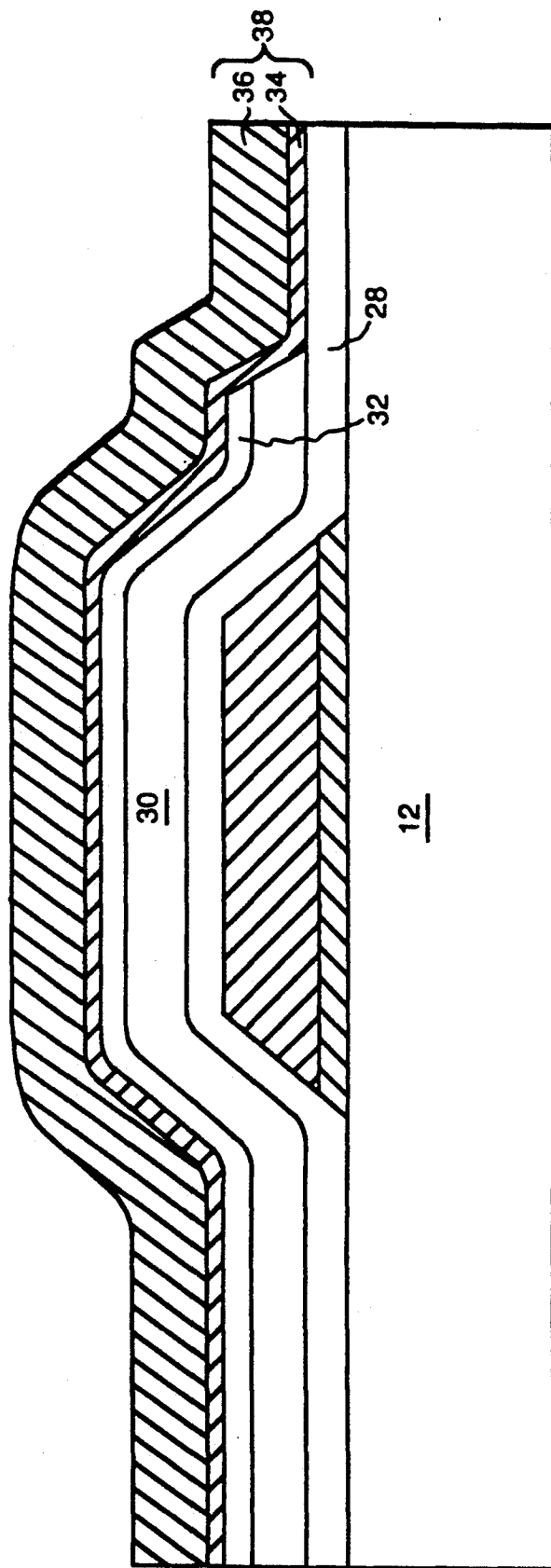


FIG. 5



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