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United States Patent [19]

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Mori et al.

[45] Date of Patent: **Dec. 14, 1993**

[54] **THIN FILM TRANSISTORS WITHOUT CAPACITANCES BETWEEN ELECTRODES THEREOF**

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[75] Inventors: **Hisatoshi Mori, Fussa; Nobuyuki Yamamura, Hanno, both of Japan**

[73] Assignee: **Casio Computer Co., Ltd., Tokyo, Japan**

[21] Appl. No.: **845,771**

[22] Filed: **Mar. 3, 1992**

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Related U.S. Application Data

[63] Continuation of Ser. No. 574,657, Aug. 28, 1990, abandoned.

Foreign Application Priority Data

Sep. 6, 1989 [JP] Japan 1-229227

[51] Int. Cl.⁵ **H01L 49/02**

[52] U.S. Cl. **257/412; 257/66**

[58] Field of Search **357/23.4, 4, 23.7; 257/61, 59, 66, 72, 412**

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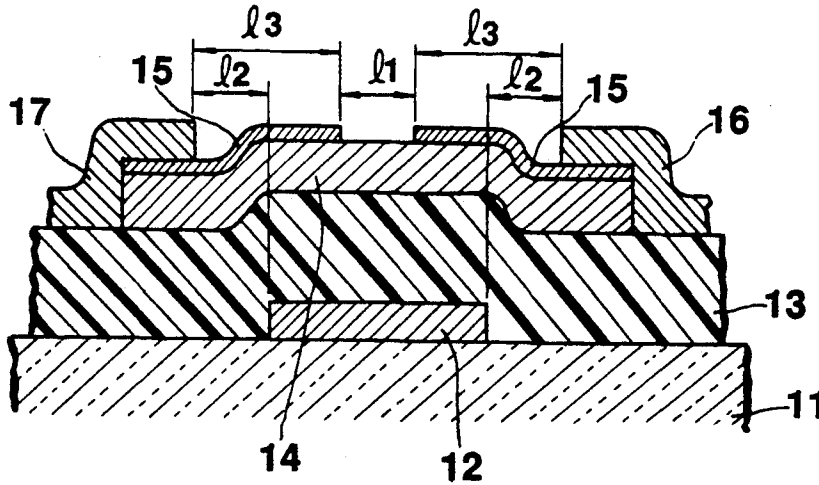
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Primary Examiner—Martin Lerner
Assistant Examiner—Hung Dang
Attorney, Agent, or Firm—Frishauf, Holtz, Goodman & Woodward

[57] ABSTRACT

In this film transistor used for a liquid crystal display element, etc., the source and drain electrodes are formed at positions which do not overlap the gate electrode. Capacitances between the gate and source electrodes and between the gate and drain electrodes can be almost eliminated.

5 Claims, 6 Drawing Sheets



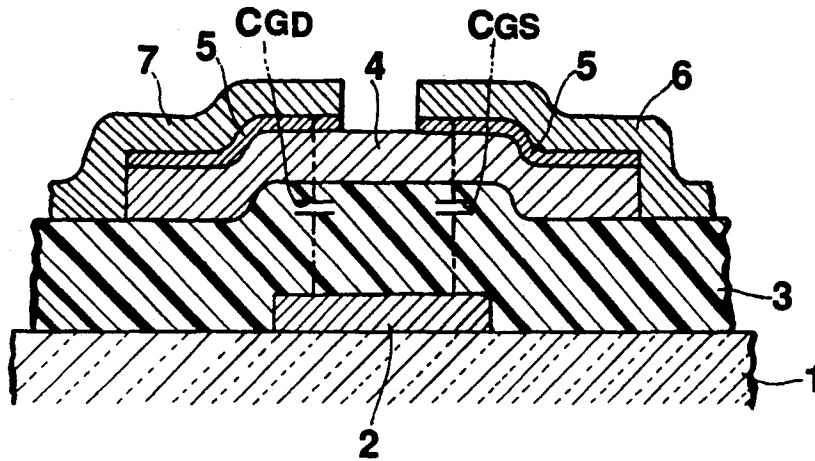


FIG. 1
(PRIOR ART)

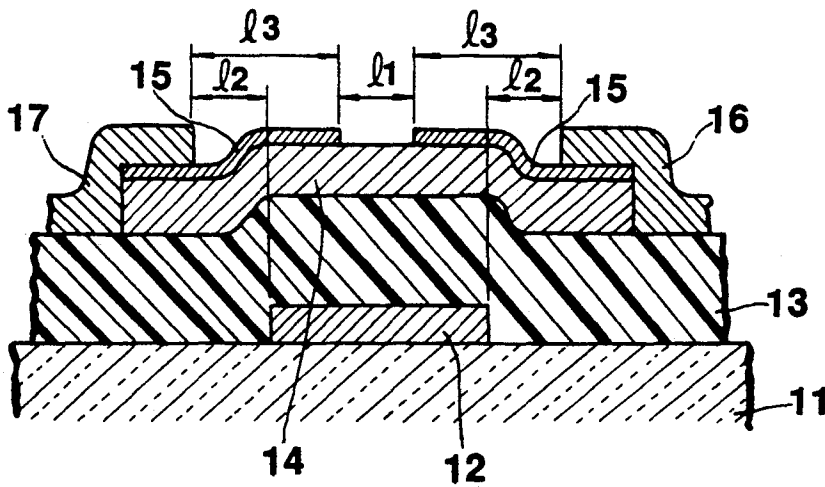


FIG. 2

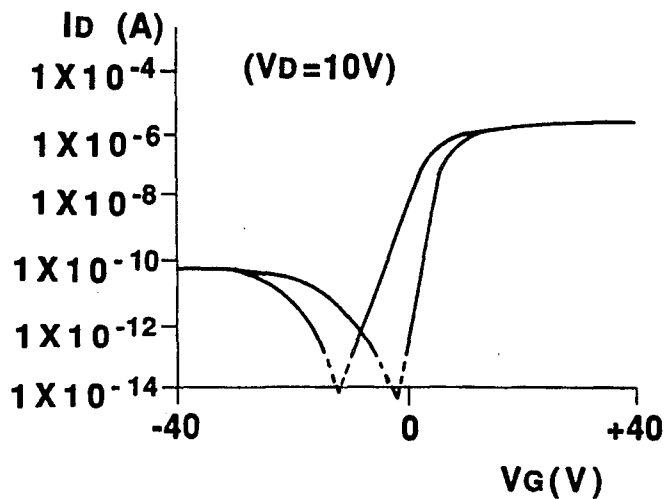


FIG. 3

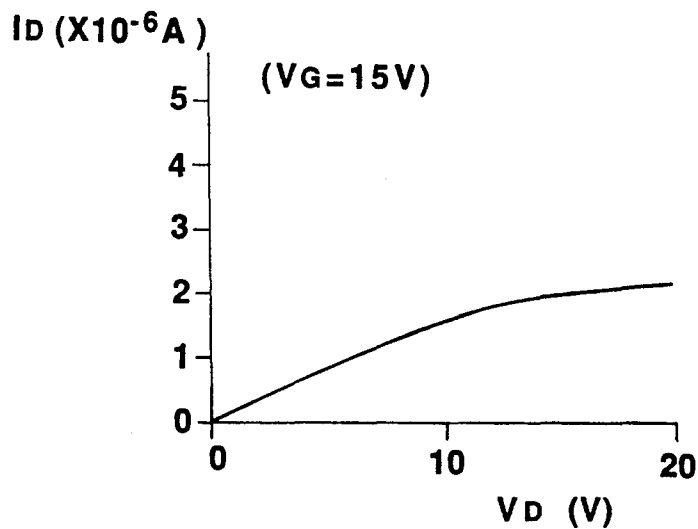


FIG. 4

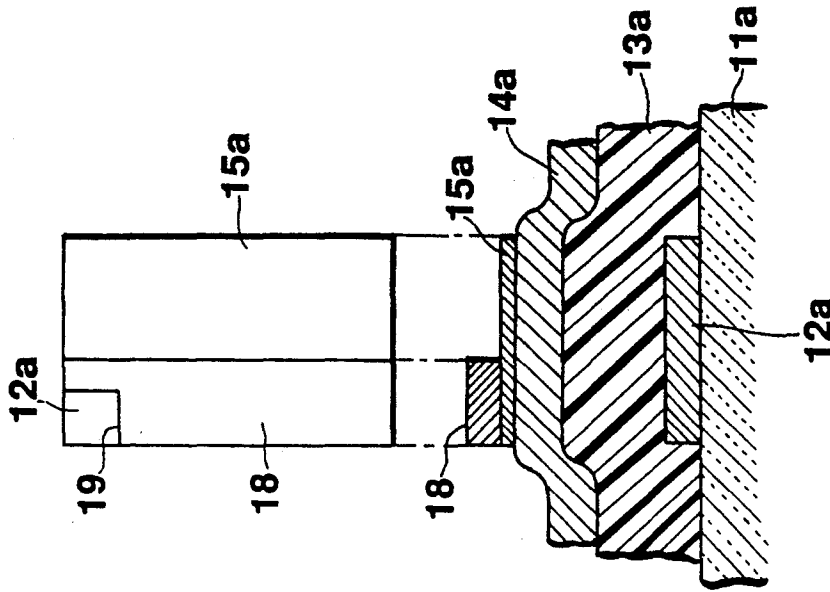


FIG. 5

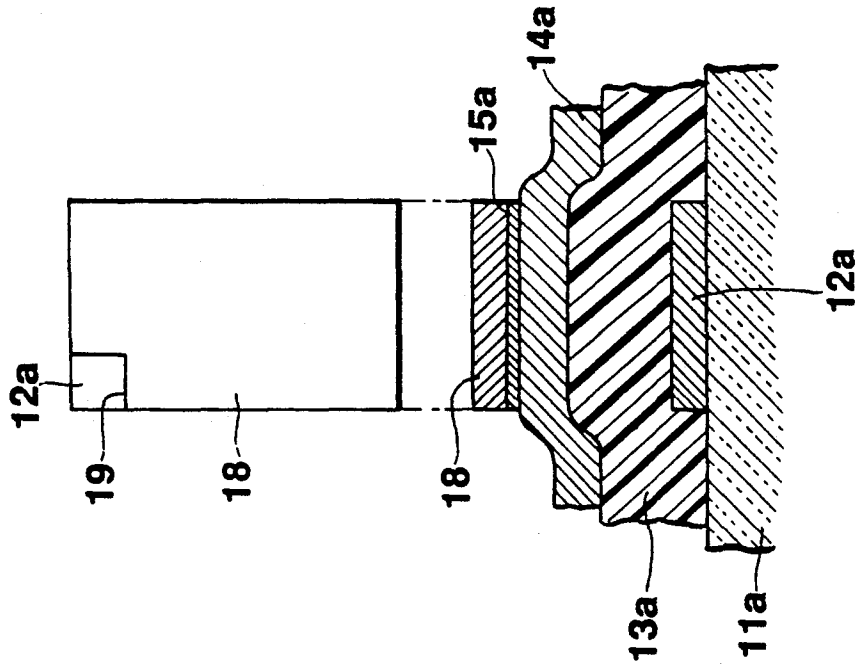


FIG. 6

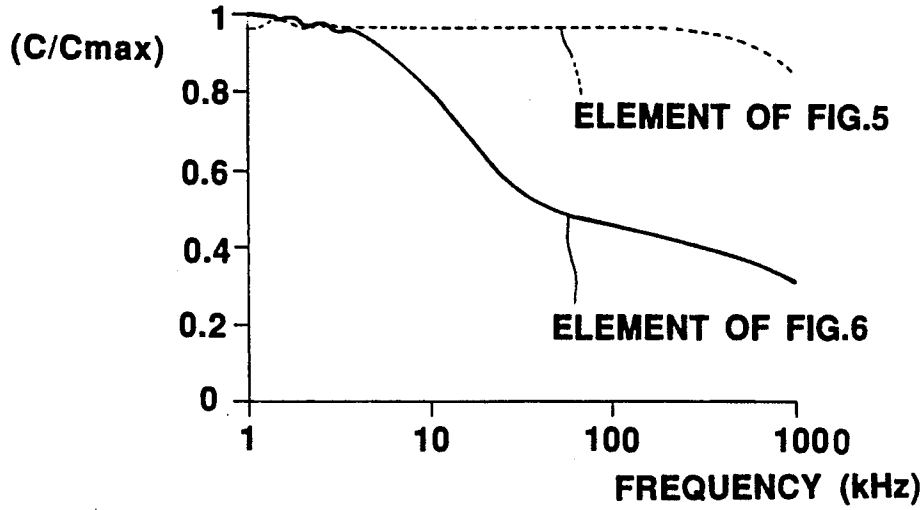


FIG. 7

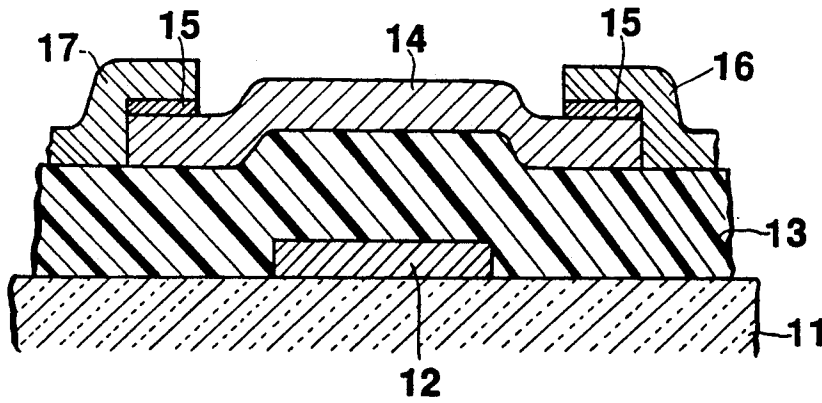


FIG. 8

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