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(54) Title of Invention: Thin-film transistor manufacturing method

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SPECIFICATION

1. Title of Invention

Thin-film transistor manufacturing method

2. Claims

In a manufacturing method for a reverse staggered amorphous silicon thin-film transistor that is formed on an insulating substrate in the sequence of gate electrode, gate insulating film, amorphous silicon film, and source and drain electrodes, a thin-film transistor manufacturing method that is characterized in that it has, after a channel digging-in step which etches a layer, which has a high concentration of impurities, of an amorphous silicon film of a back channel part between a source electrode and a drain electrode, a step in which a modified layer is formed by exposing the i layer surface of the etched amorphous silicon film, by plasma discharge in an atmosphere in which at least one or more species of N, O, C, and B are present.

3. Detailed Description of the Invention

[Industrial field of application]

This invention concerns a manufacturing method for a reverse staggered channel dug-in type thin-film transistor using amorphous silicon; in particular, it concerns a thin-film transistor manufacturing method that includes a back channel processing method that has good stability and yields high reliability.

[Prior art]

From such factors as the fact that a thin-film transistor (TFT) that makes use of amorphous silicon (a-Si) that has been hydrogenated or otherwise treated can be formed on a large-area substrate at low temperature, practical application is being made, in the form of integrating, on a glass or other low-cost substrate, many switching elements of long-size image sensors or large-area, large-capacity liquid crystal display elements.

In an a-Si TFT, from differences in the sequence in which the thin films are laid down onto the substrate, typical forward staggered and reverse staggered structures are known. Of these, from the advantages in structure and the stability of the properties of the TFT, the reverse staggered structure is adopted relatively often, and the channel dug-in type is adopted relatively often because of the terminal dug-in shape, in which there are differences in the ohmic contact formation method.

FIG. 5 (I) to (III) shows an outline of the manufacturing steps for a channel dug-in reverse

staggered a-Si TFT. FIG. 5 (I) shows what results when going through a step in which a $C_?$ [subscripts are illegible] gate electrode 20 is patterned on a glass substrate 10; a step in which onto this are laminated, by breaking down SiH_4 or the like by plasma CVD [chemical vapor deposition], a gate insulating film 30 of $SiO_?$ or $SiN_?$ and an a-Si film i layer 40 and n^+ layer 50; a step in which onto this is formed a source and drain electrode material 670 of ITO [indium tin oxide] or $C_?$ or the like; and a step in which a resist 500 is coated on for patterning in providing source and drain electrodes.

Thereafter, as shown in (II), upon going through a step in which the ITO or $C_?$ is etched and the source and drain electrode material 670 of the back channel part 90 is removed, an a-Si film n^+ layer 50 is exposed on the surface.

In the case of a TFT of channel dug-in type, as in (II), a step is gone through in which, besides the breakdown of the source and drain electrodes 670, the n^+ layer 50 of the a-Si film that is exposed on the back channel part 90 is dug in by etching, and is removed, as shown in FIG. 5 (III). In etching the n^+ layer 50, dry etching is often used, and often a step is adopted in which digging-in is done about as far as the i layer 40.

In the conventional TFT manufacturing method, after[?; as?] shown in (III), if the resist 600 is removed, the step ends, and a structure as shown in FIG. 6 was obtained.

[Problems that the invention is to solve]

As shown in FIG. 6, the above-described channel dug-in reverse staggered a-Si TFT manufacturing method is a manufacturing method in which a back channel part 90 between the source electrode 60 and the drain electrode 70 becomes the topmost surface.

As a result of this, the back channel part 90 becomes a structure in which the i layer a-Si surface 803 is exposed. Thus, surface contamination becomes a cause of contamination of the i layer a-Si surface 803 directly, and becomes a factor leading to a potential change in the back channel 90. Therefore with the conventional manufacturing method for a channel dug-in reverse staggered a-Si TFT, it has been difficult to make an element having the reliability of stable TFT properties.

Also, as an example of this solution measure, one can consider preventing contamination and achieving stability by forming a $SiO_?$ or $SiN_?$ film on the back channel part as a passivation film. But in a general manufacturing step, the step in which the source electrode and drain electrode are formed, the step in which the channel part is formed by etching an a-Si film n^+ layer, and the step in which the above passivation film is formed are all separate steps which must be carried out using completely different manufacturing equipment.

Thus the result is that before the passivation film is formed, the a-Si film i layer is exposed to the outside[?; illegible] and under the working environment, creating a type in which these effects are taken into the interface of the i layer and the passivation film, and there has been the problem that it is difficult to obtain a complete passivation effect.

For example, a conventional product has had the drawback that as shown in FIG. 7 (b), compared with the initial TFT property 42, the TFT property breaks down after formation of the passivation film following back channel formation, or for example after the assembly of liquid crystal display elements, and in the TFT property 44 when inspected, the electric current value in the OFF region increases significantly, resulting in insufficiency as the so-called switching property of a display element.

So the purpose of this invention is to provide a TFT manufacturing method that has high reliability with good stability and reproducibility, etc. of the properties.

[Means for solving the problems]

The thin-film transistor manufacturing method of this invention has -- in the steps for manufacturing a reverse staggered amorphous silicon thin-film transistor in which there are formed on an insulating substrate, in order, a gate electrode, gate insulating film, amorphous silicon film, and source and drain electrodes -- a channel digging-in step which etches an n^+ layer of an amorphous silicon film of a back channel part between the source electrode and the drain electrode, then a step in which a modified layer is formed by exposing the i layer surface of the etched amorphous silicon film, by plasma discharge in an atmosphere in which at least one or more species of N, O, C, and B are present.

In contrast with the above-described conventional thin-film transistor manufacturing method, this invention has a step in which the amorphous silicon film i layer surface of the back channel part is exposed in a plasma discharge, and modification is actively induced so that at least one component of N, O, C, and B

is present. Thus, unlike the laminating in a subsequent step as in a conventional passivation film, because it has a step in which the i layer itself of the TFT channel active layer serves as the modified layer, it is a step in which the interface does not get contaminated, and the interface is made within the i layer. Also, it is easier than a step in which the n^+ layer also is made into an oxide layer as a treatment of the back channel part, and in addition it is simpler than a step in which doping is done by ion implantation, with less damage, no degradation of properties, and the potential for an improved effect.

[Working examples]

In the following we describe this invention, making reference to the drawings.

FIG. 1 is a typical view showing the sequence of steps for describing the manufacturing method of a working example of the invention of this application.

In FIG. 1 (I), a gate electrode 20 of $NiC_?$ is patterned and provided, with a thickness of 1,500 Å, on a borosilicate glass substrate 10. On top of this is formed, by plasma CVD, a silicon nitride ($SiN_?$) film with a thickness of 3,000 Å, and a gate insulating film 30 is provided. At the same time, there are formed by plasma CVD, in order, a hydrogenated a-Si film i layer 40 at 2,000 Å and an n^+ layer 50 at 100 Å, and on top of this are formed, as the source and drain electrode material 670, ITO at 1,000 Å, and $C_?$ at 2,000 Å. Provided on top of this is a resist 500 for performing patterning of the source and drain electrodes.

As the next step, as shown in FIG. 1 (II), using the resist 500 as a mask, the $C_?$ and ITO are wet-etched, and a source electrode 60 [and] drain electrode 70 are formed.

As the following step, as shown in FIG. 1 (III), using the same resist 500 as is, dry etching is done on the a-Si n^+ layer 50 that is present on the back channel part 90. Used for this dry etching is a Cl gas such as, for example, a gas in which O_2 is added to $CCl_?$ gas. Also, this is done including a margin, until the a-Si i layer 40 is etched slightly. Therefore in the back channel part 90, the a-Si surface 803 of the i layer is exposed.

In this invention, further, as the next step, the following plasma treatment step is added, as shown in FIG. 1 (IV).

After completely discharging the etching gas that is used for the dry etching, a plasma discharge is set up using O_2 gas, and the i layer a-Si surface 803 of the back channel part 90 immediately after this etching is done is exposed for about 10 minutes to 15 minutes. This plasma treatment results in a surface modified layer 80 in which the a-Si surface is oxidized on the back channel part 90.

Going through the above steps, the resist 500 is half[?; illegible] separated, and ultimately a TFT is finished that has a cross-sectional shape as shown in FIG. 3.

As stated above, following the dry etching the gas is replaced without taking it out into the atmosphere, plasma processing can be done, and the a-Si surface is not contaminated. Even if the etching and plasma treatment are done using separate manufacturing equipment, after the plasma treatment, the interface between the a-Si i layer and the surface modified layer can be provided on the inner side from the etching surface in the depth direction, and thus its effect can be greatly reduced.

Also, as gas to be used for this plasma treatment, one can use nitrogen, oxygen, $N_?O$, ammonia, methane, ethane, propane, diborane gas, etc. singly, or a mixed gas using nitrogen or oxygen gas as the carrier gas. If these are used, the above sequence of steps is the same, but the resulting surface modified layer 80 is different, and as a result of Auger analysis, N, O, C, and B, etc. were respectively detected.

As shown in FIG. 7 (a), with a TFT having such a surface modified layer 80, the TFT property is almost unchanged between the manufacturing initial period 42 and at 41 when a breakdown inspection was made after assembling it into a liquid crystal display device. Very stable results were obtained. This is due to the fact that in the working examples of this invention, a surface modified layer 80 is formed even if the back channel part 90 is not given a passivation film, so it has characteristics that show no degradation in the following steps or in the step of assembling the display device.

This working example shows another working example of this invention; it is the same as the above working example up to the manufacturing step.

Manufacturing was done by the same method as in the above working example from FIG. 1 (I) to (IV). Thereafter, in this working example the steps in FIG. 2 were added. In FIG. 2 (V), after performing as far as FIG. 1 (IV), the resist 500 was allowed to settle, a film was

formed of SiO_2 or SiN_2 or the like by sputtering or P-CVD, or of polyimide or the like by a coater, and an inter-layer insulating film 100 was formed. After this step, in FIG. 2 (VI), a light-blocking film 110 of C? or Al, etc. is formed at 1,500 Å to 2,000 Å, and the desired pattern is formed via the resist 500.

As stated above, in this working example, after the surface modified layer 80 is formed (the same as in working example 1), a step is added in which an inter-layer insulating film 100 and a light-blocking film 110 are formed. As a result, as the final mode, a TFT can be manufactured that has a structure such as that shown in FIG. 4.

If as heretofore the inter-layer insulating film or light-blocking film is provided on the i layer a-Si surface (803 in FIG. 5 (III)), it was a manufacturing method in which fluctuations in the TFT property occur and reproducibility is lacking, but with a manufacturing method as in the working example of this invention in which a step is interposed in which a surface modified layer 80 is formed, it had characteristics in which the stability of the TFT property is maintained, as shown in FIG. 7 (a), the same as in the working examples.

This is thought to be an effect of the fact that before the step in which the inter-layer insulating film is formed, the back channel part is protected by the surface modified layer. In the case of just an inter-layer insulating film, without providing any light-blocking film, this inter-layer insulating film is equivalent to what is generally called a passivation film, and in this case too, the same effect is obtained.

[Effects of the invention]

As explained above, this invention, by adding a step in which a surface modified layer is formed on the back channel part of the TFT, has made it possible to have a manufacturing method of stable TFT property and high reliability, without any contamination or degradation of the i layer surface, which is the active layer of the a-Si. And the same effect is also obtained in a TFT manufacturing method that provides a passivation film or light-blocking film.

4. Brief Explanation of the Drawings

FIG. 1 (I) to (IV) is a cross-sectional view showing the sequence of steps for explaining the manufacturing method according to one working example of this invention; FIG. 2 (I) and (II) is a cross-sectional view showing the sequence of steps for explaining another working example of the manufacturing method of this invention; FIG. 3 is a cross-sectional view showing the final structure that has gone through the steps of FIG. 1; FIG. 4 is a cross-sectional view showing the final structure that has gone through the steps of FIG. 1 and FIG. 2; FIG. 5 (I) to (III) is a cross-sectional view showing the sequence of steps for explaining a conventional manufacturing method; FIG. 6 is a cross-sectional view showing the final structure according to a conventional manufacturing method; and FIG. 7 (a) and (b) are property diagrams for explaining the changes in the TFT property conventionally and in this invention.

50 … n^+ a-Si film, 803 … i, a-Si surface, 90 … back channel part, 80 … surface modified layer, 100 … inter-layer insulating film, 110 … light-blocking film.

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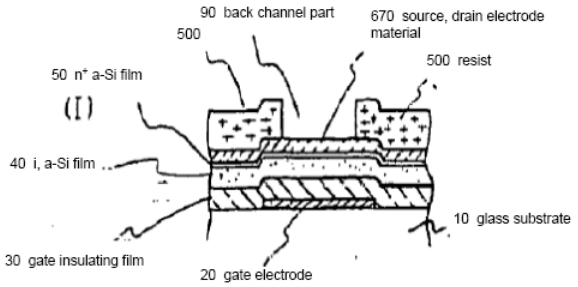
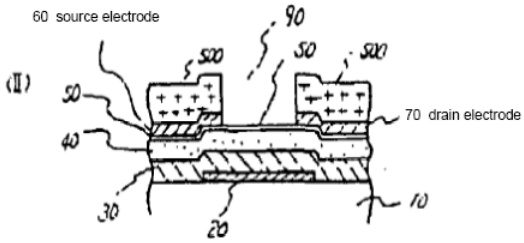
FIG. 1





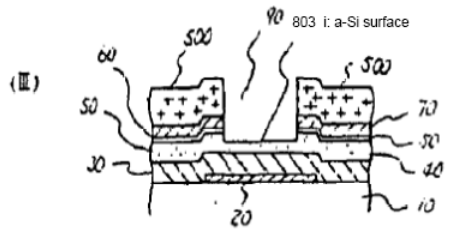


FIG. 1

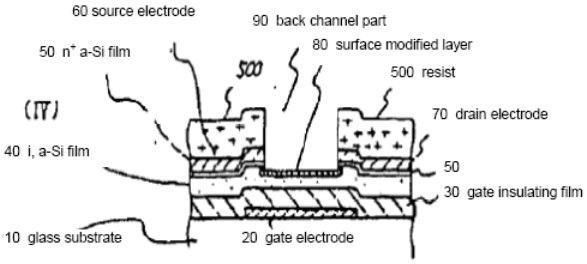
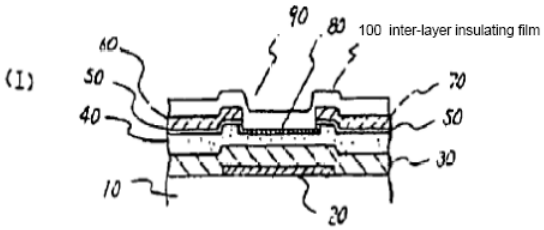
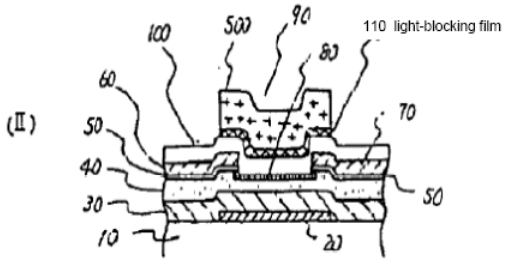


FIG. 2





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