SEL EXHIBIT NO. 2021

INNOLUX CORP. v. PATENT OF SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

IPR2013-00064





Patent Number:

US006104042A

United States Patent [19]

Date of Patent: Aug. 15, 2000 [45]

[11]

[54]	THIN FILM TRANSISTOR WITH A MULTI-
	METAL STRUCTURE A METHOD OF
	MANUFACTURING THE SAME

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[73] Assignee: Chi Mei Optoelectronics Corp.,

Hsinchu, Taiwan

[21] Appl. No.: 0	9/328,580
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Sah

[22]	Filed:	Iun.	10.	1999

[51]	Int. Cl. ⁷		H01L 29/04;	H01L	31/036
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[52]	U.S. Cl.		257/59;	257/66;	257/72
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257/61, 57, 58, 60, 462, 459

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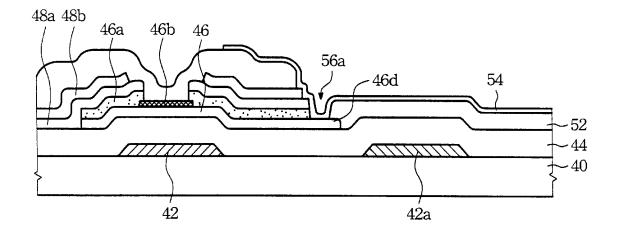
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6-85255	3/1994	Japan	257/72

Primary Examiner—Donald L. Monin, Jr.

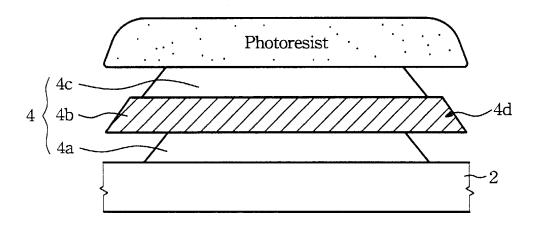
[57] **ABSTRACT**

The present invention includes forming a gate on a transparent substrate. A gate isolation layer is then formed on the gate. An amorphous silicon (a-Si) layer and n+ doped silicon layer are successively formed on the gate isolation layer. Then, the a-Si layer and the n+ doped silicon layer are patterned. A first, a second and a third metal layers are successively formed on the n+ doped silicon layer, thereby forming a multi-metal layer structure. Subsequently, a wet and a dry etching is utilized to etch the multi-metal layer, thereby defining the S/D electrodes. A passivation layer is deposited on the S/D structure.

26 Claims, 9 Drawing Sheets







Aug. 15, 2000

FIG.1 (Prior Art)

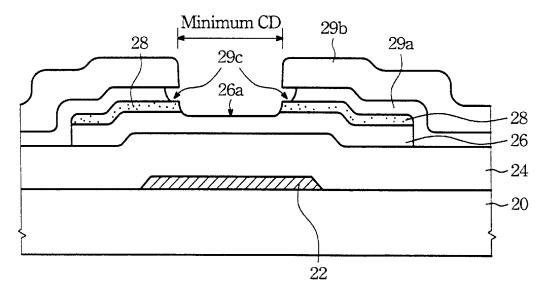


FIG.2 (Prior Art)

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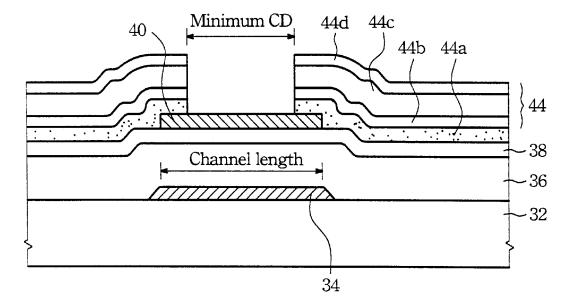


FIG.3 (Prior Art)

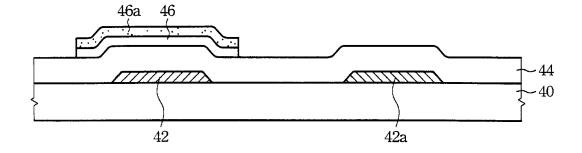


FIG.4

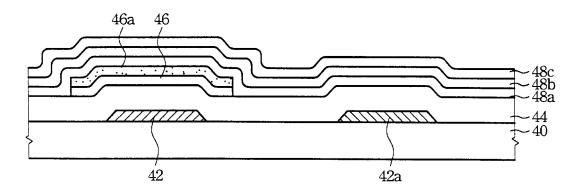


FIG.5

DOCKET

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