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Electrical Instability of Hydrogenated Amorphous Silicon Thin-Film Transistors for Active-Matrix Liquid-Crystal Displays

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We investigated the threshold voltage shifts (ΔV_T) of inverted-staggered hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) induced by steady-state (dc) and pulsed (ac) gate bias-temperature-stress (BTS) conditions. Our study showed that, for an equivalent effective-stress-time, ΔV_T has an apparent pulse-width dependence under negative BTS conditions—the narrower the pulse width, the smaller the ΔV_T. This gate-bias pulse-width dependence is explained by an effective-carrier-concentration model, which relates ΔV_T for negative pulsed gate-bias stress to the concentration of mobile carriers accumulated in the conduction channel along the a-Si:H/gate insulator interface. In addition, our investigation of the methodology of a-Si:H TFT electrical reliability evaluation indicates that, instead of steady-state BTS, pulsed BTS should be used to build the database needed to extrapolate ΔV_T induced by a long-term display operation. Using these experimental results, we have shown that a-Si:H TFTs have a satisfactory electrical reliability for a long-term active-matrix liquid-crystal display (AMLCD) operation.

KEYWORDS: amorphous silicon thin film transistor, threshold voltage, electrical instability, active-matrix liquid-crystal display

1. Introduction

There have been many studies of hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) that concluded that two main mechanisms can explain the electrical instabilities.[1–8] One is the carrier trapping in the gate insulator. In most cases, the gate insulator of a-Si:H TFTs is made of amorphous silicon nitride (a-SiN_x:H) deposited by plasma-enhanced chemical-vapor-deposition (PECVD) technique. It is known that this type of a-SiN_x:H can have a high density of defects,[1,2] which could trap charges during a gate bias-stress of a-Si:H TFTs. This trapping will induce a threshold voltage (V_T) shift. The other mechanism is point defect creation at or near the a-Si:H/a-SiN_x:H interface that will increase the density of deep-gap states, causing the electron threshold voltage to shift in a more positive direction.[4,5,8] A decrease in defect density has the opposite effect on V_T.

Until recently, most studies of a-Si:H TFT electrical instability have employed a steady-state (dc) bias-temperature-stress (BTS) conditions in which a constant gate bias is applied to the gate electrode and a-Si:H TFT characteristics are measured during and/or after a certain bias-stress period. A satisfactory description of the stress-voltage, stress-temperature, and stress-time dependence of the threshold voltage shift (ΔV_T) has been reported for such experiments.[1] However, in active-matrix liquid-crystal displays (AMLCDs), a-Si:H TFTs are bias-stressed under a pulsed (ac) gate-bias addressing (line-at-a-time) with a typical addressing frequency of 60 Hz.[9] It has been pointed out that certain differences exist in ΔV_T between the steady-state and pulsed-bias stresses.[10,11] Therefore, from a practical point of view, to obtain a good estimation of the long-term reliability of a-Si:H TFTs in AMLCDs, it is necessary to understand the details of the electrical instability of a-Si:H TFTs under pulsed gate-bias stress conditions that are similar to a typical AMLCD addressing conditions.

In this paper, we investigate the ΔV_T of bottom-gate back-channel-etched a-Si:H TFTs induced by pulsed BTS. First, we examine the mechanism responsible for ΔV_T in our a-Si:H TFTs. Then, we propose a model to explain the observed difference between steady-state and pulsed BTS induced ΔV_T, especially in the case of the negative gate-bias stress. We also examine methods of estimating ΔV_T of a-Si:H TFTs under pulsed bias-stress having both positive and negative gate-voltage cycles. Using the proposed pulsed gate-bias instability model, an example of the reliability estimation of AMLCDs is given at the end of this paper.

2. Experiment

Figure 1(a) shows the cross-section of the inverted-staggered bottom-gate a-Si:H TFT used in this study. Both a-Si:H and a-SiN_x:H layers are about 3000 Å thick. This TFT is a back-channel-etched type with a phosphorus (P) doped (n^+) a-Si:H layer 500 Å thick that is used to form an ohmic contact to chromium source/drain electrodes. An over-etch process was used to assure complete removal of the n^+ a-Si:H in the back-channel region. At room temperature (~25°C), the regular a-Si:H TFT with channel width(W)/length(L) of 80 μm/12 μm has a field-effect mobility (μ_{FE}) of about 0.9 $cm^2/V{\cdot}s$ and a threshold voltage (V_T) of 1 V. These values indicate a good electrical performance of a-Si:H TFTs used in this study. Together with the regular TFTs, ambipolar a-Si:H TFTs were also fabricated for studying the electrical instability mechanism as shown in Fig. 1(b). The fabrication process for the ambipolar TFT is the same as for the regular TFT except that the n^+ a-Si:H layer was omitted and aluminum was used as the source/drain contact metal. To have a similar process sequence for both types of a-Si:H TFTs, an etching process of the back-channel was used for the ambipolar a-Si:H TFTs with an etching time approximately equal to the over-etching time used for the regular TFT. In addition, the ambipolar a-Si:H TFT has a channel length of 480 μm; a long channel length is selected in this case to reduce the effect of series resistance of the source/drain contacts.

A series of bias-temperature-stress experiments were con-

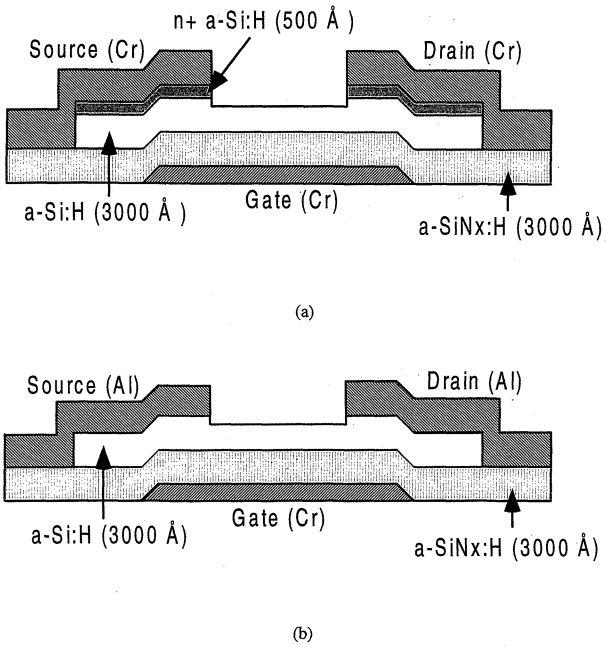


Fig. 1. Cross-sections of (a) regular and (b) ambipolar back-channel-etch a-Si:H TFTs used in this study.

using an HP4156A semiconductor parameter analyzer and a pulse generator (Fig. 2). Pulses with different waveforms were applied to the gate electrode. To assure a uniform electrical field distribution along the a-Si:H/a-SiN_x:H interface, the drain-to-source voltage (V_D) of the TFT was set to 0 V during the BTS. At the preselected stress time, the bias-stress was interrupted and the current–voltage (I_D–V_G) characteristics were immediately measured in the saturation region ($V_D > V_G - V_T$) at the temperature used for BTS. For the ambipolar a-Si:H TFTs, a drain voltage of 15 V and a larger gate voltage (sweeping from −30 V to +30 V) were used to obtain both electron and hole conduction characteristics. A delay time of 2 s was used for each measurement point to reduce the transient effect. This delay time was a trade-off between getting a significant hole current and reducing the measurement voltage stress effect. Because of the longer measurement time needed for the ambipolar TFTs, a lower stress temperature (40°C) was used to reduce the stress effect during the I_D–V_G sweeping. On the other hand, a higher stress temperature (T_{ST} = 70°C) was chosen for the regular a-Si:H TFTs during the steady-state and pulsed BTS to accelerate the electrical instability that can be produced within a reasonable experimental period. The threshold voltage (V_T) at stress time (t_{ST}) during the stress of a-Si:H TFT was extracted from the I_D–V_G characteristics by using the conventional current-voltage equations derived from the gradual channel approximation (GCA) theory,

$$I_D(t_{ST}) = \frac{1}{2}\mu_{FE}C_i\frac{W}{L}[V_G - V_T(t_{ST})]^2 \quad \text{with} \quad V_D > (V_G - V_T) \tag{1}$$

where I_D (t_{ST}) is the measured drain current at t_{ST} and C_i is the gate insulator capacitance per unit area. We used regular a-Si:H TFTs with $L = 10\,\mu$m and $W = 60\,\mu$m, that is similar to the TFTs used in AMLCDs. It should be noted that

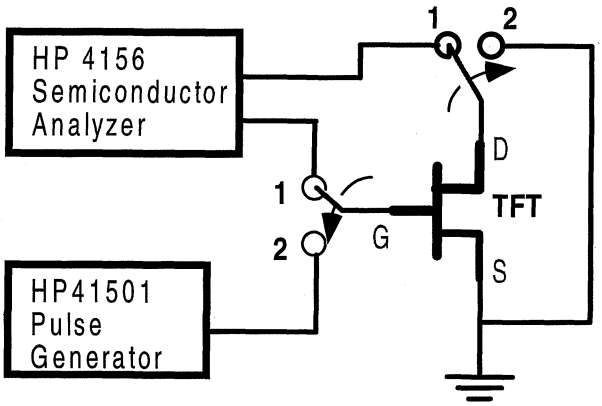


Fig. 2. Schematic of experimental setup used for steady-state and pulsed bate bias-temperature-stress experiments.

dark condition.

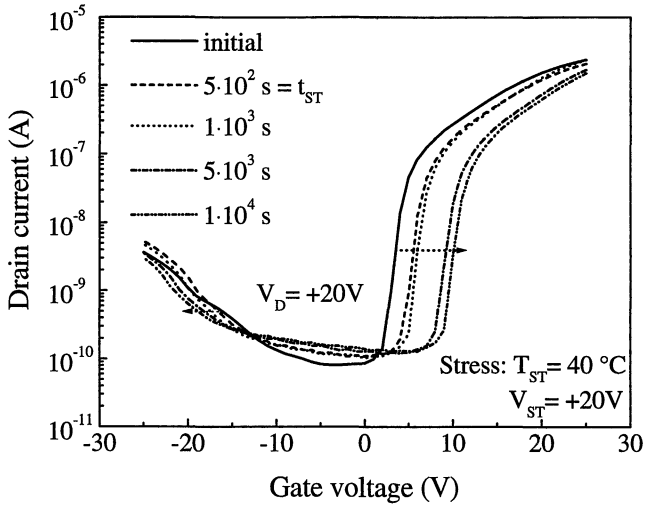
3. Results and Discussion

3.1 Steady-state BTS of a-Si:H TFTs

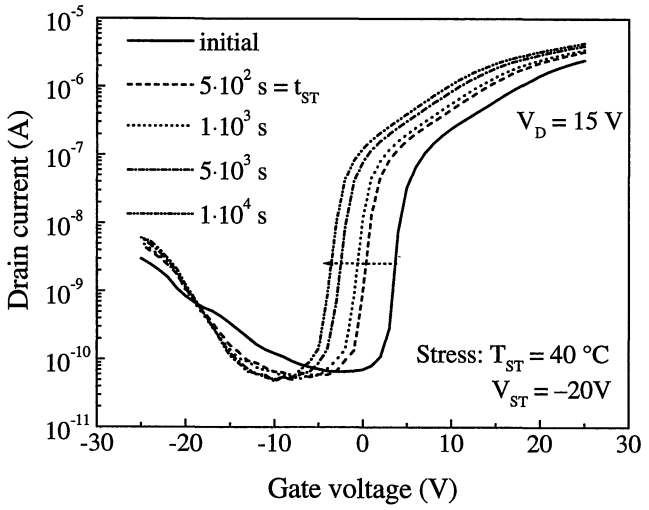
It has been previously indicated that the mechanism responsible for ΔV_T of a-Si:H TFTs can be determined by using ambipolar a-Si:H TFTs.[4] The ambipolar a-Si:H TFTs provide the capability of measuring electron and hole conductions simultaneously because no n^+ a-Si:H layer is used at source/drain contacts to block the hole current. If charges are trapped in a-SiN_x:H during BTS, both electron and hole conduction characteristics will have rigid shift in the same direction. On the other hand, they will shift in the opposite directions if defect density is changed by BTS. Figure 3 shows the evolution of I_D–V_G characteristics for our ambipolar a-Si:H TFTs under +20 V and −20 V steady-state BTS. As can be seen in this figure, the electrons have a higher conduction current than holes, indicating that electrons have a higher mobility in a-Si:H TFTs. For the +20 V BTS condition, an apparent right shift was obtained for electron conduction characteristics. The hole conduction characteristics, on the other hand, shifted slightly to the right at the beginning of the positive gate-bias stress and then started to shift to the left. These results indicate that there is an increase of the density of deep-gap states in a-Si:H near the a-Si:H/a-SiN_x:H interface, which causes the electron and hole conduction characteristics to shift in opposite directions. However, there are also charge trapping which induces the initial right shift of the hole conduction characteristics. The combination of charge trapping and defect creation causes an additive and complimentary effects in the shifts of electron and hole conduction characteristics, respectively. For −20 V BTS, an apparent left shift was obtained for electron conduction characteristics, and a steeper characteristics was obtained for hole conduction. This result corresponds to a decrease of deep-gap states in the band-gap region. Similarly to the positive BTS, charge trapping is also present and the resulting effects is large electron conduction shifts and much smaller hole conduction shift.

It was reported previously that, empirically, a stretched-exponential function can well describe the stress-time and stress-voltage dependence of ΔV_T in a-Si:H TFTs,[1,12]

$$\Delta V_T(t_{ST}) = \Delta V_{To}\left\{1 - \exp\left[-\left(\frac{t_{ST}}{\tau}\right)^{\beta}\right]\right\}, \tag{2}$$

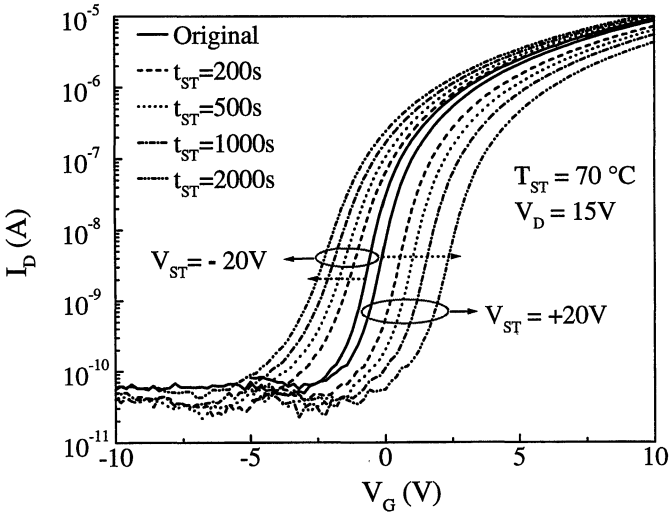


(a)

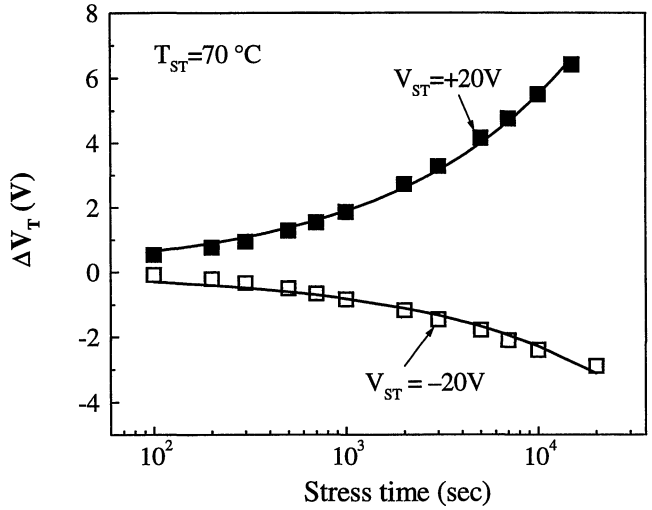


(b)

Fig. 3. Evolution of I_D–V_G characteristics of the ambipolar a-Si:H TFTs induced by (a) positive and (b) negative steady-state gate bias-temperature-stress. The stress and measurement temperatures are 40°C.



(a)



(b)

Fig. 4. (a) Evolution of I_D–V_G characteristics and (b) extracted ΔV_T versus stress time for the regular a-Si:H TFTs induced by steady-state positive and negative gate bias-temperature-stress. The TFT channel width and length are 80 and 12 μm, respectively. The stress and measurement temperatures are 70°C.

with

$$\Delta V_{To} = \Delta V_T(\infty) = V_{ST} - V_T(0), \tag{3}$$

where ΔV_{To} is the shift at infinite time, τ is a characteristics time constant, and β is the stretched-exponential exponent which is temperature-dependent. For a short effective stress time ($t_{ST} \ll \tau$), eq. (2) can be simplified as

$$\Delta V_T(t_{ST}) = \Delta V_{To} \tau^{-\beta} t_{ST}^{\beta}. \tag{4}$$

Figure 4(a) shows the evolution of I_D–V_G characteristics of our ordinary a-Si:H TFTs under +20 V and −20 V steady-state BTS at 70°C. Because of the presence of P-doped a-Si:H layer at the source/drain contacts, only the electron conduction characteristics are observed. The characteristics have right and left shifts under +20 V and −20 V BTS, respectively. The evolution of the threshold voltage shift extracted from the

ting of the experimental data with eq. (4) is also shown; we obtained the stretched-exponential exponents β of 0.50 and 0.32 for positive and negative BTS, respectively; and these β values are similar to those reported previously.[1,3]

Figure 5 shows ΔV_T as the functions of effective gate-bias stress voltages at various stress times. The effective stress voltage is defined as the difference between the applied gate-bias stress voltage (V_{ST}) and the initial threshold voltage (V_{Ti}). It can be seen that there is a power-law dependence between ΔV_T and the effective stress voltage that can be described by,

$$|\Delta V_T| \propto |V_{ST} - V_{Ti}|^{\alpha}. \tag{5}$$

This power law dependence on stress voltage indicates that the characteristics time constant τ in eq. (2) must be stress-voltage dependent. We can further simplify the stretched-

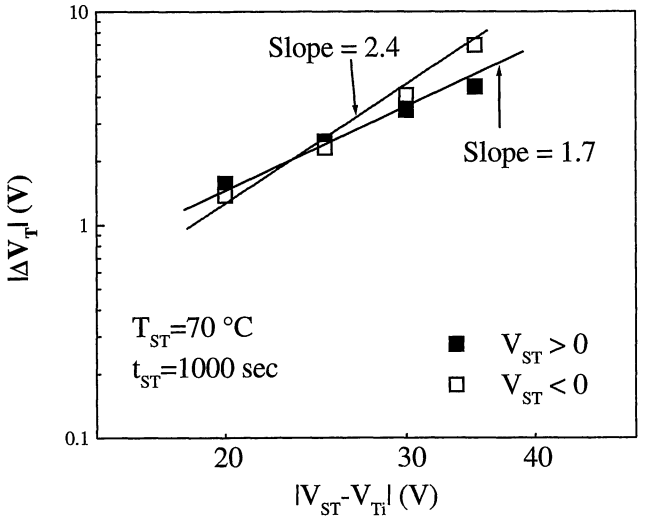


Fig. 5. ΔV_T as a function of effective stress voltage $|V_{ST} - V_{ti}|$ induced by positive and negative BTS.

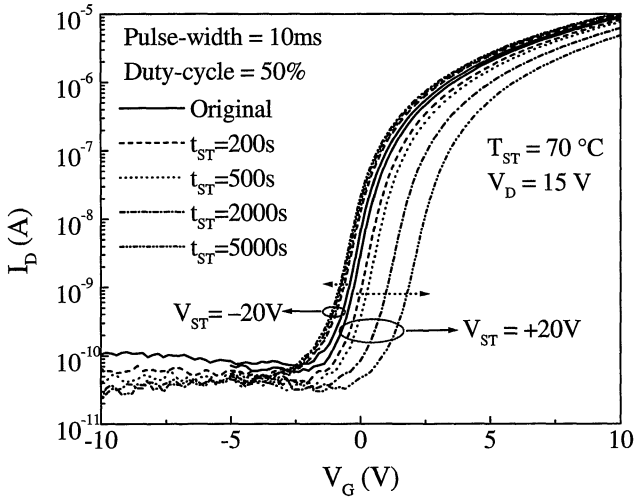


Fig. 6. Evolution of I_D–V_G characteristics of the regular a-Si:H TFTs induced by pulsed positive and negative gate bias-temperature-stress. The TFT channel width and length are 80 and 12 μm, respectively. The stress and measurement temperatures are 70°C.

$$\Delta V_T(t) = A|V_{ST} - V_{Ti}|^{\alpha} t^{\beta} \quad (6)$$

where A is a constant. Equation (6) was often used for the estimation of ΔV_T in AMLCDs,[13] and will be used in this study. Table I lists the parameters extracted from the experimental data obtained for the a-Si:H TFTs under positive and negative steady-state gate-bias stress. This data is consistent with the previously reported results.[13]

3.2 *Pulsed BTS of a-Si:H TFTs*

Figure 6 show the evolution of I_D–V_G characteristics of a-Si:H TFTs during a positive and negative pulsed BTS with a duty-cycle of 50% and gate-bias pulse width of 50 μs at 70°C. A qualitative comparison between Fig. 6 and Fig. 4(a) shows that, under positive BTS, pulsed and steady-state bias-stress induce a similar evolution of I_D–V_G characteristics. However, ΔV_T induced by the negative pulsed gate-bias stress is significantly smaller in comparison with ΔV_T induced by negative steady-state gate-bias stress. Figure 7 shows the threshold voltage shift versus effective stress time under both positive and negative bias-stress for different pulse conditions. The effective stress time is the accumulated time when the gate voltage is high (ON). For positive pulsed gate-bias stress, ΔV_T is slightly smaller than that for steady-state gate-bias stress and does not depend apparently on gate-bias pulse width. For negative pulsed gate-bias stress, ΔV_T has strong pulse-width (PW) dependence—the wider the pulse-width, the greater the magnitude of ΔV_T.

It was reported previously that detrapping during pulsed operation can explain the smaller ΔV_T induced by steady-state BTS.[10] The detrapping mechanism can be applied to a-Si:H TFTs if the electrical instability mechanism is mainly

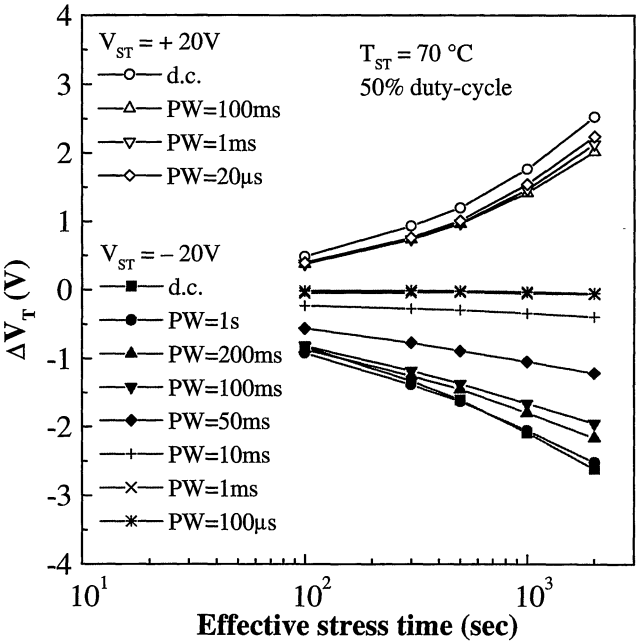


Fig. 7. ΔV_T versus effective stress time induced by positive and negative gate-bias stress with different gate pulse width. The effective stress time is the accumulated time when the gate voltage is high (ON).

Table I. Extracted parameters from ΔV_T induced by positive and negative steady-state bias-stress for inverted-staggered a-Si:H TFTs used in this study.

	A	α	β
Positive(+)BTS	1.5×10^{-4}	1.9	0.5
Negative(–)BTS	1.4×10^{-4}	2.4	0.32

associated with the charge-trapping in the gate insulator. During the OFF-cycle of the pulse bias-stress, some of the trapped charge which is not deeply trapped could be relaxed from the trap centers. However, for our a-Si:H TFTs, defect creation also contributes to the shift of V_T. Therefore, this smaller ΔV_T for positive pulsed BTS can also be partially attributed to relaxation of created deep-gap defects during OFF-periods in the pulsed operation. It should be noted that there is a very small pulse-width dependence observed for positive pulsed BTS. As will be discussed below, this can be explained by the fast channel electron accumulation during positive pulse bias, that is about or less than 1 μs for a 10-μm channel-length

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