SEL EXHIBIT NO. 2016

INNOLUX CORP. v. PATENT OF SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

IPR2013-00064

THE EFFECT OF CONTACT OVERLAP DISTANCE ON a-Si TFT PERFORMANCE

SHUICHI UCHIKOGA, MASAHIKO AKIYAMA, TAKASHI KOIZUMI, MITSUSHI IKEDA AND KOUJI SUZUKI
Research and Development Center, TOSHIBA Corp., 1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 210, Japan

ABSTRACT

The gate/source overlap distance (ΔL_s) is an important factor in fabricating self-aligned TFT with passivating layer. Six types of TFT were fabricated using thin intrinsic a-Si layers such as 20 nm,50 nm and 100 nm and a n+:a-Si or a n+:μc-Si were used as the contact layer. The least required gate/source overlap distance, ΔL_{sc} is the critical overlap where the TFT performance is not limited by the contact. This ΔL_{sc} was determined experimentally. ΔL_{sc} was found to be significantly affected by the intrinsic a-Si layer thickness and the ΔL_{sc} can be small by depositing a thin intrinsic layer. The intrinsic layer thickness dependence of ΔL_{sc} in the linear region can be explained from a existing model. However, the behavior in the saturation region suggests the need of another model, which will be discussed here. The variation of n^+ contact layer shown to have a small effect on ΔL_{sc}. In order to determine appropriate ΔL_s for self-alignment TFT, the magnitude of field effect mobility, threshold voltage and drain current as well as ΔL_{sc} must be considered.

INTRODUCTION

The self-alignment technique is important especially for liquid crystal display (LCD) manufacturing. This is because either in large area LCDs or in high definition LCDs, pattern misalignment fatally degrades picture quality. One of the effective methods to avoid deterioration of picture quality is the self-alignment of passivating SiNx which covers the channel region to the gate electrode. Passivating SiNx can be self-aligned to the gate electrode by exposing photoresist from the back side of the substrate. Channel length can be fabricated uniformly without any mask alignment by using this technique. Hence, gate/source overlap (ΔL_s) is made uniformly over the whole display area. Usually the overlap will be less than one micron. Furthermore, this small gate/source overlap reduces parasitic capacitance. However, small ΔL_s limits TFT performance [1], [2].

In this work, the authors wish to study factors which determine the least required ΔL_s, which will be defined as ΔL_{sc}. The TFT structure used in this work is shown in Fig.1. Two parameters, namely, intrinsic layer thickness and n+ contact layer quality, were varied to investigate the effect of ΔL_{sc} on TFT characteristics.

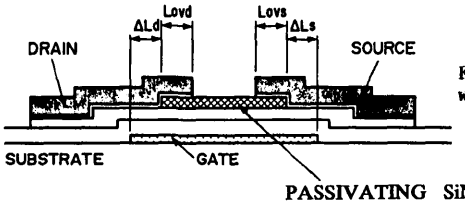


Fig.1; Cross sectional view of TFT with passivating layer.

Mat. Res. Soc. Symp. Proc. Vol. 258. ©1992 Materials Research Society

EXPERIMENTAL

Device fabrication

The Mo-Ta gate electrode was patterned on a glass substrate, and PECVD was utilized to deposit SiOx and SiNx as the gate insulators, a-Si as intrinsic layer, and SiNx as the passivating layer. The photomask was designed to vary ΔL_s from -3 μm to 3 μm and ΔL_d was fixed to 3μm. Here, minus means an offset TFT. Intrinsic a-Si layers were deposited with the thickness of 20 nm, 50 nm and 100 nm. Furthermore, phosphorus doped n+ amorphous silicon (n+:a-Si) or n+ microcrystalline silicon (n+:μc-Si) were deposited as the contact layer. As a result, 6 types of TFT were fabricated. The channel length and width of the TFT were 12 μm and 60 μm, respectively.

In this work, the main concern was focused on the source contact. L_{ov_s} and L_{ov_d} were designed to be constant, since it greatly affects device performance. From the measurement, L_{ov_s} and L_{ov_d} were in a length about 2.5 μm.

Characterization

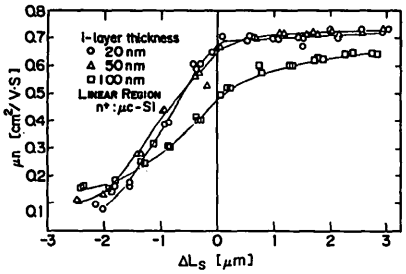
All ΔL_s were measured by using pictures taken from FE-SEM observation. TFT performance was characterized by field effect mobility (μn), threshold voltage (Vth), and drain current (Ids). μn and Vth were obtained for both linear region and saturation region. Drain voltage Vds=0.1[V] was used for the linear region and Vds=15[V] for the saturation region. Gradual channel approximation was adopted to obtain μn and Vth for linear region and saturation region. Ids at Vgs=15[V] was employed as characteristic Ids for both the linear and saturation region.

The n+ contact layers were characterized by measuring its dark conductivities. The conductivities were measured by depositing approximately 1 μm thick phosphorus doped a-Si film. The conductivities were 1.0×10^{-3} $(ohm\cdot cm)^{-1}$ and 8.0×10^{-1} $(ohm\cdot cm)^{-1}$ for a-Si and μc-Si, respectively.

RESULTS

Figures 2, 3 and 4 show the ΔL_s dependence of TFT performance for three different intrinsic layer thickness in terms of μn, Vth and drain current Ids(Vgs=15[V]). These results are obtained by TFTs with n+:μc-Si contact layer. The figures clearly show that μn and Ids decrease as ΔL_s reduces. The figures also show that μn and Ids become independent of ΔL_s in the region $\Delta L_s > 2$ μm.

The μn in $\Delta L_s > 2$ μm greatly depends on the intrinsic layer thickness in the saturation region while the thickness does not affect the μn in the linear region, as it can be seen in Figs.2 and 3. That is, in the saturation region (Fig.3), the average μn at $\Delta L_s > 2$ μm are 0.52 $(cm^2/V\cdot S)$, 0.63 $(cm^2/V\cdot S)$, and 0.78 $(cm^2/V\cdot S)$ for intrinsic layer thickness 20 nm, 50 nm, and 100 nm, respectively. In the linear region, 0.73 $(cm^2/V\cdot S)$, 0.73 $(cm^2/V\cdot S)$, and 0.64 $(cm^2/V\cdot S)$ for thickness 20 nm, 50 nm, and 100 nm, respectively. The drain current in the saturation region is also affected by the film thickness (Fig.4).



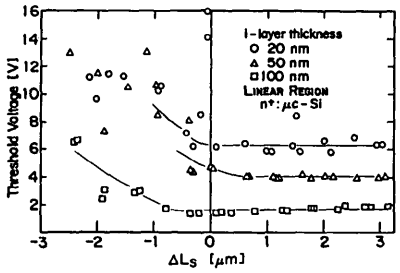
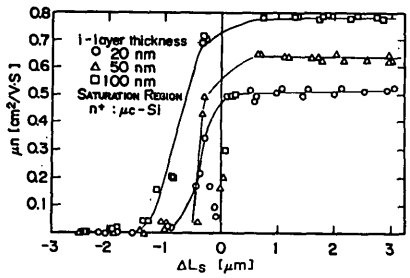


Fig.2; ΔLs dependence of field effective mobility (above) and threshold voltage (below) in the linear region for n+:μc-Si contact layer.



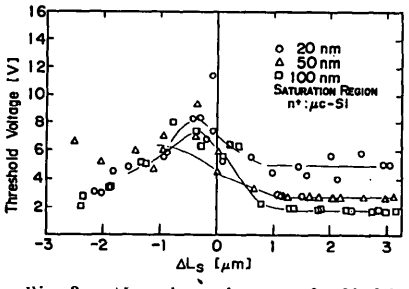


Fig.3; ΔLs dependence of field effective mobility (above) and threshold voltage (below) in the saturation region for n+:μc-Si contact layer.

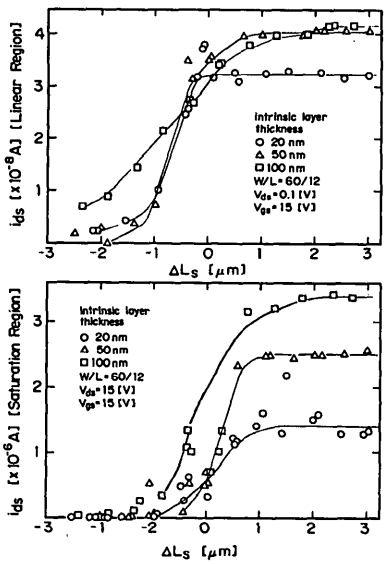


Fig.4; ΔLs dependence of the drain current at Vgs=15[V], Vds=0.1[V] (above) and Vds=15[V] (below) for n+:μc-Si contact layer.

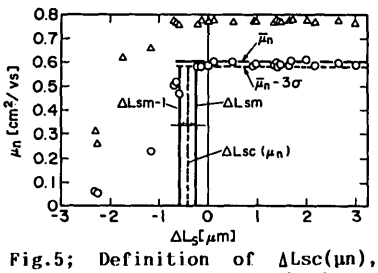


Fig.5; Definition of ΔLsc(μn), which is the least required ΔLs for field effective mobility.

Definition of ΔL_{sc}

In order to evaluate the effect of ΔL_s on the TFT performance, the critical length, ΔL_{sc}, will be introduced. The meaning of ΔL_{sc} is the least required gate/source overlap distance, that does not deteriorate TFT performance.

To show the procedure of obtaining ΔL_{sc}, Fig.5 will be used in the case of μn. The values of μn and Ids at $\Delta L_s > 2$ μm will be used as TFT characteristics which are not deteriorated by the gate/source contact overlap.

The embodiment of obtaining ΔL_{sc} experimentally is as shown below.

1. Calculate the average μn (μn(avg)) and standard deviation(σ).
2. Define the minimum ΔL_s as ΔL_{ss} from the measured data point which satisfies μn(avg)-3σ. Then, define the next smaller data point as ΔL_{ss-1}.
3. Then we define ΔL_{sc} for μn as

$$\Delta L_{sc}(\mu n) = (\Delta L_{ss}(\mu n) - \Delta L_{ss-1}(\mu n))/2.$$

In the same manner, ΔL_{sc} for drain current (ΔL_{sc}(Ids)) is defined as

$$\Delta L_{sc}(Ids) = (\Delta L_{ss}(Ids) - \Delta L_{ss-1}(Ids))/2.$$

ΔLsc dependence of TFT performance

Figures 6 and 7 are obtained by using the above definition for each intrinsic layer thickness and for each contact layer. Fig.6 is the ΔL_{sc} dependence for μn and Fig.7 is for the drain current. It is clear that ΔL_{sc} decreases as intrinsic layer thickness reduces for both μn and Ids. It is shown that intrinsic layer thickness is one of the major factors which determine ΔL_{sc}.

These results from Figs.6 and 7 indicate that ΔL_s can be made smaller for thinner intrinsic layers when self alignment of passivating SiNx by gate pattern is concerned. However, it must

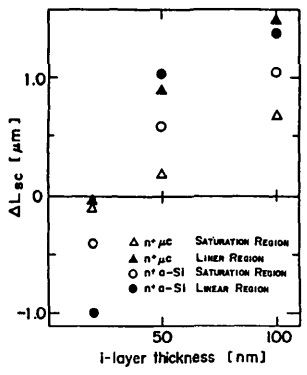


Fig.6; Intrinsic layer thickness dependence of ΔLsc for field effective mobility.

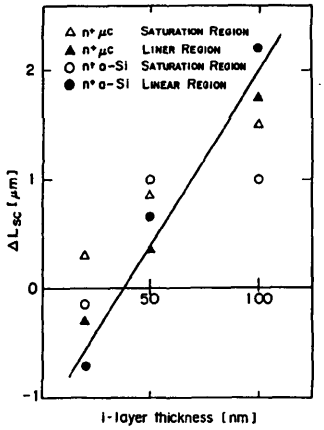


Fig.7; Intrinsic layer thickness dependence of ΔLsc for drain current.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.