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SIMPLE PROCESS FOR MAKING NEW SELF-ALIGNED TFT WITH IMPROVED ON-CURRENT.

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A simple process for making new self-aligned a-Si:H thin film transistor has been proposed in this paper. In order to pattern both etch stopper SiN_x and channel a-Si:H simultaneously, only one photo and one reactive ion etching (RIE) process were used. Second a-Si:H layer was deposited prior to the deposition of n^+ a-Si:H layer. Compared to that of the TFT without second a-Si:H layer, I_{on} of the TFT with second a-Si:H layer increases because of the increase of space charge limited current through the longer overlap length. As a result, the on-current of the new self-aligned TFT is comparable to that of the conventional self-aligned TFT. As the deposition power of second a-Si:H increases, the threshold voltage decreases and the field effect mobility increases. At the high deposition power, the damaged SiH bond, considered as a positive charge-trapping center, at the top of the gate insulator in the overlap region would be etched more effectively by the high energy hydrogen plasma. This decrease of positive charge-trapping center is consistant with the lower threshold voltage.

INTRODUCTION

Since the hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) has been considered as a good driving and switching device for the active matrix liquid crystal display(AMLCD) and other large area electronics[1], the TFT-LCD industry has been grown up to the mass production era. So many researches have been focused not only on the physics but also on the improvement of image quality of the large are AMLCD with low manufacturing cost and high production yield.

Typically, there are two kinds of structure in inverted-staggered TFT, back channel etch (BCE) type and etch stopper (E/S) type. Among the two structures, E/S type TFT is less photo sensitivity due to the thinner a-Si:H layer and less leakage current due to its lower top interfacial density of states than the BCE type TFT.[2] Especially, self-aligned TFT (SA-TFT) is considered as a prominent structure for better image quality because the uniform and small capacitance between gate/drain overlap could be made all over the display area.[3]. But, the process for making SA-TFT is more complicated than that for BCE TFT. Usually, in order to make E/S SiN_x and channel a-Si:H, photolithography and etch steps are used twice. These are wet etch process with buffered hydrofluoric (BHF) acid for E/S SiN_x, and dry etch for channel a-Si:H.

In order to reduce the process steps, Kuo[4] reported a simple process with one photo step and two etch steps to get E/S SiN_x and channel a-Si:H. But the on-current of the TFT prepared by that process is not so high as that of the SA-TFT prepared by conventional method. Besides, the BHF was used to pattern the E/S SiN_x. As the Kato *et al* reported[5], some particles such as $(NH_4)_3AlF_6$ and $(NH_4)_2SiF_6$ would be produced from the interaction between the glass substrate and BHF solution. These particles are hardly removed by conventional cleaning method. If these particles would be attached to the glass substrate, these might cause some defects in TFT array.

In this work, a new SA-TFT with improved on-current has been prepared by simple and clean process. Only one photo and etch step was used for the E/S and channel a-Si:H. In order to increase the on-current of the new SA-TFT, the second intrinsic a-Si:H layer was deposited at different deposition power. The role of the second a-Si:H layer and the effect of the deposition power of it on the TFT characteristics was investigated.

EXPERIMENTAL PROCEDURES

Figure 1 shows the vertical structure of the new SA-TFT with second a-Si:H layer.

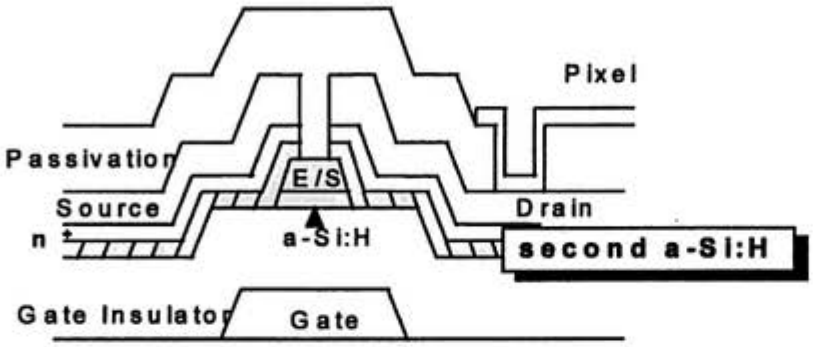

Fig. 1 . The vertical view of new self-aligned TFT.

Al-alloy of 2500 Å was deposited on the glass substrate (Corning 1737) by magnetron sputtering system (Leybold, ZV6000), and patterned as a gate bus line and then anodized. The gate insulator SiN_x (4000 Å), channel a-Si:H (600 Å) and E/S SiN_x (2000 Å) were deposited sequentially by plasma enhanced chemical vapor deposition system (PECVD, Anelva 9106) at 320 ℃, 250 ℃ and 230 ℃, respectively. The back side exposing method was used to form the E/S island photo resist pattern. The initial overlap length after development was 0.5 ㎛. Then reactive ion etching (RIE) process (PSC, DES-325EA) was applied to pattern both E/S SiN_x and channel a-Si:H simultaneously in one vacuum chamber with the feeding gases of $CF_4 + He + O_2$ for SiNx and $CF_4 + Cl_2 + O_2$ for a-Si:H. Because the etch selectivity between thick SiN_x and thin a-Si:H was very low, end point detector (EPD) sensor was used to minimize the damage on the gate insulator for E/S SiN_x. Then n^+ a-Si:H layer of 500 Å and Cr of 1500 Å were deposited. After source/drain electrodes were patterned, n^+ a-Si:H was etched using source/drain pattern as a mask. Then the passivation SiN_x of 3000 Å was deposited and the contact hole was patterned. Finally, the ITO as a pixel electrode was deposited and then patterned to complete the new SA-TFT.

Second a-Si:H layer of 500 Å was deposited prior to the deposition of n^+ a-Si:H layer in order to increase the on-current. And second a-Si:H layer was deposited at different power of 70 W, 100 W and 200 W in order to investigate its effect on the V_{th}.

The overlap length was measured by the scanning electron microscope (SEM). Transfer curves and output curves were measured with HP4145B parameter analyzer. The least-square method was used to extract parameters such as V_{th} from $I_d^{1/2}$ vs V_d curves. The depth profiling was performed by secondary ion mass spectroscopy (SIMS) in order to determine the composition profile at the interface between second a-Si:H and damaged gate insulator SiN_x.

RESULTS AND DISCUSSION

Figure 1 shows the top view of the new SA-TFT with second a-Si:H layer. The completed overlap length is about 0.8 μm which means that the undercut of E/S SiN_x is about 0.3 μm below the E/S photo resist pattern. Because the RIE etching method is an anisotropic process, it is much easier to control the undercut length of the E/S SiN_x by RIE method than by wet etching method with BHF.

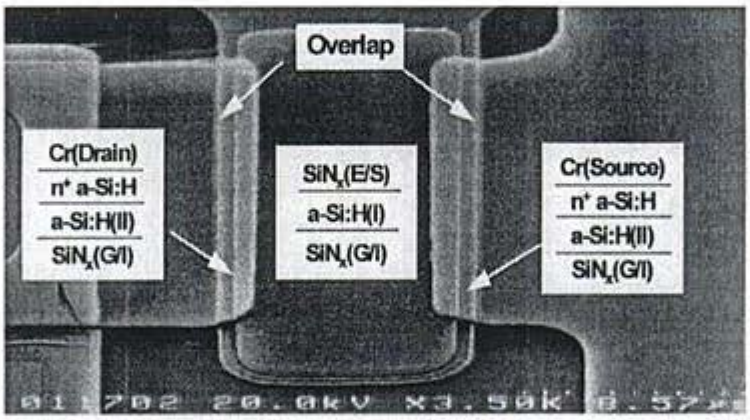

Fig. 1 . The vertical and top view of new self-aligned TFT.

The stacked layers at the overlap region consist of Cr / n^+ a-Si:H / second a-Si:H / SiN_x. Therefore, there is no increase of the contact resistance by the second a-Si:H layer compared to the conventional SA-TFT.

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