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Cu/CuMg Gate Electrode for the Application of Hydrogenated Amorphous Silicon Thin-Film Transistors

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The feasibility of using Cu/CuMg as a gate electrode for a-Si:H thin-film transistors (TFTs) has been investigated in this work. The issue of adhesion between the Cu film and glass substrates has been overcome by introducing the Cu/CuMg alloy. Furthermore, a wet-etching process of Cu-based gate metal has been proposed by using the copper etchant in the conventional printed circuit boards. The experimental result showed superior performance of a-Si:H TFT with desired electrode taper angle and minimal loss of critical dimension. The a-Si:H TFT exhibited mobility of 0.37 cm^2/V s, subthreshold slope of 0.83 V/dec, and V_{th} of 2.02 V.
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Copper metallization has received increasing attention in both microelectronics[1,2] and the large-area and high-resolution active matrix liquid-crystal displays (AM-LCDs),[3] because resistance-capacitance (RC) time delay can be reduced considerably by employing low electrical resistivity metallurgy. Moreover, double-frequency addressing has been proposed to improve the moving image quality by reducing the motion blur of thin-film transistor (TFT)-LCDs. However, the double-rate operation also shortens the device charging time and therefore reduces the TFT-LCD brightness.[4,5] To reduce the RC delay effectively, either the gate busline thickness or width needs to be increased to reduce the line resistance. However, large busline width is not desirable, because it may not only reduce the pixel aperture-ratio but may also increase the line capacitance (crossover and busline-to-common electrode capacitances). To increase the busline thickness, taper edge formation of the gate has to be developed to prevent crossover and interlayer defects due to the poor step coverage and the pinhole formation through the gate insulators. Unfortunately, this process is not available at the present time and it is very difficult to develop. This has led to the introduction of copper metallization to silicon integrated circuits despite the challenges that copper poses to the fabrication processing and the fact that it is a potential lifetime killer. However, the use of Cu has also been hampered by its poor adhesion to the glass substrates and taper angle of the multilayer metal etching process. Several technologies have been used to break through these problems. First, self-passivated Cu gates with MgO and CrO were investigated. Annealing Cu alloy at 350–500°C in an O_2 environment gives rise to the self-passivation of Cu by forming metal oxide, which showed good adhesion to the substrate glass and good stability of Cu. Also, the efficient passivation of Cu electrode can be performed by all plasma-enhanced chemical vapor deposition (PECVD) processes.[6-8] Second, an insertion of an indium tin oxide (ITO) layer between the glass substrate and Cu gate showed a good adhesion to the glass substrate.[9] However, the former approach suffers a high temperature process and the resistivity may be increased due to the doping metal element. As for the second approach, the development of the etchant is difficult because of the galvanic effect of the dissimilar metals in the etchant. Third, the Al_2O_3 buffer layer formed by plasma improves the adhesion to the glass substrate and AlN formed by plasma protects the Cu diffusion to the TFT and plasma damage during the deposition of silicon–nitride layer.[10] However, the thin Al_2O_3 buffer layer and AlN layer suffered from the process stability. The deposition of a CuMg alloy film has been reported by Lee et al. to form a MgO/Cu bilayer structure with low Cu resistivity and good adhesion to SiO_2, although a higher leakage current density has been observed in this structure.[11] In this paper, the Cu/CuMg alloy bilayer structure with similar Cu resistivity was studied in the gate metal structure for a good adhesion layer and provided a good taper angle of metal gate electrode after multilayer metal-etching process.

Experimental

A thin CuMg alloy layer (50 nm) was deposited onto a glass substrate by dc magnetron sputtering at 99.99% purity level of CuMg alloy target (4.5 atom % Mg) at room temperature. Afterward, a 300 nm thick Cu layer was continuously deposited by sputtering on the CuMg alloy layer without breaking the vacuum. The sputtering conditions of Cu and CuMg alloy were as follows. The base pressure of the deposition chamber was 7.0×10^{-7} Torr, Ar pressure 6 mTorr, power 1500 W, and the substrate temperature was at room temperature. The resistivity of the metal film was measured by four-point probe. To investigate the adhesion ability between the Cu/CuMg alloy and glass substrates, the 3M 610-tape test technology was performed. The taper angle of the Cu/CuMg alloy structure after the etch process was also confirmed by scanning electron microscopy (SEM) and optical microscopy (OM). The gate metal hillock issue of the Cu/CuMg alloy structure was also confirmed via SEM and OM observation. After patterning the Cu/CuMg alloy gate electrodes, the a-Si:H TFT devices were fabricated by depositing a 300 nm thick silicon–nitride (SiN_x), a 200 nm thick a-Si:H active layer, and a 50 nm thick n^+-a-Si:H layer subsequently onto the Cu/CuMg alloy gate using PECVD. After the Si active islands were patterned, an Al metal layer was deposited by sputtering and patterned for forming source/drain electrodes. Finally, the n^+-a-Si:H layer on the TFT channel region was etched via the source/drain pattern electrodes as the etching mask. The detailed process flow was illustrated in Fig. 1. The dimensions of channel length and width were both 20 μm for the TFT devices. The electrical measurement was carried out on a HP 4156C precision semiconductor parameter analyzer.

Results and Discussion

Table I shows the comparison of resistivity and adhesion between different Cu metals and glass substrate using the 3M-610 tape test method. The alloy resistivity is increased from 2.6 to 8.7 μΩ cm with doping elements. Although the resistivity of pure Cu film is only 2.6 μΩ cm, the 3M tape test failed due to the poor adhesion of Cu film on the glass substrate. Doping the Mg element

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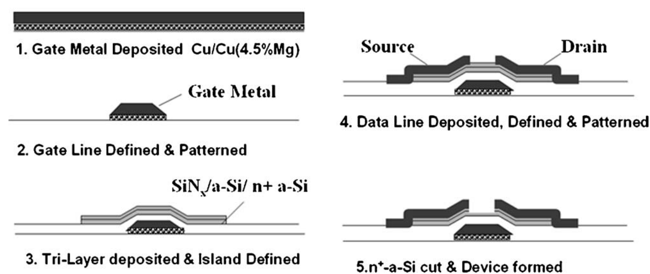

Figure 1. Detailed process flow of the Cu/CuMg gate a-Si:H TFT with the back-channel-etched (BCE) inverted-staggered TFT structure.

into Cu could improve the adhesion and could pass the 3M tape test. This is because the Mg could easily form the MgO layer between the glass substrate and Cu during the sputtering process. As a result, the CuMg alloy film acting as a buffer layer could improve the adhesion between the Cu and glass substrates. By using the Cu/CuMg alloy structure, therefore, a low-resistance metal line with good adhesion can be obtained experimentally. The gate metal structure of Cu/CuMg alloy has low resistivity compared with the pure Cu film and could pass the 3M tape test. Furthermore, the wet-etching process of the Cu/CuMg alloy structure was also successfully completed by introducing the ferric chloride base etchant typically used in printed circuit boards (PCBs). The SEM image shown in Fig. 2 has exhibited a much-desired taper angle (42°) for the Cu/CuMg gate electrode, beneficial for film step coverage and preventing pinhole formation through the gate insulators.[12-15] By decreasing the etching time, the taper angle below 40° could be achieved. The inset in Fig. 2 shows the definition of the taper angle. The conventional value of the taper angle used in the TFT-LCD was from 45 to 70°. The etch rate of the Cu/CuMg film was about 1.8 nm/s and the critical dimension loss was less than 1.5 μm. The use of the CuMg film enhances the taper angle, due to the complete wet-etching process of Cu/CuMg materials similar to each other. Figure 3 shows the SEM image of the Cu/CuMg alloy gate after

Table I. The adhesion and resistivity of metal.

	Thickness (nm)	Resistivity (μΩ cm)	3M-610 tape test
Pure Cu	300	2.6	No pass
CuMg alloy	50	8.7	Pass
Cu/CuMg alloy	300/50	2.63	Pass

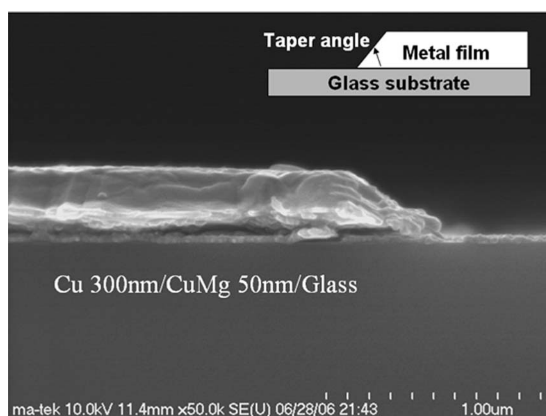

Figure 2. SEM cross-sectional picture of the Cu/CuMg alloy structure after the wet-etching process. (Inset) Definition of taper angle of gate electrode.

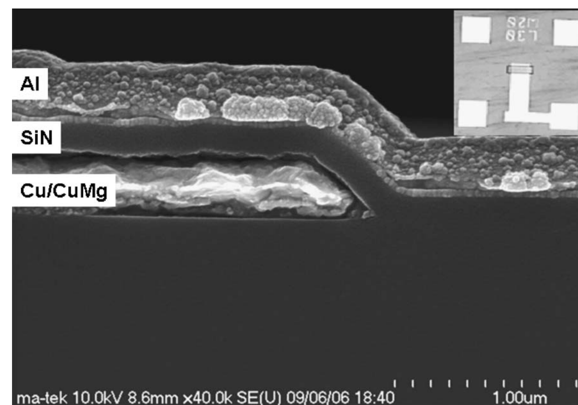

Figure 3. SEM cross-sectional picture of the Cu/CuMg alloy as gate structure after PECVD trilayer dielectrics. (Inset) OM picture of the TFT device after island is defined.

PECVD trilayer dielectrics. Also, the inset shows the OM image of the TFT device after Si island etch. Neither the SEM nor the top-view OM images have shown hillock formation in the thin-film deposition process. Because the metallic Cu has higher heat endurance than Al, the hillock formation was not observed after the PECVD trilayer dielectric film on the gate metal. After a complete TFT manufacture process, the electrical characteristics of a-Si:H TFTs with the Cu/CuMg alloy gate are also investigated, as shown in Fig. 4. Figure 4a shows transfer characteristics of the Cu/CuMg alloy gate a-Si:H TFT measured at the drain voltages of 0.1 and 10 V. The proposed a-Si:H TFT with the Cu/CuMg alloy gate demonstrated the field-effect mobility of 0.37 cm^2/Vs (extracted from the linear I_D-V_G plot, where the $V_D = 0.1$ V), the subthreshold slope of 0.83 V/dec, the threshold voltage of 2.02 V (extracted from the linear I_D-V_G plot, where the $V_D = 0.1$ V), and the I_{ON}/I_{OFF} ratio of 10^6 at $V_D = 10$ V. The gate leakage current through the gate insulator is less than 10^{-13} A. The low gate leakage current is also due to the superior performance of the Cu/CuMg alloy gate electrode with the desired taper angle and nonhillock formation. Furthermore, the output characteristics of a-Si:H TFTs are also shown in Fig. 4b, measured at the gate voltages sweeping from 2 to 8 V by a voltage step of 2 V. No current crowding effect is observed in the Cu/CuMg gate a-Si:H TFT device. This also means that the voltage applied on the TFT was not limited by the source/drain contacted resistance.

Conclusions

A Cu alloy gate a-Si:H TFT device with low resistivity has been developed successfully in this work. The CuMg alloy film acting as a buffer layer could improve the adhesion between the Cu and glass substrates. In addition, the desired taper angle of the Cu/CuMg alloy electrode can be obtained by applying a wet-etch process with a ferric chloride base etchant. Low gate leakage and reliable process was achieved due to the Cu/CuMg electrode with an ideal taper angle and hillock-free dielectric film formation. Compared to the typical a-Si:H TFT, the Cu gate a-Si:H TFT exhibited similar device performance but much lower gate-line resistivity than Al or MoW metal gate line.

Acknowledgments

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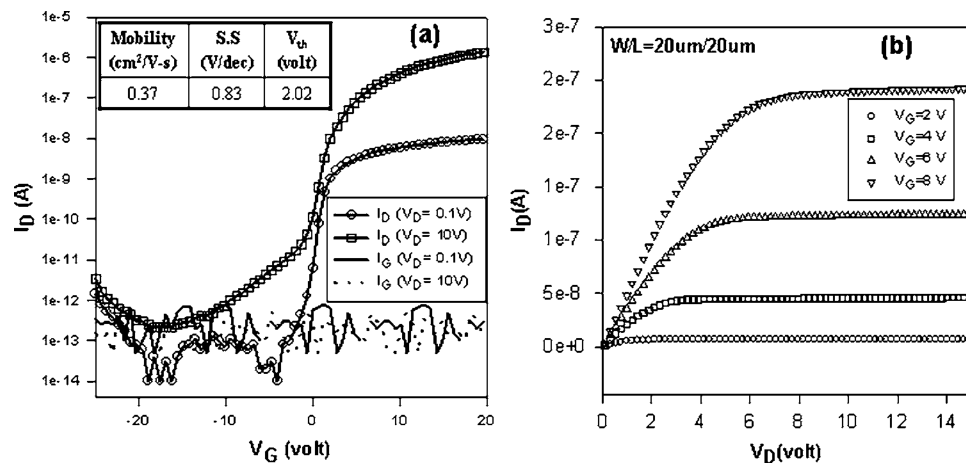

Figure 4. (a) Output characteristics (I_D-V_G curve) of the Cu gate a-Si:H TFT and (b) output characteristics (I_D-V_D curve) of the Cu gate a-Si:H TFT. The channel length and width of TFT devices were 20 μm.

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