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Investigation of intrinsic channel characteristics of hydrogenated amorphous silicon thin-film transistors by gated-four-probe structure

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We use a new hydrogenated amorphous silicon (*a*-Si:H) device structure, the gated-four-probe *a*-Si:H thin-film transistor (TFT), to investigate the intrinsic channel characteristics of inverted-staggered *a*-Si:H TFTs without the influence of source/drain series resistances. The experimental results have shown that, for the conventional *a*-Si:H TFT structure, the field-effect mobility, threshold voltage, and field-effect channel conductance activation energy have a strong dependence on *a*-Si:H thickness and TFT channel length. On the other hand, for the gated-four-probe *a*-Si:H TFT structure, these values are *a*-Si:H thickness and TFT channel length independent, clearly indicating that this new *a*-Si:H TFT structure can be effectively used to measure the channel intrinsic properties of *a*-Si:H TFTs. © *1998 American Institute of Physics.* [S0003-6951(98)04622-1]

Among the existing hydrogenated amorphous silicon (*a*-Si:H) thin-film transistor (TFT) structures, the *n*-channel inverted-staggered TFT structure is the most popular in active-matrix liquid-crystal displays (AMLCDs) and image sensors.[1] In this *n*-channel inverted-staggered TFT structure, the gate electrode is separated from the source and drain electrodes by a gate insulator (amorphous silicon nitride), an intrinsic *a*-Si:H, and a phosphorus-doped ($n+$) *a*-Si:H layer. Under a positive above-threshold gate bias, an accumulation layer of electrons is induced to form a conducting channel near the *a*-Si:H/amorphous silicon nitride (*a*-SiN_x:H) interface. Because of such inverted-staggered structure, the electrical performance of *a*-Si:H TFTs is determined by two factors: the intrinsic channel characteristics and parasitic series resistances. The characteristics of the intrinsic channel are mainly determined by the electronic quality of *a*-Si:H/*a*-SiN_x:H interface, *a*-Si:H bulk, and back-channel interface. On the other hand, the properties of parasitic resistances are affected by the quality of contacts between source/drain metal and $n+$ *a*-Si:H, intrinsic *a*-Si:H and $n+$ *a*-Si:H film thickness, and gate-to-source/drain electrode overlap. The existence of parasitic series resistances makes it difficult to accurately determine *a*-Si:H TFT intrinsic characteristics such as field-effect mobility (μ_{FE}) and threshold voltage (V_T) for optimized *a*-Si:H bulk material and *a*-Si:H/*a*-SiN_x:H interface. To study the intrinsic performance of *a*-Si:H TFTs, the effects of source/drain series resistances must be excluded.

We previously reported a new structure—the gated-four-probe (GFP) *a*-Si:H TFT—to accurately measure the intrinsic characteristics of *a*-Si:H TFTs.[2] In the GFP *a*-Si:H TFT structure, two additional narrow probes are placed between the source and drain electrodes of a conventional inverted-staggered *a*-Si:H TFT to sense the voltage difference along the conducting channel. By correlating this voltage difference with the source/drain current induced by the applied gate bias, the *a*-Si:H TFT intrinsic channel characteristics for electron conduction can be measured without the influence of source/drain series resistances. In a previous study,[3] we employed a two-dimensional device simulator to predict the electrical characteristics of the new GFP *a*-Si:H TFT structure. The simulation results indicated that the effect of series resistances can be excluded in GFP *a*-Si:H TFTs, and determination of the intrinsic characteristics of *a*-Si:H TFTs is possible with this new structure.

In this letter, we present experimental results for conventional inverted-staggered and GFP *a*-Si:H TFTs structures, which were fabricated at the same time on glass substrates (Corning 7059F). A 1500 Å thick chromium (Cr) layer was first deposited by sputtering and patterned to form the gate electrode. Following the gate electrode formation, a 3000 Å thick *a*-SiN_x:H gate insulator, intrinsic *a*-Si:H channel layer (having thicknesses of 1500 and 3000 Å), and 500 Å thick $n+$ *a*-Si:H layer were deposited consecutively by plasma-enhanced chemical vapor deposition. A 2000 Å thick Cr layer was then deposited by sputtering and patterned as source/drain electrodes and, for GFP TFTs, two additional narrow probes have been added. After the source/drain/probe patterning, a dry back-channel-etch process was used to remove the $n+$ *a*-Si:H using the patterned source/drain electrodes as the mask. To insure complete removal of $n+$ *a*-Si:H in the channel region, an over-etch process was used to etch off approximately 200 Å of intrinsic *a*-Si:H layer within the channel.

An HP4156A semiconductor parameter analyzer was used to measure the current-voltage ($I-V$) characteristics at different temperatures. For the *a*-Si:H TFT, the gradual channel approximation equation in the linear region, $G = I_D/W V_D = \mu_{FE} C_i (V_G - V_T)$, was used for μ_{FE} and V_T

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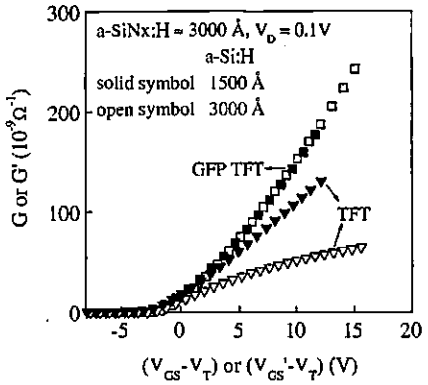


FIG. 1. Sheet conductance vs effective gate voltage characteristics for conventional *a*-Si:H TFT and GFP *a*-Si:H TFT structures having two different *a*-Si:H layer thicknesses. (*W*/*L*) for the conventional *a*-Si:H TFT and GFP *a*-Si:H TFT are (56/16) and (100/20), respectively. V_T (1500 Å)≈5.8 V and V_T (3000 Å)≈2.5 V. Thickness of gate insulator (*a*-SiN_x:H) is fixed at 3000 Å.

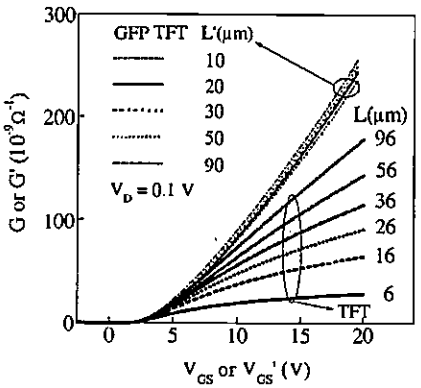


FIG. 2. Sheet conductance vs effective gate voltage characteristics for conventional *a*-Si:H TFT and GFP *a*-Si:H TFT structures having different channel lengths. *a*-Si:H and *a*-SiN_x:H films are both about 3000 Å thick.

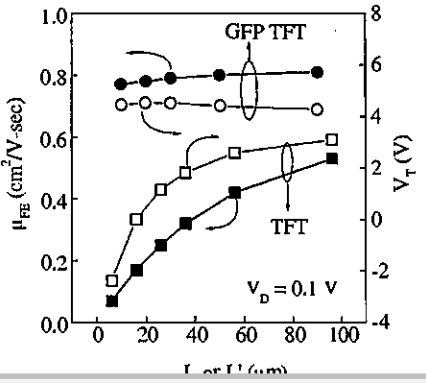
extraction, where G is the normalized channel conductance, C_i is the geometrical capacitance of the gate insulator, V_G is the applied gate bias, and W and L are the channel width and length. For the GFP *a*-Si:H TFT structure, the device characteristics can be expressed as $G' = I_D L'/W(V_B - V_A) = C_i \mu_{FE}(V'_{GS} - V_T)$, where G' is the effective normalized channel conductance, V_A and V_B are the electrical potential for the two inner probes, $V'_{GS} = V_{GS} - (V_B + V_A)/2$ is the effective gate bias, and $L' = (X_B - X_A)$ is the effective channel length. Since probes A and B only sense the electrical potential, V_A and V_B represent the true channel electrical potential. Hence, by using the GFP *a*-Si:H TFT structure, intrinsic field-effect mobility and intrinsic threshold voltage can be extracted from this equation without the influence of source/drain series resistances. The field-effect channel conductance activation energy (E_A) at different gate voltages was obtained from the slope of the Arrhenius ln(G) vs T^{-1} plot, as $G \approx G_0 \exp(-E_A/kT)$, where G_0 is a constant, k is the Boltzmann constant, and T is the absolute temperature.

Figure 1 shows the $G - V_{GS}$ and $G' - V'_{GS}$ characteristics in the linear region obtained for both *a*-Si:H TFT and GFP *a*-Si:H TFT structures having *a*-Si:H layers 1500 and 3000 Å thick. By fitting the experimental data to the above equations, we obtained for GFP *a*-Si:H TFTs the intrinsic field-effect mobility of about 0.85 cm^2/V s. An effective gate bias, $V_{GS} - V_T$ or $V'_{GS} - V_T$, was used in Fig. 1 to offset the effect of back-interface defect states on the threshold voltage; V_T is 2.5 and 6 V for TFTs with 3000 and 1500 Å *a*-Si:H films, respectively. As can be seen in Fig. 1, a thicker *a*-Si:H layer (3000 Å) causes a stronger reduction in the source-drain conductance of *a*-Si:H TFTs at higher gate voltages, indicating that a thicker *a*-Si:H layer introduces a higher device series resistance. However, for GFP *a*-Si:H TFTs, the $G' - (V'_{GS} - V_T)$ characteristics are nominally independent of *a*-Si:H film thickness, indicating that the effect of TFT series resistances has been excluded in this structure, which is consistent with the simulated data.[3]

The $G - V_{GS}$ and $G' - V'_{GS}$ characteristics for *a*-Si:H

length TFT. Again, this is due to the effect of source/drain series resistances, which becomes stronger in *a*-Si:H TFTs with shorter channel lengths.[4] For GFP *a*-Si:H TFTs, no substantial channel length dependence is observed in the $G' - V'_{GS}$ characteristics. Figure 3 shows the evolution of the field-effect mobilities and threshold voltages, extracted from Fig. 2, with channel lengths for both conventional *a*-Si:H TFTs and GFP *a*-Si:H TFTs. As predicted by the numerical simulation,[3] no dependence on channel length is observed for GFP *a*-Si:H TFTs. For *a*-Si:H TFTs, a strong dependence on channel length is observed, where longer channel length devices have higher extracted field-effect mobilities. This result clearly illustrates that the GFP *a*-Si:H TFT structure can effectively eliminate the effect of series resistances and provide the intrinsic device properties.

The field-effect channel conductance activation energy (E_A) is associated with the position of the Fermi level (E_F) in *a*-Si:H that can be changed by gate biases. Its evolution with V_{GS} was used to calculate the density of states in *a*-Si:H TFTs.[5] Therefore, it is critical to know the exact E_A values at different gate biases. As shown above, the series resistance has a significant effect on the overall source-to-drain conduction characteristics, especially for shorter channel length TFTs. It is expected, therefore, that series resistances will influence the determination of E_A values, and the extent of that influence depends on the *a*-Si:H film thickness and the channel length.[6] Figure 4 shows the evolution of E_A with



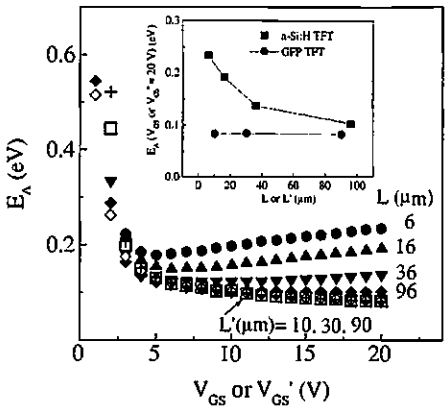


FIG. 4. Evolution of the channel conductance activation energy as a function of gate voltages for conventional *a*-Si:H TFT and GFP *a*-Si:H TFT structures. The channel length for *a*-Si:H TFTs is 6 μm (●), 16 μm (▲), 36 μm (▼), and 96 μm (◆); channel length for GFP TFTs is 10 μm (□), 30 μm (◇), and 96 μm (+). Channel widths for *a*-Si:H TFT and GFP TFT are 60 and 100 μm, respectively. Thickness of *a*-Si:H layer is 3000 Å. E_A at V_{GS} (or V_{GS}') = 20 V as a function of channel length is shown in the inset.

V_{GS} obtained for *a*-Si:H TFT and GFP *a*-Si:H TFT structures, where *a*-Si:H thickness is 3000 Å. At a higher gate bias (V_{GS}=20 V), the extracted E_A values are 0.23, 0.19, 0.14, and 0.10 eV for *a*-Si:H TFTs with channel lengths of 6, 16, 36, and 96 μm, respectively. For V_{GS} above the threshold voltage, E_A increases with increasing V_{GS} for a short channel length TFT (L=6 μm), while it saturates at higher V_{GS} for a longer channel TFT (L=96 μm). This channel-length dependence of E_A is mainly due to the increasing influence of series resistances on TFT conduction characteristics with decreasing channel length and increasing gate voltage; variation of E_A with L at V_{GS}=20 V is shown in the inset of Fig. 4. On the other hand, for a GFP *a*-Si:H TFT with different channel lengths (10, 30, and 90 μm), the E_A value decreases with increasing effective gate bias, which indicates that E_F approaches the conduction band-edge as gate-bias increases. In addition, E_A values extracted for GFP TFTs do not depend on channel length (see inset of Fig. 4). This observation is consistent with theoretical calculation,[3] since the effect of source/drain series resistances have been excluded in this structure. Hence, the E_A value obtained for GFP *a*-Si:H TFTs represents the true intrinsic E_A value that can be used to characterize the quality of *a*-Si:H TFT channel (including the *a*-Si:H/*a*-SiN_x:H interface).

In this letter we have shown the experimental results for GFP *a*-Si:H TFTs that confirm our previous numerical simulation[3] indicating that GFP *a*-Si:H TFTs are immune to the influence of source/drain series resistances. This work clearly demonstrates that the GFP *a*-Si:H TFT structure is a very useful tool for optimization and control of the intrinsic performance of *a*-Si:H TFTs during AMLCD fabrication.

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