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(54) [Name of Invention] Thin-film Electric Field-effect Transistor Substrate

(57) [Abstract]

[Object] To reduce mask costs by making thin-film transistor substrate connection terminal part patterns identical regardless of the manufacturing process.

[Composition] Contact holes 2 are fabricated in an insulating layer 5 on top of an underlying metal layer 1. The contact holes 2 are fabricated on only a portion of the top part of the underlying metal layer 1. An overlay metal layer 3 completely covers the contact holes 2, and the surface area thereof is less than half the surface area of a transparent metal layer 4 of the terminal part top layer contact surface. Regardless of the sequence in which the overlay metal layer 3 and the transparent metal layer 4 are fabricated, more than half of the terminal part surface area is the transparent metal layer 4.

[INSERT FIGURES]

[Patent Claim]

[Claim 1] A thin-film electric field-effect transistor substrate, wherein, in a contact terminal part comprising, at least, an underlying metal layer, an insulating layer, contact holes, an overlay metal layer, and a transparent metal layer, at the periphery part of a thin-film electric field-effect transistor substrate fabricated with multiple scan lines laid out in parallel and multiple signal lines laid out in parallel so as to intersect each other, with thin-film electric field-effect transistors fabricated at each intersection between said scan lines and said signal lines, said contact holes are fabricated on only a portion of the area on top of said underlying metal layer, said overlay metal layer completely covers said contact holes, and at least a part of said transparent metal layer is fabricated as the top layer.

[Detailed Explanation of the Invention]

[0001]

[Area of Use in Industry]

The present invention relates to thin-film field transistor-drive liquid crystal display devices, and in particular, relates to thin-film field-effect transistor substrates.

[0002]

[Prior Art] Liquid crystal displays have been developed as flat panel display for portable computers and pocket television sets, and of these [liquid crystal displays], active matrix-type displays, wherein thin-film field-effect transistors are fabricated in an array on a glass substrate and are used as switches for each pixel, have been actively developed and commercialized by a variety of organizations as space-saving and power-saving displays because they are capable of producing full-color displays on par with those of cathode ray tubes. It is imperative to decrease their cost and increase their reliability if these active matrix liquid crystal displays are to be accepted broadly.

[0003] In thin-film field-effect transistor-driven liquid crystal display devices, the thin-film field-effect transistors are used as switching elements. Figure 6 shows a planar view of a conventional thin field-effect transistor substrate terminal part and a display element array part thin-film field-effect transistor that use amorphous silicon hydride [sic?] thin-film field-effect transistors as the switching elements. Figure 7 (a) shows a cross-sectional diagram along the sections E-E' and F-F' in the terminal part in Figure 6. Furthermore, Figure 7 (b) shows a cross-sectional drawing along the section G-G' in the thin-film field-effect transistor of Figure 6. Figure 8 shows a planar view of a thin-film field-effect transistor substrate terminal part and a display element array part thin-film field-effect transistor with another conventional structure. Figure 9 (a) is a cross-sectional drawing along the sections H-H' and I-I' in the terminal part in Figure 8. Figure 9 (b) is a cross-sectional drawing along the section J-J' in the thin-film field-effect transistor in Figure 8.

[0004] In Figures 6 and 9, 1 is a terminal part underlying metal layer, 5 is an insulating layer, 2 is a contact hole that in the insulating layer 5, 3 is an overlay metal layer, 4 is a transparent metal layer, 6 is a scan line, 7 is a gate electrode, 8 is amorphous silicon, 9 is amorphous silicon doped with phosphorous, 10 is a signal line, 11 is a source electrode, 12 is a drain electrode, 13 is a pixel electrode, and 14 is a glass substrate. Furthermore, the part shown by the dotted line in Figure 7 (a) is a part of an external circuit, where 20 is a base file [SIC - "film?"], 21 is a copper plate interconnect pattern, 22 is a thermally curable resin, and 16 is a metal particle (solder).

[0005] In actual thin-film field-effect transistor substrates, the scan lines 6 and signal lines 10 in Figures 6 and 8 are laid out in the form of a matrix, where thin-film field-effect transistors are fabricated in the vicinity of the intersections between the scan lines 6 and the signal lines 10. The terminal part underlying metal layer 1, scan lines 6, and gate electrodes 7 are all fabricated from the same metal, where the terminal part overlay metal layer 3, the signal lines 10, the source electrodes 11 and the drain electrodes 12 are all fabricated from the same metal [different from the metal mentioned above], and the transparent metal layer 4 in the terminal part and the pixel electrodes 13 are both fabricated from the same metal [which is different from the metals described above].

[0006] One conventional thin-film field-effect transistor substrate structure will be explained by showing the manufacturing process using Figures 6 and 7. First a terminal part underlying metal layer 1, scan lines 6, and gate electrodes 7, made from a 2000 angstrom-thick chrome layer, are fabricated on a glass substrate 14. Next, a gate insulator layer 5, made from a 3000 angstrom-thick silicon nitride layer, a 3000 angstrom-thick amorphous silicon 8, and a 500 angstrom-thick phosphorous-doped amorphous silicon 9 are fabricated sequentially, after which islands, made from the amorphous silicon 8 and the phosphorous-doped silicon 9, are formed on the gate electrodes 7. Next contact holes 2, which make contact with the underlying metal layer 1 in the terminal part, are fabricated in the insulation layer 5 in the terminal part. Chrome is then used to fabricate the terminal part underlying metal layer 3, the signal lines 10, the source electrodes 11, and the drain electrodes 12 to a thickness of 2000 angstroms. After this, the transparent metal layer 4 and the pixel electrodes 13 are fabricated from indium tin oxide (ITO), to a thickness of 500 angstroms. Following these processes, the phosphorous-doped amorphous silicon 9 is removed from between the source electrodes 11 and the drain electrodes 12, producing the thin-film field-effect transistors.

[0007] The connections to the external circuits are made by placing a base film 20, on which a copper plating pattern 21 is fabricated, on a specific location with a thermal curable resin 22, which contains metal particles 16, interposed between [said copper plating pattern 21 and] the transparent metal layer 4. The copper plating pattern 21 and the transparent metal layer 4 are connected to each other through the metal particles 16. The benefit of this structure is that excellent connections can be made because, in the terminal part of Figure 7 (a), the step height part of the contact hole 2 is covered by the terminal part overlay metal layer 3; however, the drawback is that the pixel electrodes 13 become discontinuous at the step height part of the drain electrode 12 terminal in the thin-film field-effect transistor part shown in Figure 7 (b), making the connections unreliable.

[0008] The difference in the other conventional thin-film field-effect transistor substrate structure shown in Figures 8 and 9 is that the terminal part overlay metal layer 3, the signal lines 10, and source electrodes 11, and the drain electrodes 12 are fabricated after fabricating the terminal part transparent metal layer 4 and pixel electrodes 13. The benefit of this structure is that excellent connections are made in the drain electrode 12 terminals in the thin-film field-effect transistors in Figure 9 (b), because the step height part with the pixel electrodes 13 is covered by the top-layer drain electrodes 12; however, the drawback is that the step height parts of the contact holes 2 in the terminal part in Figure 9 (a) are covered only by the transparent metal layer.

[0009] In Figure 7 (a) and Figure 9 (a), the topmost layer in the terminal part is made out of the transparent metal layer 4. The reason for this is that the surface becomes oxidized and thus becomes highly resistant with metals such as chrome, aluminum, or the like, thus degrading the connections with external circuitry and leading to a loss of reliability, so ITO, which is resistant to oxidation because it already contains oxygen, is used as the contact surface with external circuitry, to make low-resistance reliable electrical connections.

[0010]
[Problem Solved by the Present Invention]

Thin-film filed effect transistor substrates of either of the two conventional structures are selected based on requirements such as manufacturing process conditions and the size of the liquid crystal display device. For example, when fabricating ultra fine thin-film field-effect transistors, a manufacturing process is used wherein the drain electrodes are made last, in consideration of the quality of the contacts with the drain electrodes and the pixel electrodes, while a manufacturing process is used wherein it is the pixel electrodes that are fabricated last when fabricating thin-film field-effect transistors that are not so fine. When the planar views in Figure 6 and Figure 8 are examined, the planar views of the thin-film field-effect transistors are identical, but the planar views of the terminal parts are different. This is because when the drain electrode is made first when using a mask pattern for manufacturing with the drain electrode fabricated last, the underlying metal layer is also removed when fabricating the top metal layer, and when the drain electrode is made last using a mask pattern for manufacturing with the drain electrode made first, the surface for connecting with the external circuitry will be the top metal layer instead of the transparent metal layer. In other words, the conventional [approach] required a larger number of masks because, even when thin-film field-effect transistors of identical sizes were fabricated, it was necessary to provide different mask patterns for the photolithography for fabricating the terminal parts.

[0011] The object of the present invention is to provide a thin-film field-effect transistor substrate wherein the same mask pattern can be used regardless of the manufacturing process selected.

[0012]
[Means By Which the Problem Is Solved]

The thin-film field-effect transistor substrate according to the present invention, is a thin-film field-effect transistor wherein, in a contact terminal part comprising, at least, an underlying metal layer, an insulating layer, contact holes, an overlay metal layer, and a transparent metal layer, at the periphery part of a thin-film electric field-effect transistor substrate fabricated with multiple scan lines laid out in parallel and multiple signal lines laid out in parallel so as to intersect each other, with thin-film electric field-effect transistors fabricated at each intersection between said scan lines and said signal lines, said contact holes are fabricated on only a portion of the area on top of said underlying metal layer, said overlay metal layer completely covers said contact holes, and at least a part of said transparent metal layer is fabricated as the top layer.

[0013]
[Example Embodiments]

Figure 1 is a planar view of one example embodiment of a thin-film field-effect transistor substrate according to the present invention. Figures 2 (a) and (b) are cross-sectional drawings of the terminal part. Figure 2 (a) is a cross-sectional drawing along the section A-A' and along the section B-B' in the terminal part in Figure 1 in the case wherein the substrate part top metal layer is fabricated first and the transparent metal layer is fabricated on the surface afterwards. The cross-sectional drawing along the section C-C' in the field-effect transistor part is the same as in the conventional Figure 7 (b). Figure 2 (b) is a cross-sectional drawing along the section A-A' and section B-B' in the terminal part in Figure 1 in the case wherein the transparent metal layer is fabricated first and the top metal layer in the terminal part is fabricated afterward. In this case, the cross-sectional drawing along the section C-C' in thin-film field-effect transistor part is the same as in the conventional Figure 9 (b).

[0014] In Figure 1 and Figure 2, 1 is a the terminal part underlying metal layer, 5 is an insulating layer, 2 is a contact hole in the insulating layer 5, 3 is an overlay metal layer, 4 is a transparent metal layer, 6 is a scan line, 7 is a gate electrode, 8 is amorphous silicon, 9 is phosphorous-doped amorphous silicon, 10 is a signal line, 11 is a source electrode, 12 is a drain electrode, 13 is a pixel electrode, and 14 is a glass substrate.

[0015] Amorphous silicon hydride field-effect transistors are used as switching elements. In actual thin-film field-effect transistor substrates, the scan lines 6 and the signal lines 10 in Figure 1 are laid out in a matrix pattern, where connection terminals are fabricated at the ends of the scan lines 6 and the ends of the signal lines 10, and thin-film field-effect transistors are fabricated in the vicinity of the intersections between these scan lines 6 and the signal lines 10. The terminal part underlying metal layer 1, the scan lines 6, and the gate electrodes 7 are all made from the same metal layer. The terminal part overlay metal layer 3, the signal lines 10, the source electrodes 11, and the drain electrodes 12 are each made from the same metal as each other, and the terminal part transparent metal layer 4 and pixel electrodes 13 are each made of the same metal as each other.

[0016] The thin-film field oxide transistor part (the cross-section along section C-C' in Figure 1) according to the present invention has the same structure as in the conventional Figure 7 (b) and Figure 9 (b). Furthermore, the connections with the external circuits are the same as in Figure 7 (a). The terminal part in this example embodiment will be explained. In Figure 1 and Figure 2, the contact holes are fabricated in only a part over the terminal part underlying layer 1, and the overlay metal layer 3 is of the minimum size required to completely cover contact holes 2.

[0017] In Figure 2 (a) the overlay metal layer 3 is fabricated first, and the transparent metal layer 4 is fabricated afterwards. Because in the contact holes 2 the overlay metal layer 3 covers the step-height part, the electrical contact between the underlying metal layer 1 and the top-most layer, the transparent metal layer 4, is assured. In addition, because the entire surface of the terminal part is the transparent metal layer 4, connections with the outside circuitry can also be made with low resistance.

[0018] On the other hand, in Figure 2 (b) the transparent metal layer 4 is fabricated first, and the overlay metal layer 3 is fabricated afterwards. In the contact hole 2 the overlay metal layer 3 is covered by the transparent metal layer 4 from above at the step height, making a more reliable electrical connection between the underlying metal layer 1 and the transparent metal layer 4. In addition, because most of the surface of the terminal part is the transparent metal layer 4, the electrical connections with the external circuitry are similarly low resistance. The external circuitry can be connected through the surface of the low-resistance transparent metal layer 4 by disposing the transparent metal layer 4 as the top most layer on the terminal part by making the surface area of the overlay metal layer 3 smaller than they of the transparent metal layer 4 on the surface of the terminal part.

[0019] Figure 3 shows a planar view of another example of a terminal part of a thin-film field-effect transistor substrate according to the present invention. In the actual terminal part, the length is several millimeters (in the horizontal direction in Figure 3), and the width is several dozen to several hundred microns (in the vertical direction in Figure 3). The transparent metal layer 4 is highly resistive as a bulk material (as opposed to a surface oxide) when compared to the overlay metal layer 3, and thus, in order to reduce the resistance, the contact holes 2 and overlay metal layer 3 are fabricated in the center of the terminal part as well. In addition, by increasing the number of contact holes, it has been possible to reduce the resistance and increase the reliability of the electrical contacts

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