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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	0756-2237
First Inventor	Yoshiharu HIRAKATA et al.
Title	CONTACT STRUCTURE
Express Mail Label No.	

APPLICATION ELEMENTS

See *MPEP chapter 600 concerning utility patent application contents.*

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status.
   See 37 CFR 1.27
3. ☒ Specification [Total Pages 36]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) *(35 U.S.C. 113)* **Figs. 1-14** *[Total Sheets 13]*
5. Oath or Declaration *[Total Sheets 3]*
   a ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies; or
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
    (when there is an assignee)
11. ☐ English Translation Document *(if applicable)*
12. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☒ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. ☒ Other: Notice of Change of Name and Notice of Change of Address

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/361,218 filed Juy 27, 1999 which itself is a Divisional of Serial No. 09/046,685, filed March 24, 1998 now U.S. Patent 5,982,471.

Prior application information Examiner D. Nguyen Group / Art Unit: 2871

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* 22204 *(Insert Customer No. or Attach bar code label here)* or ☐ *Correspondence address below*

Name	**Eric J. Robinson**				
	NIXON PEABODY LLP				
Address	8180 Greensboro Drive, Suite 800				
City	McLean	State	VA	Zip Code	22102
Country	United States	Telephone	(703) 790-9110	Fax	(703) 883-0370

Name (Print/Type)	**Eric J. Robinson**	Registration No. (Attorney/Agent)	**38,285**
Signature		Date	12/12/00

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FEE TRANSMITTAL FOR FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) **1400.00**

Complete if Known	
Application Number	**Not Yet Assigned**
Filing Date	**December 12, 2000**
First Named Inventor	**Yoshiharu HIRAKATA et al**
Examiner Name	**D. Nguyen**
Group Art Unit	**2871**
Attorney Docket No.	**0756-2237**

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to.

Deposit Account Number: 19-2380

Deposit Account Name: NIXON PEABODY LLP, 8180 Greensboro Drive Suite 800, Mclean, Va. 22102

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☒ **Payment Enclosed:**

☒ Check ☐ Credit Card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Divisional Fling fee	$710 00
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2, EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	30	-20**=	10	X	18.00	=	$180.00
Independent Claims	6	-3** =	3	X	80.00	=	$240 00
Multiple Dependent					270 00	=	$270 00

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) $690.00

**or number previously paid, if greater, For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge – late filing fee or oath	
127	50	227	25	Surcharge – late provisional filing fee or cover sheet	
139	130	139	130	Non-English transaction	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,240	241	620	Petition to revive – unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.29(b))	
179	710	249	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	**Eric J. Robinson**	Registration No. *(Attorney/Agent)*	**38,285**	Telephone	(703) 790-9110
Signature				Date	12/12/00

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NVA139273.1

Docket No.: 0756-2237

/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **DIVISIONAL** Application of	)	
Yoshiharu HIRAKATA et al	)	
Based On Serial No. 09/361,218	)	Art Unit: 2871
Which was filed: July 27, 1999	)	Examiner: D. Nguyen
For: CONTACT STRUCTURE	)	

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 09/361,218 filed July 27, 1999; which itself is a Divisional of Serial No. 09/046,685 filed March 24, 1998 now U.S Patent 5,982,471.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

EJR/sas

Docket No.: 0756-2237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **Divisional** Application of	)	
Yoshiharu HIRAKA et al	)	
Based On Serial No.: 09/361,218	)	Art Unit: 2871
Which was filed: July 27, 1999	)	Examiner: D. Nguyen
For: CONTACT STRUCTURE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, it is requested that the reference listed on the attached Form PTO-1449 be made of record in the above-identified application.

The references listed on the attached Form PTO-1449 were cited in parent application Serial Nos. 09/361,218, 09/046,685.

Respectfully Submittetd,

Eric J. Robinson
Registration No. 38,285

Nixon Peabody LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

ERJ/sas

NVA157161 1

CONTACT STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a contact structure for electrically connecting together conducting lines formed on two opposite substrates, respectively, via conducting spacers and, more particularly, to a contact structure used in common contacts of an electrooptical device such as a liquid crystal display.

Description of the Related Art

In recent years, liquid crystal displays have been extensively used in the display portions of mobile intelligent terminals such as mobile computers and portable telephones including PHS (personal handyphone system). Also, active-matrix liquid crystal displays using TFTs as switching elements are well known.

A liquid crystal display comprises two substrates and a liquid crystal material sealed between them. Electrodes are formed on these two substrates to set up electric fields. A desired image or pattern is displayed by controlling the magnitudes of these electric fields. In the active-matrix liquid crystal display, TFTs (thin-film transistors) are formed on one substrate to control the supply of voltage to each pixel electrode. Therefore, this substrate is referred to as the TFT substrate. A counter electrode placed opposite to the pixel electrodes is formed on the other substrate and so it is referred to as the counter substrate.

In the active matrix display, an electric field is produced between each pixel electrode on the TFT substrate and the counter electrode on the counter substrate, thus

providing a display. The potential at each pixel electrode on the TFT substrate is controlled by the TFT and thus is varied. On the other hand, the counter electrode on the counter substrate is clamped at a common potential. For this purpose, the counter electrode is connected with an extractor terminal via a common contact formed on the TFT substrate. This extractor terminal is connected with an external power supply. This connection structure clamps the counter electrode at the common potential.

The structure of the common contact of the prior art active-matrix liquid crystal display is next described briefly by referring to Figs. 12 - 14.

Fig. 12 is a top plan view of a TFT substrate 10. This TFT substrate comprises a substrate 11 having a pixel region 12, a scanning line driver circuit 13, and a signal line driver circuit 14. In the pixel region 12, pixel electrodes and TFTs connected with the pixel electrodes are arranged in rows and columns. The scanning line driver circuit 13 controls the timing at which each TFT is turned on and off. The signal line driver circuit 14 supplies image data to the pixel electrodes. Furthermore, there are extractor terminals 15 to supply electric power and control signals from the outside. The substrate 11 makes connection with the counter electrode at common contact portions 16a - 16d.

Fig. 13 is a cross-sectional view of the pixel region 12 and a common contact portion 16 representing the common contact portions 16a - 16d. A TFT 17 and many other TFTs (not shown) are fabricated in the pixel region 12 on the substrate 11. An interlayer dielectric film 18 is deposited on the TFT 17. A pixel electrode 19 connected with the drain electrode of the TFT 17 is formed on the interlayer dielectric film 18.

A precursor for the source and drain electrodes of the TFT 17 is patterned into internal conducting lines 21 at the common contact portion 16. The interlayer dielectric film 18 is provided with a rectangular opening. A conducting pad 22 is formed in this opening and connected with the internal conducting lines 21. The pixel electrode 19 and the conducting pad 22 are patterned from the same starting film.

Fig. 14 is a top plan view of the known common contact portion 16. A region located inside the conducting pad 22 and indicated by the broken line corresponds to the opening formed in the interlayer dielectric film 18.

As shown in Fig. 13, a counter electrode 24 consisting of a transparent conducting film is formed on the surface of a counter substrate 23. This counter electrode 24 is opposite to the pixel electrodes 19 in the pixel region 12 and to the conducting pad 22 at the common contact portion 16.

Spherical insulating spacers 25 are located in the pixel region 12 to maintain the spacing between the substrates 11 and 23. A spherical conducting spacer 26 is positioned at the common contact portion 16 and electrically connects the counter electrode 24 with the conducting pad 22. The pad 22 is electrically connected with the internal conducting lines 21, which in turn are electrically connected with an extractor terminal 15. This connection structure connects the counter electrode 24 on the counter substrate 23 with the extractor terminal 15 on the substrate 11.

In the prior art liquid crystal display, the interlayer dielectric film 18 is provided with the opening at the common contact portion 16, as shown in Fig. 13. Therefore, the cell gap G_c in the common contact portion is almost equal

to the sum of the cell gap G_p in the pixel region + the film thickness t of the interlayer dielectric film 18.

The cell gap G_p (also known as the cell spacing) in the pixel region 12 is determined by the insulating spacers 25. It is common practice to use standardized spacers as the insulating spacers 25 and so if the spacers 25 have a uniform diameter, the cell gap G_p in the pixel region 12 is substantially uniform among liquid-crystal cells. However, it is difficult to avoid nonuniformity of the cell gap G_c in the common contact portion among liquid-crystal cells.

The cell gap G_c in the common contact portion is constant since the cell gap G_p is constant because of the relation described above. Therefore, the cell gap G_c in the common contact portion depends only on the film thickness t of the interlayer dielectric film 18. Consequently, to make the cell gap G_c uniform among liquid-crystal cells, it is necessary that the film thickness t of this interlayer dielectric film 18 be uniform among cells. However, this is impossible to circumvent.

Normally, the common contact portions of the liquid crystal display are 2 to 4 in number. The film thickness t of the interlayer dielectric film 18 may differ from location to location on the same substrate. In this case, the film thickness t may differ among different common contacts even on the same substrate.

Because of the aforementioned nonuniformity of the thickness t of the interlayer dielectric film 18, the cell gap G_c in the common contact portion differs among different cells or different common contacts. Furthermore, the nonuniformity of the cell gap G_c results in the cell gap G_p in the pixel region to be nonuniform.

The cell gap G_p in the pixel region is affected more by the nonuniformity of the cell gap G_c in the common contact portion as the area of the pixel region 12 becomes narrower than the area of the common contact portion. Especially, in the case of a projection display as used in a projector, the problem of above-described nonuniformity of the cell gap G_p in the pixel region becomes conspicuous, because it is a quite accurate small-sized display of about 1 to 2 inches.

A standardized spacer is also used as the conducting spacer 26. The diameter of this conducting spacer 26 is determined by the diameter of the insulating spacers 25 in the pixel region 12 and by the design thickness of the interlayer dielectric film 18. Where the thickness of the interlayer dielectric film 18 is much larger than the designed value, the cell gap G_c in the common contact portion becomes very large. This makes it impossible to connect the counter electrode with the conducting pad well by the conducting spacer 26. In consequence, the counter electrode cannot be clamped at the common potential. As a result, a display cannot be provided.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a contact structure which is free of the foregoing problems, provides less nonuniform cell gap among different cells if the thickness of the interlayer dielectric film is nonuniform across the cell or among different cells, and reduces poor electrical contacts which would normally be caused by conducting spacers.

This object is achieved in accordance with the teachings of the invention by a contact structure for connecting a conducting film formed on a first substrate

with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film by selectively leaving the dielectric film; a second conducting film covering the dielectric film left and the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the dielectric film left. The conducting spacers maintain the cell gap between the first and second substrates.

One embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film; an insulator deposited on only portions of the first conducting film exposed through the openings; a second conducting film covering the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates and connecting the second and

third conducting films. The second conducting film is connected with the first conducting film through the openings extending through the insulator. The second conducting film, the conducting spacers, and the third conducting film are connected in turn through the openings extending through the insulator. The conducting spacers maintain the cell gap between the first and second substrates.

Another embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate of an electrooptical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereover, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film by selectively leaving the interlayer dielectric film;a second conducting film defining the counter electrode formed on the second substrate; a third conducting film covering the interlayer dielectric film left and the openings; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings. The third conducting film and the pixel electrodes are formed from a common starting film. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the dielectric film left. The conducting spacers maintain the spacing between the first and second

substrates.

A further embodiment of the invention resides in a contact structure for connecting a first conducting film formed over a first substrate of an electrooptical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereon, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film; an insulator formed on selected portions of the surface of the first conducting film extending through the openings; a second conducting film covering the openings; a third conducting film defining the counter electrode formed on the second substrate; conducting spacers held between the first and second substrates and connecting the second and third conducting films. The pixel electrodes and the second conducting film are formed from a common starting film. The second conducting film is connected with the first conducting film through the openings extending through the insulator. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the insulator formed in the openings. The conducting spacers maintain the cell gap between the first and second substrates.

A still other embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first

and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film and exposing parts of the first conducting film; a second conducting film covering the openings;a third conducting film formed over the second substrate;a fourth conducting film formed between the second substrate and the third conducting film and in contact with the third conducting film; and conducting spacers held between the first and second substrates. The first conducting film, the second conducting film, the conducting spacers, the third conducting film, and the fourth conducting films are connected in turn through the openings. The spacers maintain the cell gap between the first and second substrates.

Other objects and features of the invention will appear in the course of the description thereof, which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a fragmentary cross-sectional view of a common contact portion in accordance with the present invention;

Figs. 2A and 2B are top plan views of the common contact portion shown in Fig. 1;

Fig. 3 is a top plan view of the TFT substrate of a liquid crystal display in accordance with Example 1 of the invention;

Fig. 4 is a top plan view of the counter substrate of the liquid crystal display in accordance with Example 1;

Figs. 5A - 5G are cross-sectional views illustrating a process sequence for fabricating the TFT substrate shown in Fig. 3;

Fig. 6 is a fragmentary cross-sectional view of a pixel region and a common contact portion of the liquid crystal display in accordance with Example 1;

Fig. 7 is a cross-sectional view similar to Fig. 6, but illustrating Example 2 of the invention;

Fig. 8 is a cross-sectional view similar to Fig. 6, but illustrating Example 3 of the invention;

Fig. 9 is an enlarged cross-sectional view of the common contact portion shown in Fig. 7;

Fig. 10 is an enlarged cross-sectional view of the common contact portion shown in Fig. 8;

Fig. 11 is a top plan view of the common contact portion shown in Fig. 8;

Fig. 12 is a top plan view of the TFT substrate of the prior art liquid crystal display;

Fig. 13 is a cross-sectional view of a pixel region and a common contact portion on the TFT substrate shown in Fig. 12; and

Fig. 14 is a top plan view of the common contact portion shown in Fig. 13.

DETAILED DESCRIPTION OF THE INVENTION

EMBODIMENT 1

The present embodiment of this invention is described by referring to Figs. 1, 2A and 2B. Fig. 1 is a fragmentary cross-sectional view of a common contact portion of a liquid crystal display in accordance with the present embodiment. Figs. 2A and 2B are top plan views of the TFT substrate of the liquid crystal display. The structure of a region 120 shown in Fig. 2A is depicted in the enlarged cross section of Fig. 1.

As shown in Fig. 13, in the prior art structure, the

spacers in the pixel region 12 are located over the interlayer insulating film 18 via the pixel electrode 19. However, the interlayer dielectric film 18 does not exist under the conducting pad 22 at the common contact portion 16. Hence, the cell gap G_c in the common contact portion depends on the thickness of the interlayer dielectric film 18.

Accordingly, in the present embodiment, an insulator, or a dielectric, is inserted under the conducting pad in the common contact portion. Conducting spacers are placed on top of the dielectric, so that the cell gap G_c in the contact portion does not depend on the thickness of the interlayer dielectric film 18. In the present embodiment, openings are formed, selectively leaving the interlayer dielectric film 18.

In the present embodiment, as shown in Fig. 1, a first conducting film 103 is formed on a first substrate 101. A dielectric film 104 is deposited on the first conducting film 103. The dielectric film 104 is selectively left to form openings 111 that expose parts of the first conducting film 103. A second conducting film 105 is formed so as to cover the left parts of the dielectric film, 104a, and the openings 111.

A third conducting film 106 is formed on the second substrate 102. Conducting spacers 107 are sandwiched between the first substrate 101 and the second substrate 102.

In the prior art opening 110 shown in Fig. 2A, the dielectric film 104 has been fully removed. In the present embodiment, the dielectric film 104 is selectively left to form the dielectric film portions 104a and the openings 111. The openings 111 expose parts of the first conducting film

103. The first conducting film 103 is connected with the second conducting film 105 at these openings 111.

On the first substrate 101, the left dielectric film 104a is closest to the second substrate 102; therefore, on the left dielectric film 104a, the second conducting film 105 formed on the first substrate electrically connects with the third conducting film 106 formed on the second conducting film 102 through the conducting spacer 107, as shown in Fig. 1.

In region 110, the left dielectric film 104a is closest to the second substrate; therefore, the conducting spacers 107 electrically connecting the second conducting film 105 with the third conducting film 106 maintain the gap G between the substrates. Consequently, this gap G is dependent only on the size of the conducting spacers 107. Therefore, where the conducting spacers 107 are uniform among liquid-crystal cells, the gap G can be made uniform among cells, even if the thickness t of the dielectric film 104 differs among cells.

In the present embodiment, it is desired that the area of each opening 111 be sufficiently larger than the area occupied by each conducting spacer and offer space so that the conducting spacers can move freely, because the spacers 107 existing in the openings 111 do not contribute toward maintaining the gap. Otherwise, plural conducting spacers 107 would be stacked on top of each other, making it impossible to maintain the cell gap G uniform across the cell.

Also in the present embodiment, it is desirable that the area of the surface of each left dielectric film portion 104a be sufficiently larger than the area occupied by each conducting spacer 107, assuring arrangement of the

conducting spacers 107. If the spacers 107 are not positioned over the dielectric film 104a with certainty, it will not be possible to make electrical connections between the first and second substrates. Furthermore, the gap will not be maintained.

The openings 111 are formed as shown in Fig. 2A in the present embodiment. The relation between the left dielectric film 104a and each opening 111 may be reversed as shown in Fig. 2B. It is that noted Fig. 1 is an enlarged view of the region 120 indicated by the broken line in Fig. 2B.

EMBODIMENT 2

The present embodiment is described by referring to Figs. 1 and 2A. Fig. 1 is a cross-sectional view of a common contact portion of the liquid crystal display in accordance with the present embodiment. Fig. 2A is a top plan view of the TFT substrate of the liquid crystal display. Fig. 1 is an enlarged cross-sectional view of the region 120 indicated by the broken line in Fig. 2A.

A dielectric is inserted under a conducting pad in the common contact portion, in the same manner as in Embodiment 1. Conducting spacers are positioned on the dielectric. Thus, the cell gap G_c in the common contact portion does not depend on the thickness of the interlayer dielectric film 18. The present embodiment is characterized in that the dielectric film 18 is selectively left to form openings.

In particular, in the present embodiment, the dielectric layer is formed underneath the conducting pad 22. The conducting spacers are positioned on the dielectric. Consequently, the cell gap G_c in the common contact portion is not dependent on the thickness of the interlayer

dielectric film 18.

Referring to Fig. 1, a first conducting film 103 is formed on top of a first substrate 101. A dielectric film 104 covers the first conducting film 103. The dielectric film 104 is provided with openings 111 to selectively expose the surface of the first conducting film 103. The exposed portions of the dielectric 104 are indicated by 104a. A second conducting film 105 is formed to cover the openings 111.

A third conducting film 106 is formed on the second substrate 102. Conducting spacers 107 are located between the first substrate 101 and the second substrate 102.

Fig. 2A is a top plan view of the TFT substrate, and in which the second conducting film 105 is not yet deposited. In Fig. 2A, the region 110 indicated by the broken line corresponds to the opening for the common contact formed in the interlayer dielectric film 18 of the prior art structure. A dielectric 104a is selectively deposited to leave portions of the first conducting film 103 to be exposed.

The first conducting film 103 is exposed at locations where the dielectric 104a is not deposited. The exposed portions of the first conducting film 103 are connected with the overlying second conducting film 105.

On the first substrate 101, the dielectric 104a is closest to the second substrate. As shown in Fig. 1, on the dielectric 104a, conducting spacers 107 electrically connect the second conducting film 105 on the first substrate 101 with the third conducting film 106 on the second substrate 102.

The dielectric 104a is closest to the second substrate 102. Therefore, the conducting spacers 107 electrically

connecting the second conducting film 105 with the third conducting film 106 hold the cell gap G. In consequence, the gap G is dependent only on the size of the conducting spacers 107. Where the spacers 107 are uniform in size, the cell gap G can be rendered uniform among liquid-crystal cells even if the thickness t of the dielectric film 104 differs among cells.

In the present embodiment, the area of each portion not covered with the dielectric 104a is preferably sufficiently wider than the area occupied by one conducting spacer 107 and permits the conducting spacers 107 to move freely, because the spacers 107 existing in the regions where the dielectric 104a is not present do not contribute toward maintaining the gap. Otherwise, plural conducting spacers 107 would be stacked on top of each other, making it impossible to maintain the cell gap G uniform across the cell.

Also in the present embodiment, it is desirable that the area of each portion of the dielectric film 104a be sufficiently larger than the area occupied by one conducting spacer 107 and that the conducting spacers 107 be arranged with certainty. If the spacers 107 are not positioned on the dielectric film 104a with certainty, it will not be possible to make electrical connections between the first and second substrates. Furthermore, the cell spacing will not be maintained.

In this embodiment, the dielectric 104a is deposited as shown in Fig. 2A. The relation between the regions where the dielectric 104a is deposited and each region where the first conducting film 103 is exposed may be reversed as shown in Fig. 2B.

EXAMPLE 1

In this example, the present invention is applied to a common contact portion of a reflection-type liquid crystal display. Fig. 3 is a top plan view of the TFT substrate of this liquid crystal display. Fig. 4 is a top plan view of the counter substrate of the liquid crystal display.

Referring to Fig. 3, the TFT substrate 200 comprises a substrate 201 having a pixel region 202, a scanning line driver circuit 203, and a signal line driver circuit 204. Pixel electrodes and TFTs connected with the pixel electrodes are arranged in rows and columns in the pixel region 202. The scanning line driver circuit 203 controls the timing at which each TFT is turned on and off. The signal line driver circuit 204 supplies image data to the pixel electrodes. Extractor terminals 205 are also provided to supply electric power and control signals from the outside. Common contact portions 206a - 206d form junctions with the counter electrode.

As shown in Fig. 4, the counter substrate 250 comprises a substrate on which a counter electrode 252 consisting of a transparent conducting film is deposited. A central rectangular region 253 is opposite to the pixel region 202 of the TFT substrate 200. Four corner regions 254a - 254d are electrically connected with the contact portions 206a - 206d, respectively, of the TFT substrate 200.

As shown in Fig. 3, conducting pads are formed in the common contact portions 206a - 206d, respectively, of the TFT substrate 200. These conducting pads are electrically connected together by internal conducting lines 207a - 207c. The internal lines 207a and 207b extend to the extractor terminals 205 and are electrically connected with common terminals 205a and 205b, respectively.

A process sequence for manufacturing the pixel region 202 and the common contact portion 206a - 206d on the TFT substrate is next described by referring to Figs. 5A - 5G.

First, the substrate 201 having an insulating surface was prepared. In the present example, a silicon oxide film was formed as a buffer film on the glass substrate. An active layer 302 consisting of a crystalline silicon film was formed over the substrate 201. Although only one TFT is shown, millions of TFTs are built in the pixel region 202 in practice.

In the present example, an amorphous silicon film was thermally crystallized to obtain the crystalline silicon film. This crystalline silicon film was patterned by an ordinary photolithographic step to obtain the active layer 302. In this example, a catalytic element such as nickel for promoting the crystallization was added during the crystallization. This technology is described in detail in Japanese Unexamined Patent Publication No.7-130652.

Then, a silicon oxide film 303 having a thickness of 150 nm was formed. An aluminum film (not shown) containing 0.2% by weight of scandium was deposited on the silicon oxide film 303. The aluminum film was patterned, using a resist mask 304, into an island pattern 305 from which gate electrodes will be formed (Fig. 5A).

The present example made use of the anodization technique described in Japanese Unexamined Patent Publication No. 7-135318. For further information, refer to this publication.

First, the island pattern 305 was anodized within a 3% aqueous solution of oxalic acid while leaving the resist mask 304 on the island pattern 305, the mask 304 having been used for the patterning step. At this time, an electrical

current of 2 to 3 mV was passed, using a platinum electrode as a cathode. The voltage was increased up to 8 V. Since the resist mask 304 was left on the top surface, porous anodic oxide film 306 was formed on the side surfaces of the island pattern 305 (Fig. 5B).

After removing the resist mask 304, anodization was carried out within a solution prepared by neutralizing a 3% aqueous solution of tartaric acid with aqueous ammonia. At this time, the electrical current was set to 5 - 6 mV. The voltage was increased up to 100 V. In this way, a dense anodic oxide film 307 was formed.

The above-described anodic oxidation step defined the unoxidized island pattern 305 into gate electrodes 308. Internal connecting lines 207c interconnecting the common contact portions 206c and 206d were created from the aluminum film described above simultaneously with the gate electrodes 308.

Then, using the gate electrodes 308 and surrounding anodic oxide film 306, 307 as a mask, the silicon oxide film 303 was etched into a gate insulating film 309. This etching step relied on dry etching using CF_4 gas (Fig. 5C).

After the formation of the gate insulating film 309, the porous anodic oxide film 307 was removed by wet etching using Al mixed acid.

Thereafter, impurity ions for imparting one conductivity type were implanted by ion implantation or plasma doping. Where N-type TFTs are placed in the pixel region, P (phosphorus) ions may be implanted. Where P-type TFTs are placed, B (boron) ions may be implanted.

In the present example, the above-described process for implanting the impurity ions was carried out twice by ion implantation. The first step was performed under a high

accelerating voltage of 80 keV. The system was so adjusted that the peak of the impurity ions was brought under the ends (protruding portions) of the gate insulating film 309. The second step was effected under a low accelerating voltage of 5 keV. The accelerating voltage was adjusted so that the impurity ions were not implanted under the ends (protruding portions) of the gate insulating film 309.

In this way, a source region 310, a drain region 311, lightly doped regions 312, 313, and a channel region 314 for the TFT were formed. The lightly doped region 313 on the side of the drain region 311 is also referred to as the LDD region (Fig. 5D).

At this time, it is preferable to implant the impurity ions to such a dosage that the source and drain regions 310 and 311, respectively, exhibit a sheet resistance of 300 to 500 Ω/□. In addition, it is necessary to optimize the lightly doped regions 312 and 313 according to the performance of the TFT. After the impurity ion implantation step, a thermal treatment was carried out to activate the impurity ions.

Then, a 1 μm-thick-silicon oxide film was formed as a first interlayer dielectric film 315. The thickness of the interlayer dielectric film 315 was set to 1 μm to flatten the surface of the first interlayer dielectric film 315 as much as possible. This could mitigate the protrusions due to the gate electrodes 308.

The first interlayer dielectric film 315 may be made of silicon nitride or silicon oxynitride, as well as silicon oxide. Alternatively, the first interlayer dielectric film 315 may be a multilayer film of these materials.

Contact holes for gaining access to the source and drain regions 310 and 311, respectively, were created in the

first interlayer dielectric film 315. Contact holes for allowing access to the internal conducting lines 207c were formed in the common contact portions 206c and 206d. Then, a conducting film forming a precursor for source and drain electrodes 316 and 317, respectively, and for internal conducting lines 318 was deposited.

In this example, the conducting film was created from a multilayer film of titanium (Ti), aluminum (Al), and titanium (Ti) by sputtering. Each of the titanium layers was 100 nm thick, while the aluminum layer was 300 nm thick. This multilayer film was patterned to form a source electrode 316, a drain electrode 317, and internal conducting lines 318 (Fig. 5E).

The internal conducting lines 318 shown Fig. 5E correspond to the internal conducting lines 207a and 207b shown in Fig. 3. These conducting lines 207a and 207b were connected with internal conducting lines 207c at the common contact portions 206c and 206d. The internal conducting lines 207c and the gate electrode 308 were created by the same processing steps.

Subsequently, an organic resinous film was formed as a second interlayer dielectric film 319 to a thickness of 1 to 2 μm. Polyimide, polyamide, polyimidamide, acrylic resin, or other material may be used as the material of the organic resinous film. The organic resinous material acts to planarize the surface of the second interlayer dielectric film 319. This is important to make the cell gap uniform. In the present example, polyimide was deposited as the second interlayer dielectric film 319 to a thickness of 1 μm.

Then, contact holes 320 and 321 were formed in the second interlayer dielectric film 319 to have access to the

drain electrode 317 and to the internal conducting lines 318, respectively. The contact holes 321 for the internal conducting lines 318 were formed in the openings 111 shown in Fig. 2A. That is, rectangular holes measuring 100 μm x 100 μm were arranged in 5 rows and 5 columns within the rectangular region 110 measuring 1.1 mm x 1.1 mm. These holes were spaced 100 μm from each other. Moreover, contact holes for connecting the internal conducting lines 318 (207a and 207b) with the common terminals 205a and 205b at the extractor terminals 205 were formed.

As described later, the size of each hole was set to 100 μm x 100 μm to set the diameter of the conducting spacers to 3.5 μm in this example. This provides sufficient space so that the conductive spacer located at this position can move. Hence, the conducting spacers are prevented from being stacked on top of each other.

The area of the left portions of the interlayer dielectric film 319 in the common contact portions is large enough to permit the conducting spacers to move. This assures that the conducting spacers are arranged in these regions. Consequently, the conducting spacers positioned in these regions can maintain the cell gap and make electrical connections reliably.

A thin metal film which would later be made into pixel electrodes 322 and a conducting pad 323 were formed to a thickness of 100 to 400 nm. In the present example, the thin metal film was made of an aluminum film containing 1 wt % titanium and deposited to a thickness of 300 nm by sputtering. Then, the thin metal film was patterned to form the pixel electrodes 322 and the conducting pad 323. This pad 323 measured 1.1 mm x 1.1 mm, was rectangular, and covered the contact holes 321. The extractor terminals 205

were also patterned. Thus, the TFT substrate was completed (Fig. 5G).

Referring to Fig. 6, the counter substrate 250 comprised a transparent plate 251 on which the counter electrode 252 was formed from an ITO film. A glass or quartz substrate can be used as the substrate 251.

Then, the TFT substrate 200 and the counter substrate 250 were bonded together. This bonding step may be a well-known cell assembly method.

First, a sealing material was applied to one of the TFT substrate 200 and the counter substrate 250. In this example, the sealing material was applied to the counter substrate 250. A UV-curable and thermosetting resin was used as the sealing material. This sealing material was applied around the substrate along straight lines except for the liquid crystal injection port by a sealant dispenser. A sealing material to which 3.0 wt % spherical conducting spacers 401 were added was applied to regions 254a - 254d shown in Fig. 4. The sealing material to which the conducting spacers were added functioned as an anisotropic conducting film.

Generally, the conducting spacers 401 consist of resinous spheres coated with a conducting film. In the present example, the conducting spacers 401 were coated with gold (Au). The diameter of the conducting spacers 401 may be larger than the cell gap by about 0.2 to 1 μm. In this example, the conducting spacers 401 had a diameter of 3.5 μm to set the cell gap to 3 μm. After applying the sealing material, it was temporarily baked.

Thereafter, spacers 402 were dispersed onto one of the TFT substrate 200 and the counter substrate 250 to maintain the cell gap. In this example, the spacers 402 were applied

to the counter substrate 250. To set the cell gap to 3 μm, spherical spacers of a polymeric material were used as the spacers 402.

Then, the TFT substrate 200 and the counter substrate 250 were held opposite to each other, and they were pressed against each other until the cell gap in the pixel region was decreased to the diameter of the spacers 402. Under the pressed state, UV light was directed at this assembly for more than 10 seconds to cure the sealing material. The cell gap was fixed. Then, the assembly was heated under pressure, thus enhancing the adhesive strength.

Subsequently, a liquid crystal material was injected, and the entrance hole was sealed off, thus completing the cell assembly process. As shown in Fig. 6, the counter electrode 252 on the counter substrate 250 was electrically connected with the conducting pad 323 on the TFT substrate 200 by the conducting spacer 401. On the TFT substrate, the conducting pad 323 connected the internal conducting lines 318 with the common terminals. This connection structure permitted the counter electrode 252 on the counter substrate 250 to be connected with an external power supply via the conducting lines on the TFT substrate. Fig. 1 is an enlarged view of the common contact portion of Fig. 6.

In the present example, to set the cell gap to 3 μm, the spacers 402 applied to the pixel region had a diameter of 3 μm. The diameter of the conducting spacers 401 was 3.5 μm. Setting the diameter of the conducting spacers greater than the diameter of the spacers 402 (i.e., the cell gap) made reliable the connection between the counter electrode 252 and the conducting pad 318. When the two plates were being clamped together to bond them together, the conducting spacers 401 were crushed because they were larger in

diameter than the cell gap. This increased the areas of the portions in contact with the counter electrode 252 and with the conducting pad 318, respectively. Hence, the electrical connection was rendered more reliable. Furthermore, the cell gap could be maintained at the same dimension as in the pixel region.

In this example, the internal conducting lines 318 were made of the precursor for the source and drain electrodes 316 and 317, respectively. It is only necessary for the internal conducting lines 318 to be under the pixel electrodes 322. For instance, where a black matrix consisting of a conducting film of titanium or the like is formed inside the second interlayer dielectric film 315, the internal conducting lines 318 can be formed from this conducting film.

In the present example, it is important to flatten the surface of the second interlayer dielectric film 319 on which the pixel electrodes 322 are formed in order to make uniform the cell gap. Also, the flatness of the surface of the first interlayer dielectric film 315 where the internal conducting lines 318 are formed is important.

Methods of obtaining an interlayer dielectric film having a flat surface include a method of increasing the thickness of the interlayer dielectric film, a leveling method using an organic resinous film, a mechanical polishing method, and etch-back techniques. The present example made use of the method of increasing the film thickness to planarize the first interlayer dielectric film 315. Also, the method of relying on leveling using an organic resinous film was used to flatten the first interlayer dielectric film 315. Other methods may also be employed for the same purpose.

In a liquid crystal display in accordance with the present example, a dichroic dye may be dispersed in the liquid crystal layer. Orientation films may be deposited on the TFT substrate and on the counter substrate. Color filters may be formed on the counter substrate. The practitioner may appropriately determine the kind of the liquid crystal layer, the presence or absence of the orientation films and the color filters according to the driving method, the kind of the liquid crystal, and other factors.

For instance, where the color filters are mounted on the counter substrate 250, the color filters are not formed at the common contact portions and so steps are formed between the pixel region and the common contact portions on the counter substrate. To compensate for these steps, it is necessary to make the diameter of the conducting spacers larger by an amount almost equal to the thickness of the color filter.

In the present example, the liquid crystal display is of the reflection type. A transmissive liquid crystal display may also be fabricated. In this case, the precursor for the pixel electrode and for the conducting pad may be made of a transparent ITO film or the like.

In the example described above, the transistor is a coplanar TFT that is a typical top-gate TFT. It may also be a bottom-gate TFT. In addition, thin-film diodes, metal-insulator-metal (MIM) devices, metal-oxide varistors, and other devices can be used, as well as the TFTs.

EXAMPLE 2

The present example is a modification of the common contact portions of Example 1. Fig. 7 is a fragmentary

cross-sectional view of an active-matrix display in accordance with the present example. The configuration of a TFT substrate shown in Fig. 7 is the same as the configuration shown in Fig. 6, and some reference numerals are omitted. Like components are indicated by like reference numerals in both Figs. 6 and 7. Fig. 9 is an enlarged view of the common contact portion shown in Fig. 7.

In Example 1 shown in Fig. 6, the counter electrode 252 consists of an ITO film that is a transparent conducting film. Therefore, the counter electrode 252 and the conducting spacers 401 are larger in electrical resistance than metal films. The present example is intended to reduce this electrical resistance.

Accordingly, the resistance value between the counter electrode 252 and the conducting spacers 401 can be lowered by forming a metallization layer on the counter substrate 250 and patterning the metallization layer into conducting pads, or conducting film, 501 at the common contact portions 254a - 254d. Importantly, the conducting film forming the conducting pads 501 is lower in electrical resistance than the conducting film forming the counter electrode 252.

Where the black matrix on the counter substrate is formed from a conducting film as consisting of chromium, the connecting pads 501 can be formed from this conducting film. When the conducting film is patterned to form the black matrix, the connecting pad 501 may be created.

EXAMPLE 3

The present example is a modification of Example 2. Fig. 8 is a fragmentary cross-sectional view of an active-matrix display in accordance with the present example. The TFT substrate shown in Fig. 8 is identical in structure with

that shown in Fig. 6, and some reference numerals are omitted in Fig. 8. It is noted like components are denoted by like reference numerals in both Figs. 6 and 8. Fig. 10 is an enlarged view of the common contact portion of Fig. 8.

In Example 1, both counter substrate 251 and counter electrode 252 are transparent to light and so the distribution of the conducting spacers 401 on the common contact portions can be visually observed from the side of the counter substrate 250 after both substrates have been bonded together. In Example 2, however, the connecting pad 501 consisting of metallization layer is formed and, therefore, the distribution of the conducting spacers 401 cannot be visually checked.

The present example is intended to permit one to visually observe the distribution of the conducting spacers 401 while a connecting pad is provided to lower the resistance value. For this purpose, the connecting pad, 601, is provided with openings formed at selected locations. One can observe the conducting spacers 401 through these openings.

Fig. 11 is a top plan view of the contact portions according to the present example, taken from the side of the counter substrate. Fig. 10 is a cross-sectional view of the common contact portion in a region 600 surrounded by the broken line. As shown in Fig. 11, the conducting pad 601 is formed with openings 602. In each opening 602, there exist only the counter substrate 251 and the counter electrode 252, both of which have transparency. Hence, the distribution of the conducting spacers 401 can be observed through the openings 602.

To maintain the cell gap, the openings 602 should be formed opposite to the contact holes 321 formed in the

second interlayer dielectric film of the TFT substrate. At these locations, the conducting spacers 401 are not in contact with the counter electrode. The area of each opening 602 should be slightly larger than the area of each contact holes 321 formed in the second interlayer dielectric film, i.e., about several to thirty percent greater. The number of the openings 602, their arrangement, and their shape are not limited to the example of Fig. 11. Rather, one can arbitrarily set these geometrical factors.

Setting each opening 602 in the connecting pad 601 slightly larger than each contact holes 321 makes it possible to visually check the conducting pad 602 on the second interlayer dielectric film 319, which contributes to electrical connection.

In Examples 2 and 3, the cell gap in the common contact portions is made uniform. At the same time, the contact resistances of the conducting spacers 401 and of the counter electrode 252 are decreased. If the main purpose is to lower these resistance values, the common contact portions on the TFT substrate may have the prior art structure as shown in Fig. 13. In this case, any of the connecting pads 501 and 601 described in Examples 2 and 3, respectively, may be formed between the substrate 23 and the counter electrode 24 at the common contact portions 16 shown in Fig. 13.

In Examples 1 - 3 described above, the present invention is applied to active-matrix liquid crystal displays. The contact structure in accordance with the present invention is applicable to any apparatus having a contact structure for electrically connecting conductors formed on one substrate with conducting conductors formed on the other opposite substrate via conducting spacers. For example, the novel contact structure can connect ICs built

on different silicon wafers.

The common contact structure in accordance with the present invention can eliminate variations of the cell gap among liquid-crystal cells even if the film thickness varies among interlayer dielectric films. Also, poor contacts due to conducting spacers can be reduced.

In particular, in accordance with the present invention, the cell gap depends only on the size of conducting spacers. Therefore, where the conducting spacers are uniform in size, the cell gap between opposite substrates or plates can be made uniform among different liquid-crystal cells, if the thickness of a dielectric film electrically insulating the first and second conducting films is different among different liquid-crystal cells.

IN THE CLAIMS:

1. An active matrix display device comprising:

a first substrate:

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having at least two openings;

a second conductive film provide on said second interlayer insulating film and in said openings;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film ins aid openings;

wherein at least one of said conductive spacers is held over said second interlayer insulating film and in contact with both said second conductive film and said third conductive film.

2. An active matrix display device according to claim 1, wherein each of said conductive spacers is a sphere coated with gold.

3. An active matrix display device according to claim 1, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

4. An active matrix display device according to claim 1, wherein siad active matrix display device further comprises a fourth conductive film between said third conductive film and second conductive film.

5. An active matrix display device according to claim 1, wherein said active matrix display device is a liquid crystal display device.

6. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having at least two openings;

a second conductive film provided on said second interlayer insulating film and in said openings;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said openings,

wherein said conductive spacers are dispersed into a sealing material,

wherein at least one of said conductive spacers is held over said second interlayer insulating film and in contact with both said second conductive film and said third conductive film.

7. An active matrix display device according to claim 6, wherein each of said conductive spacers is a sphere coated with gold.

8. An active matrix display device according to claim 6, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

9. An active matrix display device according to claim 6, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

10. An active matrix display device according to claim 6, wherein said active matrix display device is a liquid crystal display device.

11. An active matrix display device comrpising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having at least two openings;

a second conductive film provided on said second interlayer insulating film and in said openings;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said openings;

wherein at least one of said conductive spacers is held over said second interlayer insulating film and in contact with both said second conductive film and said third conductive film,

wherein each of said openings occupies an area larger than an area occupied by each of said conductive spacers

12. An active matrix display device according to claim 11, wherein each of said conductive spacers is a sphere coated with gold.

13. An active matrix display device according to claim 11, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

14. An active matrix display device according to claim 11, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

15. An active matrix display device according to claim 11, wherein said active matrix display device is a liquid crystal display device.

16. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate:

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having an opening with a part of said second interlayer insulating film remaining in said opening;

a second conductive film provided on said second interlayer insulating film and in said opening;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said opening,

wherein at least one of said conductive spacers is held over said part of said second interlayer insulating film and in contact with both said second conductive film and conductive film.

17. An active matrix display device according to claim 16, wherein each of said conductive spacers is a sphere coated with gold.

18. An active matrix display device according to claim 16, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

19. An active matrix display device according to claim 16, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

20. An active matrix display device according to claim 16, wherein said active matrix display device is a liquid crystal display device.

21. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said conductive film, said second interlayer insulating film having an opening with a part of said second interlayer insulating film remaining in said opening;

a second conductive film provided on said second interlayer insulating film and in said opening;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said opening,

wherein said conductive spacers are dispersed into a sealing material,

wherein at least one of said conductive spacers is held over said part of said second interlayer insulating film and in contact with both said second conductive film and said third conductive film.

22. An active matrix display device according to claim 21, wherein each of said conductive spaces is a sphere coated with gold.

23. An active matrix display device according to claim 21, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

24. An active matrix display device according to claim 21, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

25. An active matrix display device according to claim 21, wherein said active matrix display is a liquid crystal display device.

26. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having an opening with a part of said second interlayer insulating film remaining in said opening;

a second conductive film provided on said second interlayer insulating film and in said opening.

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between siad first substrate and said second susbtrate;

wherein said first conductive film is connected with said second conductive film in said opening,

wherein at least one of said conductive spacers is held over said part of said second interlayer insulating film and in conatact with both said second conductive film and said third conductive film,

wherein said opening occupies an area larger than an area occupied by each of said conductive spacers.

27. An active matrix display device according to claim 26, wherein each of said conductive spacers is a sphere coated with gold.

28. An active matrix display device according to claim 26, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

29. An active matrix display device according to claim 26, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

30. An active matrix display device according to claim 26, wherein said active matrix display device is a liquid crystal display device.

ABSTRACT OF THE DISCLOSURE

There is disclosed a contact structure for electrically connecting conducting lines formed on a first substrate of an electrooptical device such as a liquid crystal display with conducting lines formed on a second substrate via conducting spacers while assuring a uniform cell gap among different cells if the interlayer dielectric film thickness is nonuniform across the cell or among different cells. A first conducting film and a dielectric film are deposited on the first substrate. Openings are formed in the dielectric film. A second conducting film covers the dielectric film left and the openings. The conducting spacers electrically connect the second conducting film over the first substrate with a third conducting film on the second substrate. The cell gap depends only on the size of the spacers, which maintain the cell gap.

FIG.1

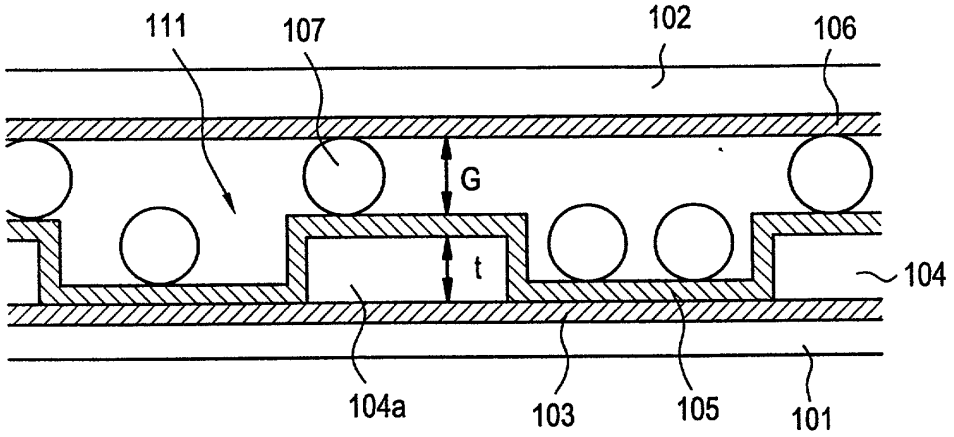


FIG.2A

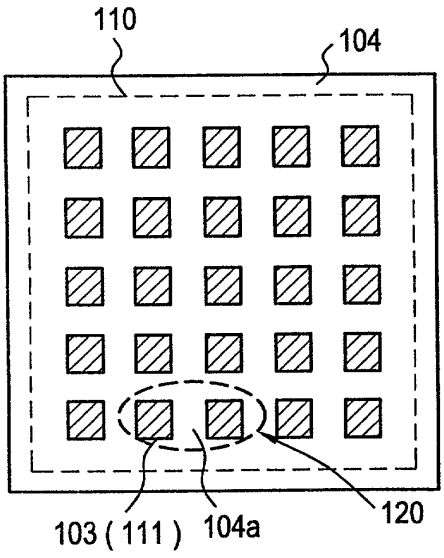


FIG.2B

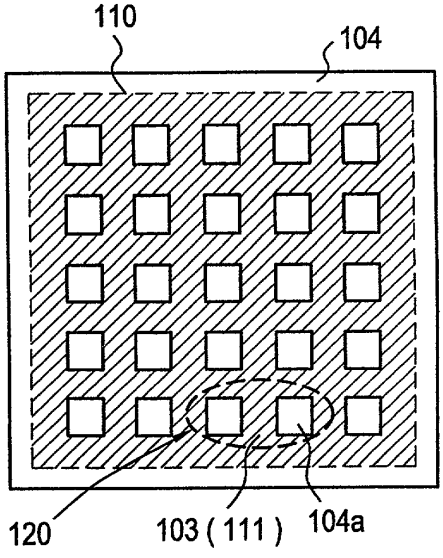


FIG.3

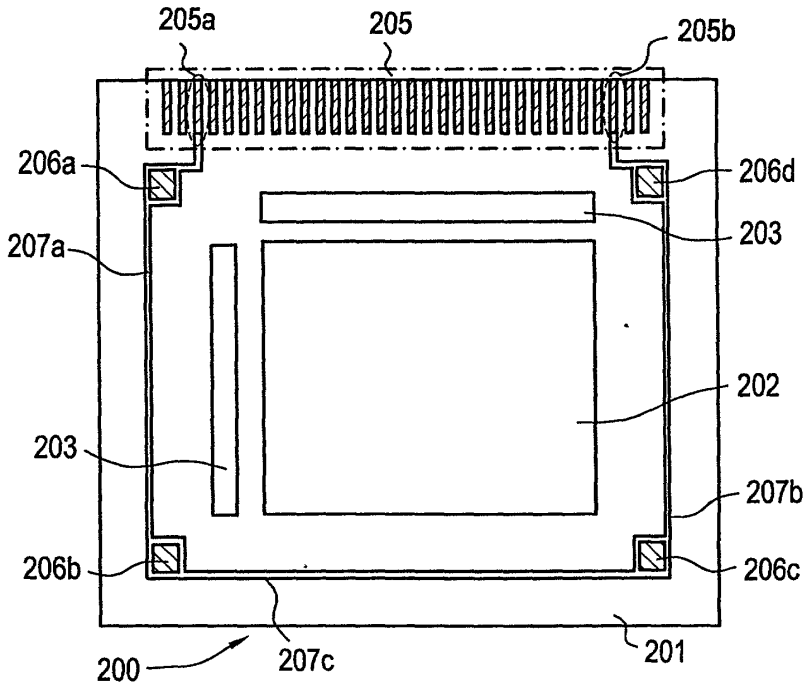
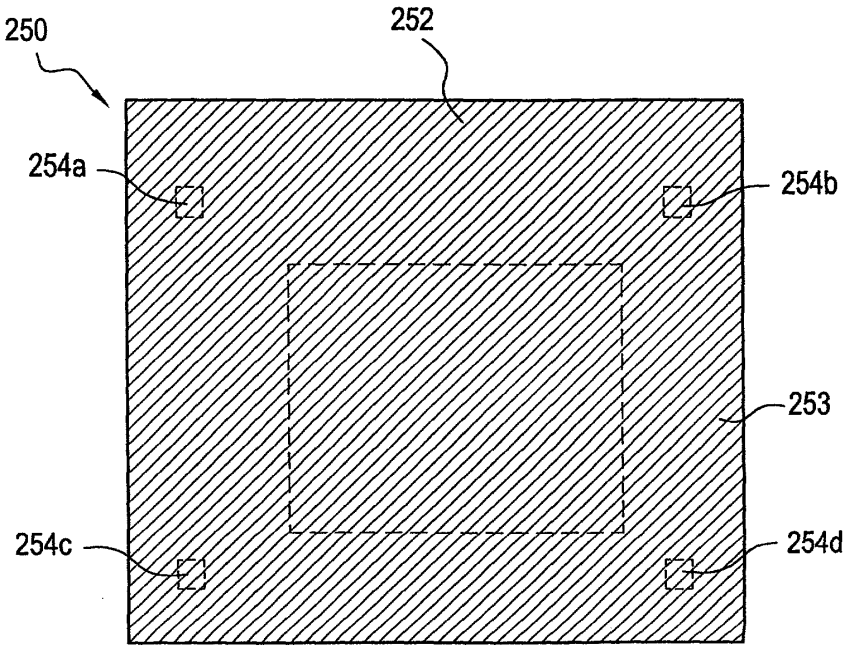

205a
205
205b
206a
206d
207a
203
202
203
207b
206b
206c
200
207c
201

FIG.4


250
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254c
254d

FIG.5A

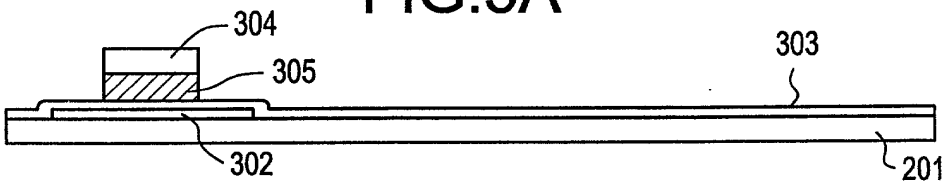


FIG.5B

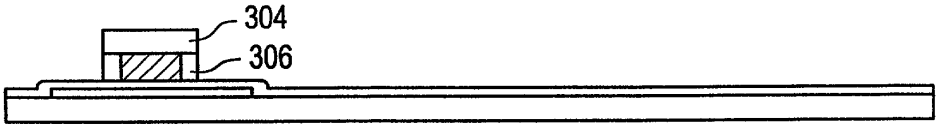


FIG.5C

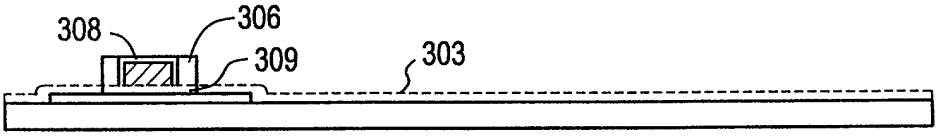


FIG.5D

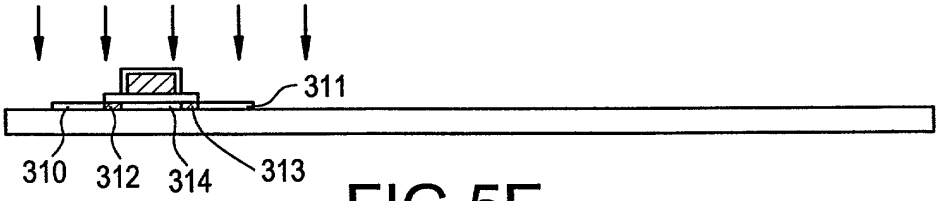


FIG.5E

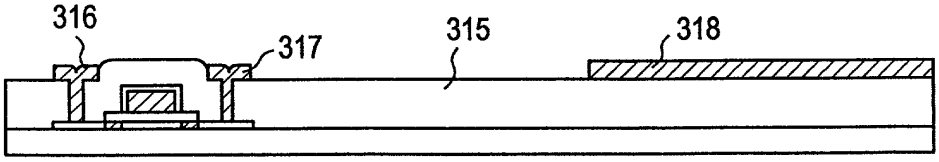


FIG.5F

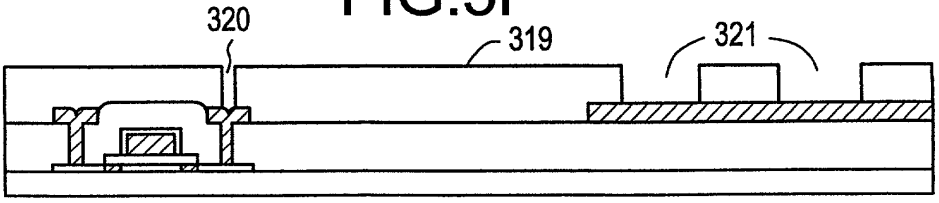


FIG.5G

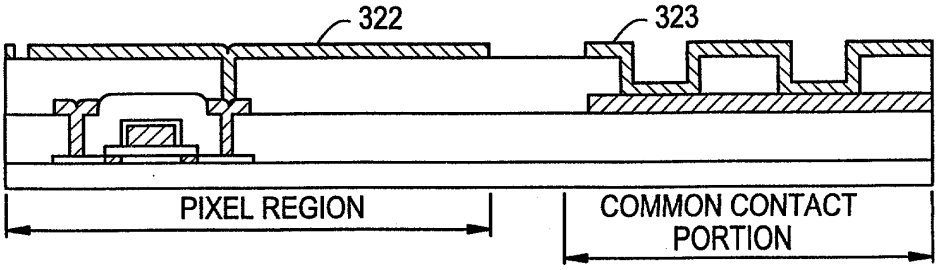


FIG.6

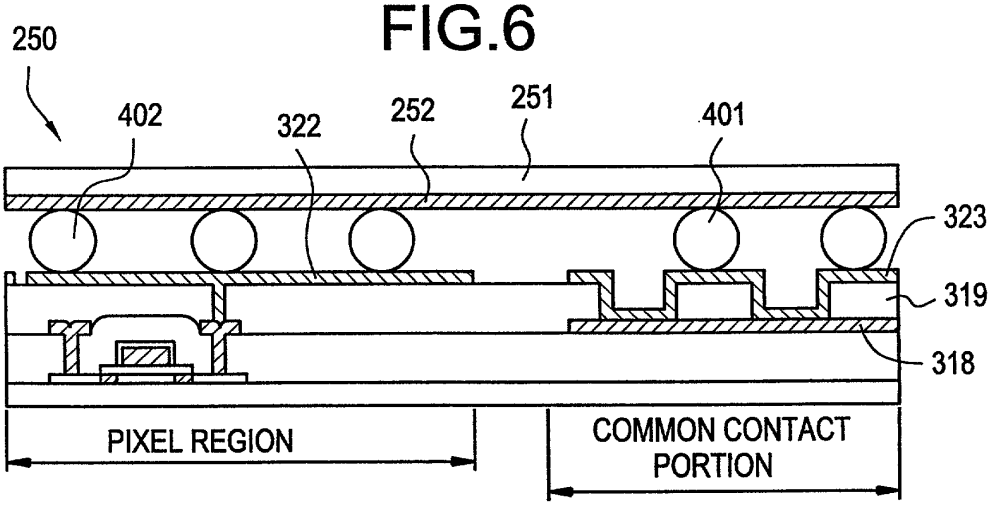


FIG.7

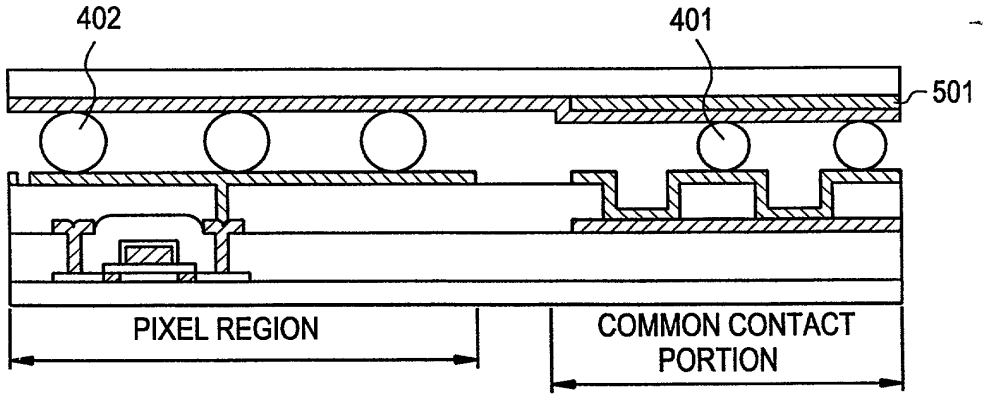


FIG.8

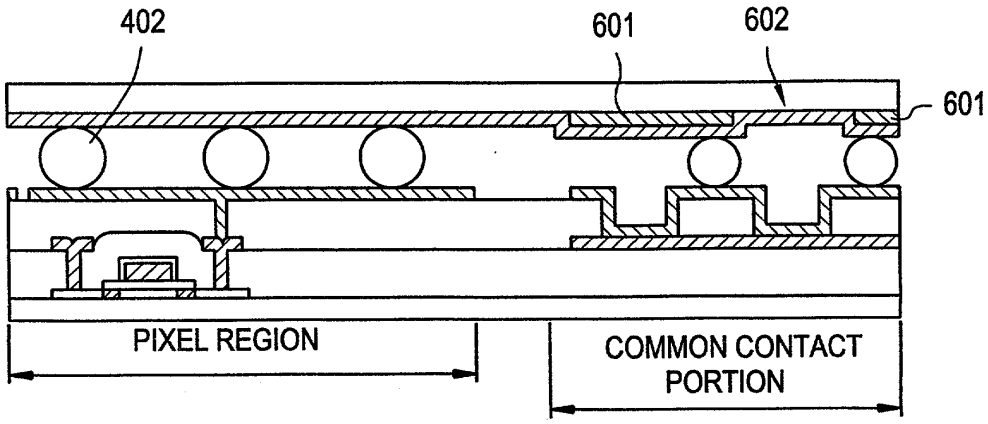


FIG.9

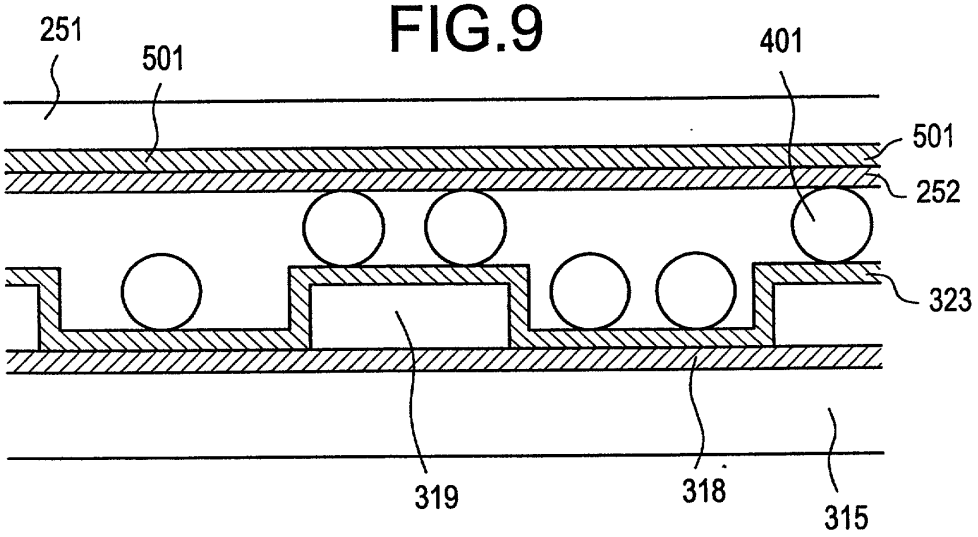


FIG.10

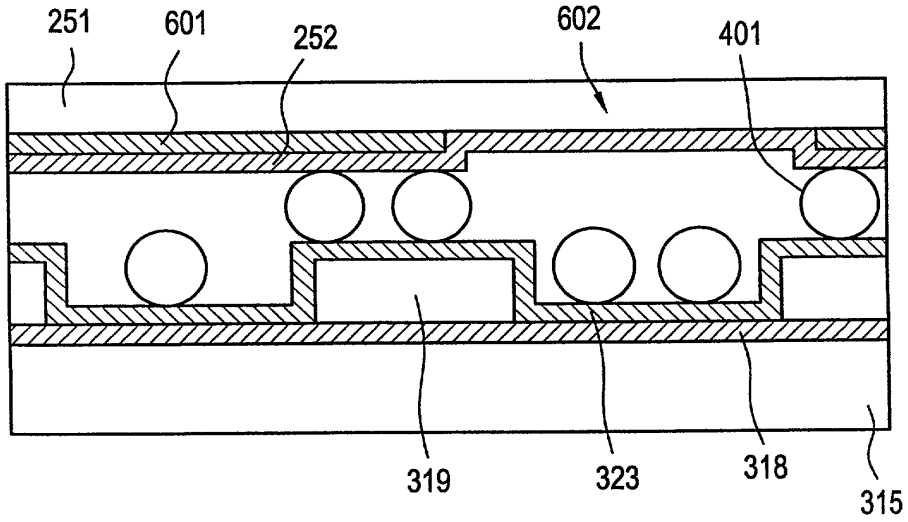


FIG.11

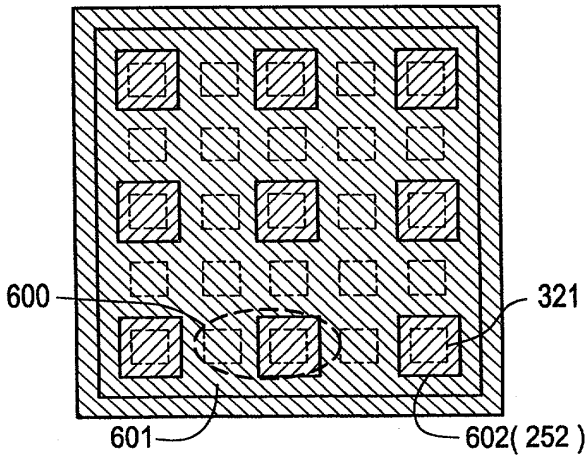


FIG.12
PRIOR ART

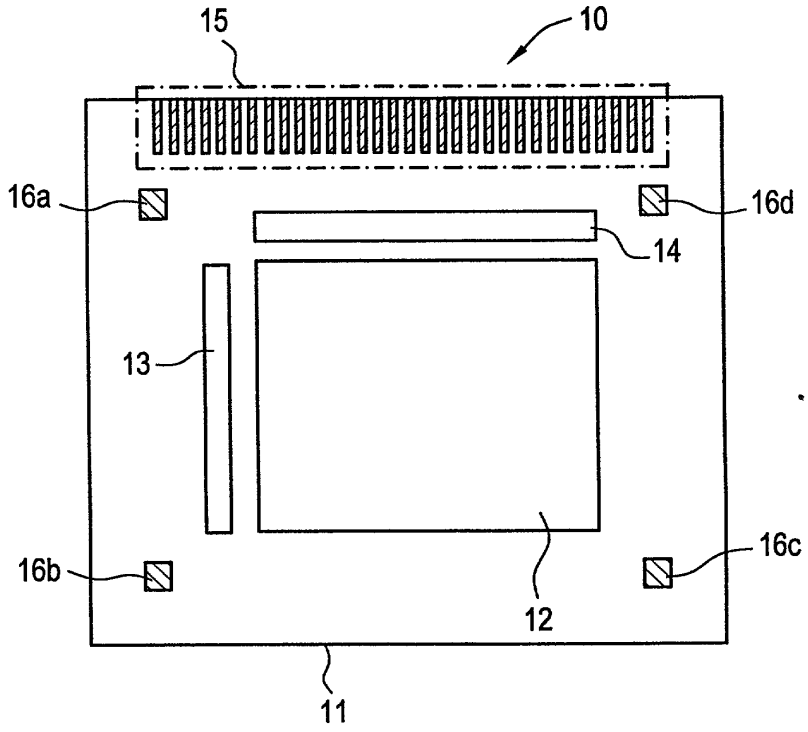


FIG.13
PRIOR ART

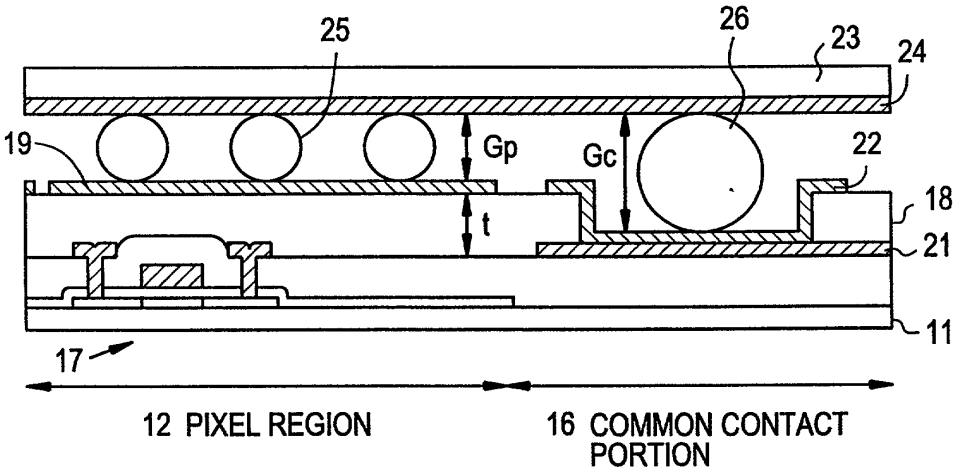
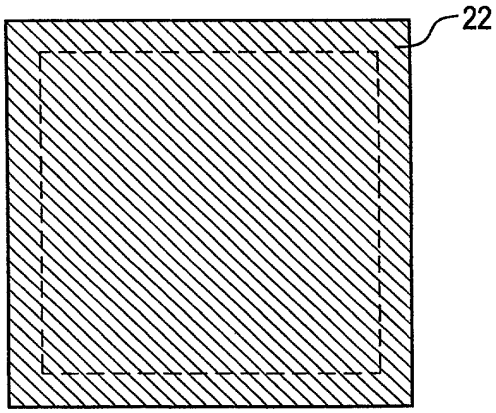


FIG.14
PRIOR ART



PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CONTACT STRUCTURE

上記発明の明細書（下記の箇でxⅡがついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____に訂正されました。

☒ was filed on March 24, 1998
as United States Application Number or
PCT International Application Number
09/046,685 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
9-094606	Japan	March 27, 1997	☐
			☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の表明を行なえば、出願した、又は発行された特許の有効性が失われることを認識し、よってここに下記のごとく宣言を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
日本語宣言書

委任状：　私は下記の発明者として、本件に関する一切の手続きを特許商標庁に対して遂行する弁護士および/または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Daniel W. Sixbey, Reg. No. 20,992) Stuart A. Fraser, Reg. No. 24,213) Charles M. Leedom, Jr. Reg. No. 25,477
Gerald J. Ferguson, Jr. (Reg. No. 23,016) David S. Safran (Reg. No. 27,997) Thomas W. Cole (Reg. No. 28,290)
Joan K. Lawrence (Reg. No. 29,940) Donald R. Studebaker (Reg. No. 32,815) Jeffrey L. Costellia (Reg. No. 35,483)
Evan R. Smith (Reg. No. 35,683) Tim L. Brackett (Reg. No. 36,092) Eric J. Robinson (Reg. No. 38,285)

書類送付先

Send Correspondence to:

SIDLEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102

SIDLEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)

Gerald J. Ferguson, Jr.
(703) 790-9110

Gerald J. Ferguson, Jr.
(703) 790-9110

唯一または第一発明者		Full name of sole or first inventor	
		Yoshiharu HIRAKATA	
発明者の署名	日付	Inventor's signature	Date
		Yoshiharu Hirakata	June 1, 1998
住所		Residence	
		Kanagawa, Japan	
国籍		Citizenship	
		Japanese	
私書箱		Post Office Address	
		c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD.	
		398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan	
第二共同発明者		Full name of second joint inventor, if any	
		Shunpei YAMAZAKI	
発明者の署名	日付	Inventor's signature	Date
		Shunpei Yamazaki	June 2, 1998
住所		Residence	
		Tokyo, Japan	
国籍		Citizenship	
		Japanese	
私書箱		Post Office Address	
		c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD.	
		398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan	

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

☐ Please see attached page 3a for names, addresses and signatures of additional inventors, if any.

Docket No.: 0756-2237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the **Divisional** Application of	)	
Yoshiharu HIRAKATA et al	)	Art Group: 2871
Based on Serial No.: 09/361,218	)	Examiner: D. Nguyen
Which was filed: July 27, 1999	)	
For: CONTACT STRUCTURE	)	

NOTICE OF CHANGE OF ADDRESS
and
NOTICE OF CHANGE OF NAME

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Effective immediately, please note that the address and the firm name of the attorney of record in the above-referenced application has been changed. Please direct all future correspondence to:

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Telephone (703) 790-9110
Facsimile (703) 883-0370

Respectfully submitted,

Eric J. Robinson
Registration No.: 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102

EJR/sas

JC-4/9/6

JC662 U.S. PTO 09/734177 12/12/00

Class	Subclass
349	155

ISSUE CLASSIFICATION

PATENT NUMBER 6404480

6404480

U.S. **UTILITY** Patent Application

O.I.P.E.	PATENT DATE
SCANNED M.H Q.A. dft	JUN 11 2002

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/734177	D F	349	155	2871	Nguyen, D

APPLICANTS: Yoshiharu Hirakata
Shunpei Yamazaki

TITLE: Contact structure

Certificate of Correction APR 05 2005

Certificate of Correction SEP 14 2004

PTO-2040 12/99

ISSUING CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)
349	155	349	138

INTERNATIONAL CLASSIFICATION

6	0	2	F	1/1333
6	0	2	F	1/1339

☐ Continued on Issue Slip Inside File Jacket

5/14/02 Formal Drawings (2 sht) set 1 12/12/00

☒ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	7	21	9	30	1

☐ The term of this patent subsequent to _____ (date) has been disclaimed.

☒ The term of this patent shall not extend beyond the expiration date of U.S Patent No. 5,583,371 4,177,474

☐ The terminal ____ months of this patent have been disclaimed.

DUNG NGUYEN (Assistant Examiner) 12/06/01 (Date)

William L. Sikes
Supervisory Patent Examiner
Technology Center 2800
(Primary Examiner) (Date)

Richards (Legal Instruments Examiner) 12/18/01 (Date)

NOTICE OF ALLOWANCE MAILED: 12-13-01

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SEARCHED

Class	Sub.	Date	Exmr.
349	42	7/24	DN
|	155	|	|
	138		
349	42	6/28	DN
|	155	|	|
	138		
349	update search	12/06	DN

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
349	all above	12/06	DN

SEARCH NOTES
(INCLUDING SEARCH STRATEGY)

	Date	Exmr.

(RIGHT OUTSIDE)

ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ART NO.	DATE
FEE DETERMINATION			
O.I.P.E. CLASSIFIER			
FORMALITY REVIEW	HB	JE-916	01-12-01
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

✔	Rejected	N	Non-elected
=	Allowed	I	Interference
—	(Through numeral)... Canceled	A	Appeal
÷	Restricted	O	Objected

Claim Final	Claim Original	Date		
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If more than 150 claims or 10 actions staple additional sheet here

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	0756-2237
First Inventor	Yoshiharu HIRAKATA et al.
Title	CONTACT STRUCTURE
Express Mail Label No.	

APPLICATION ELEMENTS

See *MPEP chapter 600 concerning utility patent application contents.*

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☒ Specification [Total Pages 36]
   (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. ☒ Drawing(s) *(35 U.S.C. 113)* **Figs. 1-14** *[Total Sheets 13]*
5. Oath or Declaration *[Total Sheets 3]*
   a. ☐ Newly executed (original or copy)
   b. ☒ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. ☐ Application Data Sheet. See 37 CFR 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies; or
      ii. ☐ paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney *(when there is an assignee)*
11. ☐ English Translation Document *(if applicable)*
12. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☒ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☒ Other: Notice of Change of Name and Notice of Change of Address

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 09/361,218 filed July 27, 1999 which itself is a Divisional of Serial No. 09/046,685, filed March 24, 1998 now U.S. Patent 5,982,471.

Prior application information: Examiner D. Nguyen Group / Art Unit: 2871

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* 22204 *(Insert Customer No. or Attach bar code label here)* or ☐ *Correspondence address below*

Name	Eric J. Robinson				
	NIXON PEABODY LLP				
Address	8180 Greensboro Drive, Suite 800				
City	McLean	State	VA	Zip Code	22102
Country	United States	Telephone	(703) 790-9110	Fax	(703) 883-0370

Name (Print/Type)	Eric J. Robinson	Registration No. (Attorney/Agent)	38,285
Signature		Date	12/12/00

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FEE TRANSMITTAL FOR FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 1400.00

Co. if Known

Application Number	Not Yet Assigned
Filing Date	December 12, 2000
First Named Inventor	Yoshiharu HIRAKATA et al
Examiner Name	D. Nguyen
Group Art Unit	2871
Attorney Docket No.	0756-2237

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 19-2380

Deposit Account Name: NIXON PEABODY LLP, 8180 Greensboro Drive Suite 800, Mclean, Va. 22102

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☒ **Payment Enclosed:**

☒ Check ☐ Credit Card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Divisional Fling fee	$710.00
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2, EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	30	-20**=	10	X	18.00	=	$180.00
Independent Claims	6	-3** =	3	X	80.00	=	$240.00
Multiple Dependent					270.00	=	$270.00

Large Entity Fee Code	Large Entity Fee	Small Entity Fee Code	Small Entity Fee ($)	Fee Description ($)
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) $690.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge – late filing fee or oath	
127	50	227	25	Surcharge – late provisional filing fee or cover sheet	
139	130	139	130	Non-English transaction	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,240	241	620	Petition to revive – unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.29(b))	
179	710	249	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	Eric J. Robinson	Registration No. *(Attorney/Agent)*	38,285	Telephone	(703) 790-9110
Signature				Date	12/12/00

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Docket No.: 0756-2237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the **Divisional** Application of	)	
Yoshiharu HIRAKATA et al	)	Art Group: 2871
Based on Serial No.: 09/361,218	)	Examiner: D. Nguyen
Which was filed: July 27, 1999	)	
For: CONTACT STRUCTURE	)	

NOTICE OF CHANGE OF ADDRESS
and
NOTICE OF CHANGE OF NAME

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Effective immediately, please note that the address and the firm name of the attorney of record in the above-referenced application has been changed. Please direct all future correspondence to:

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Telephone (703) 790-9110
Facsimile (703) 883-0370

Respectfully submitted,

Eric J. Robinson
Registration No.: 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102

EJR/sas

FIG.1

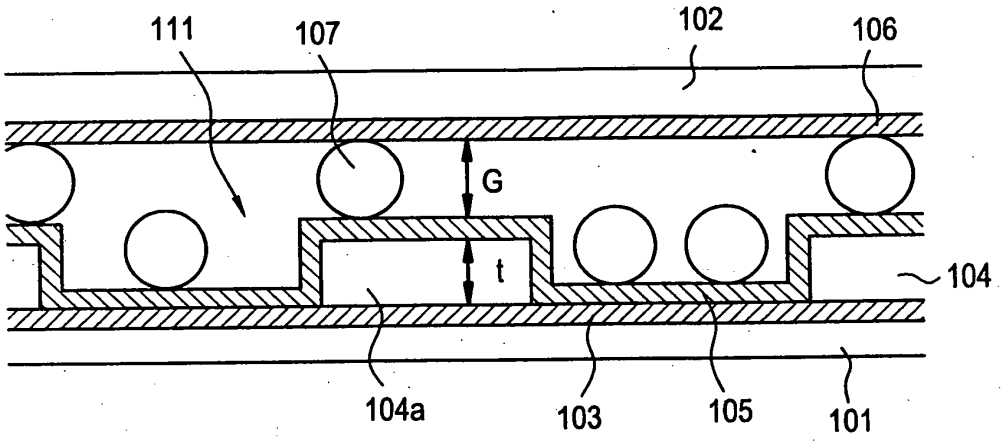


FIG.2A

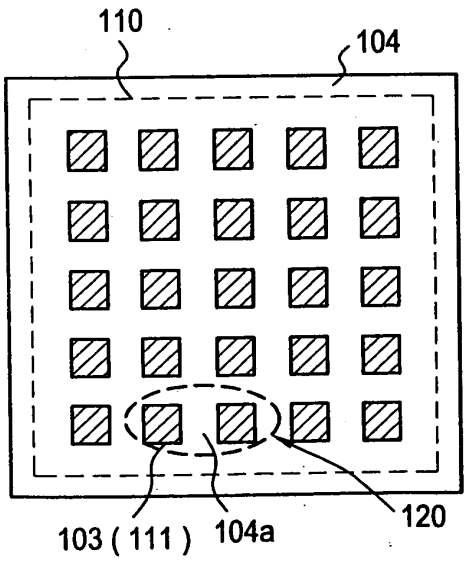
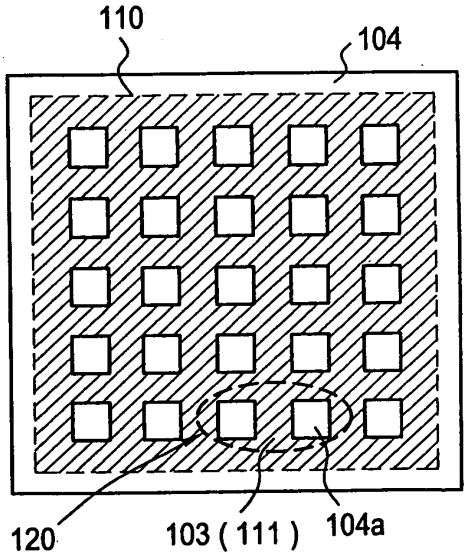


FIG.2B



2 Sheets.

FIG.3

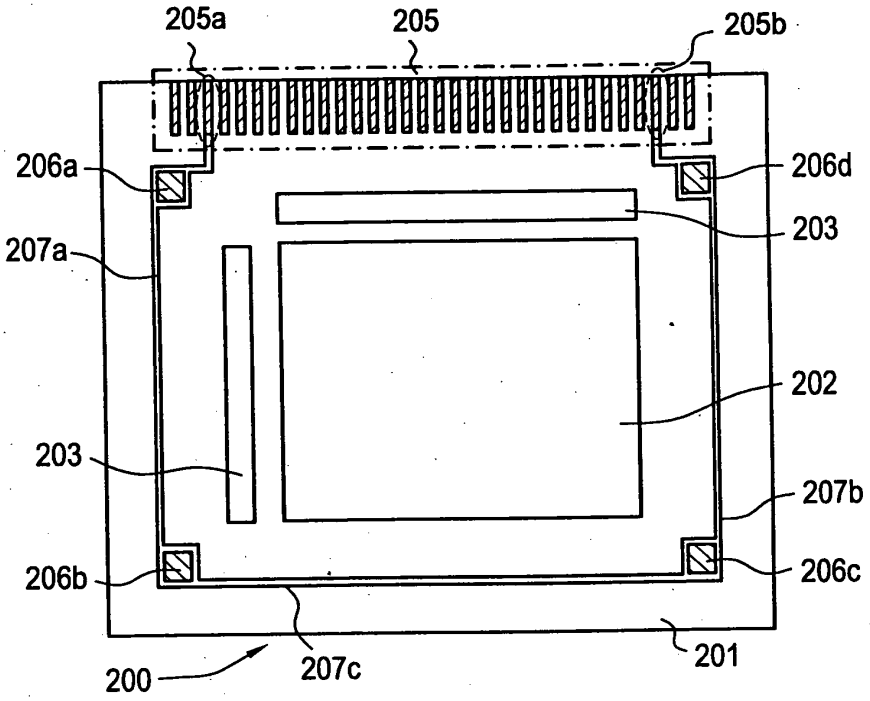


FIG.4

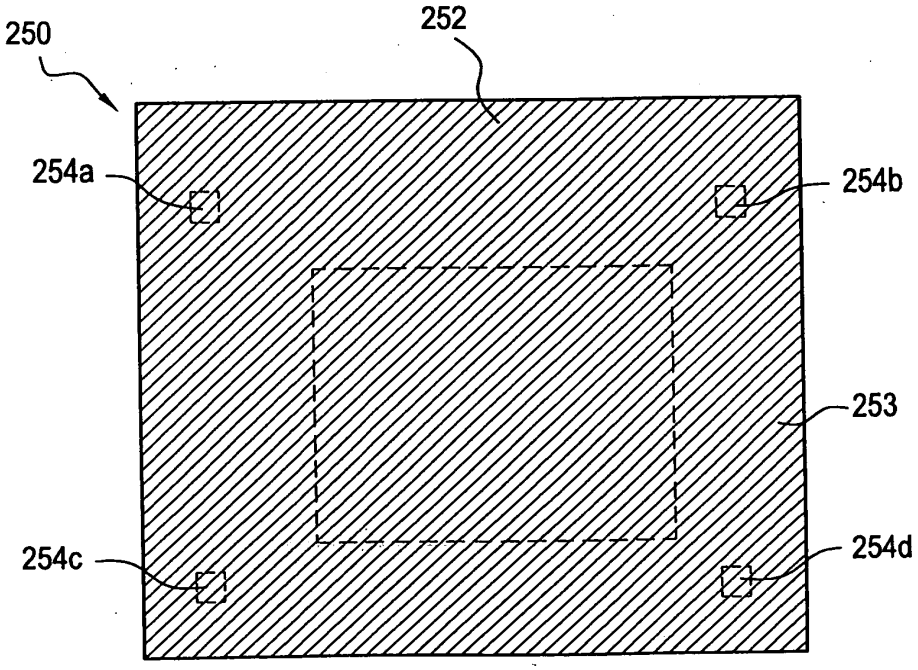


FIG.5A

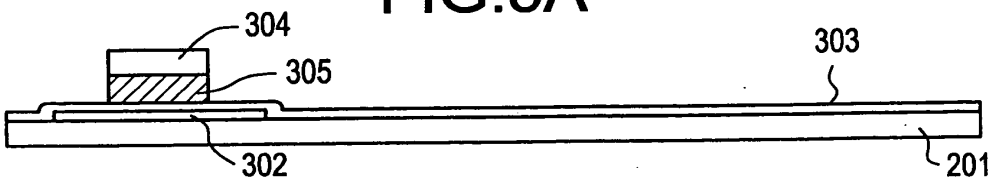


FIG.5B

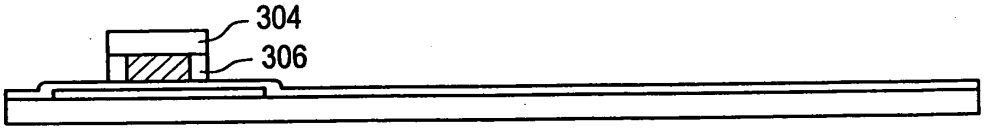


FIG.5C

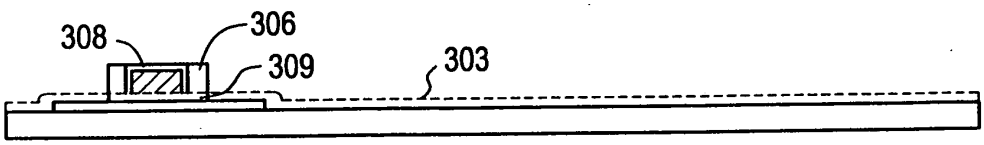


FIG.5D

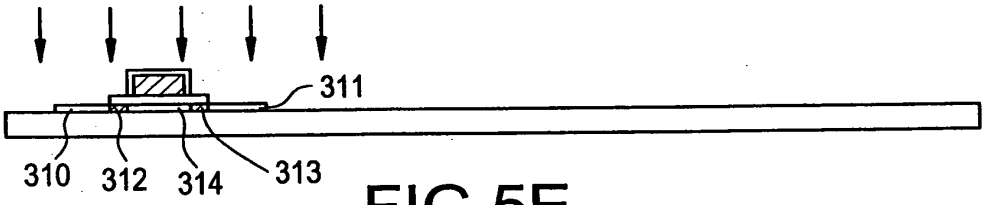


FIG.5E

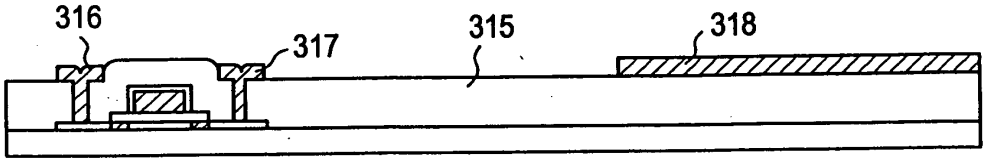


FIG.5F

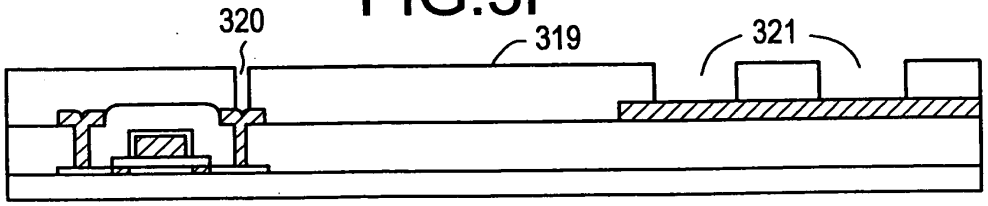


FIG.5G

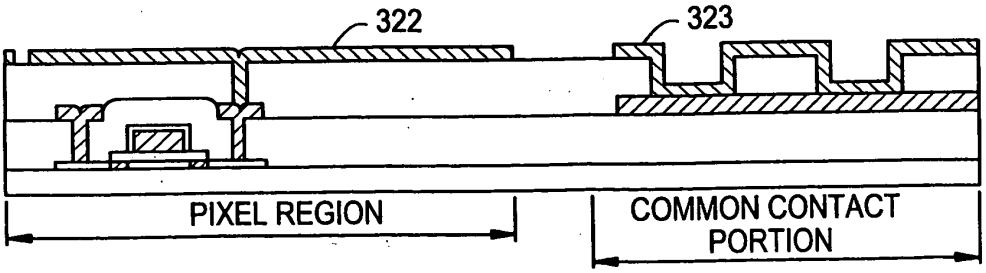


FIG.6

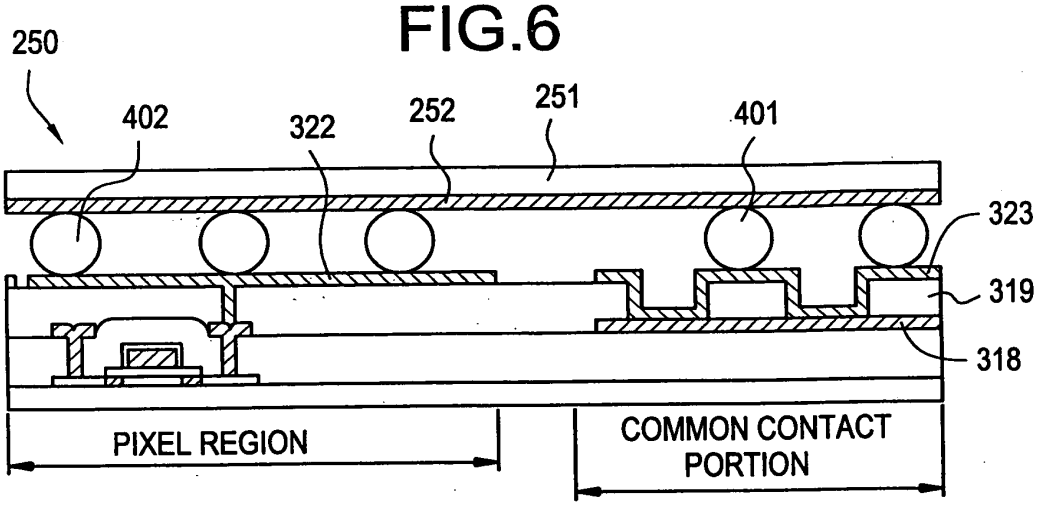


FIG.7

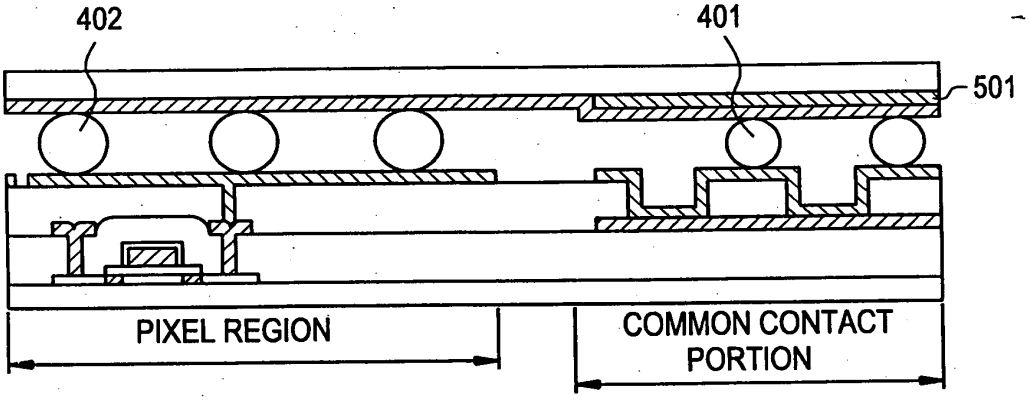


FIG.8

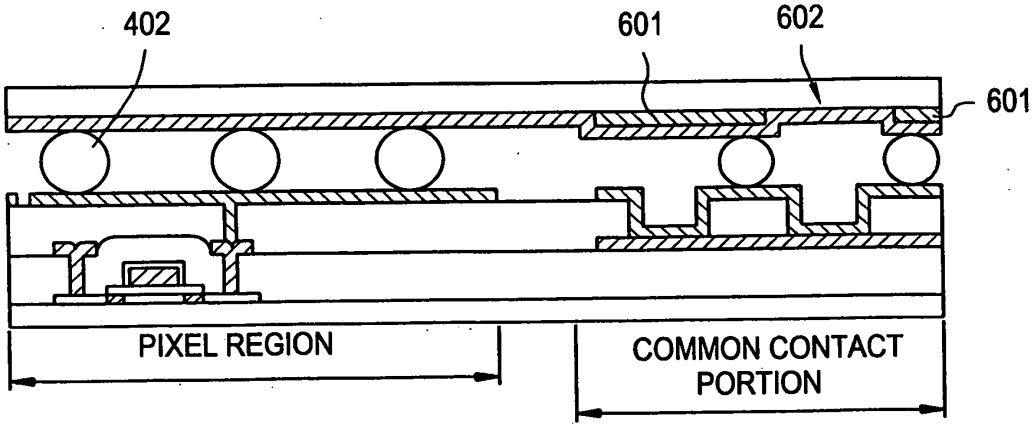


FIG.9

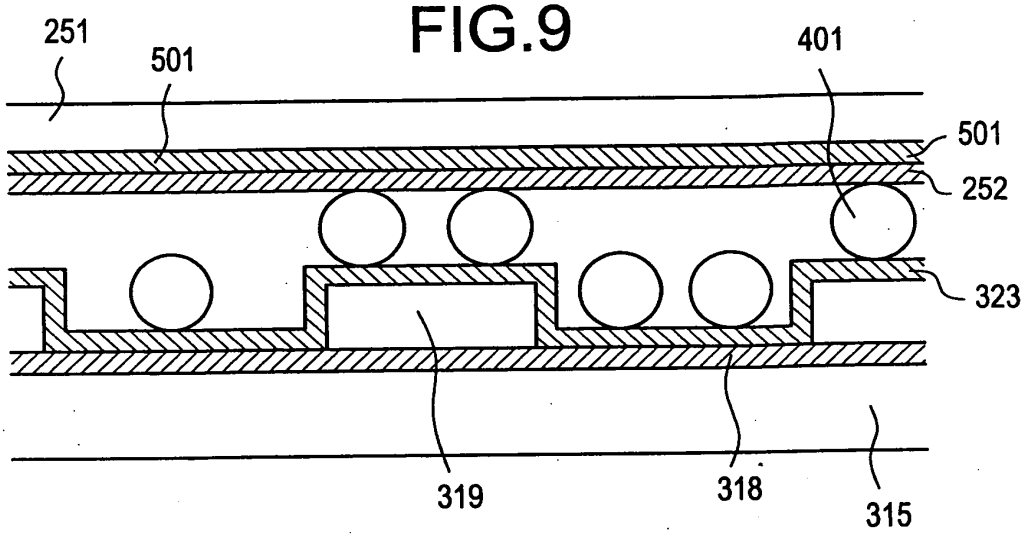


FIG.10

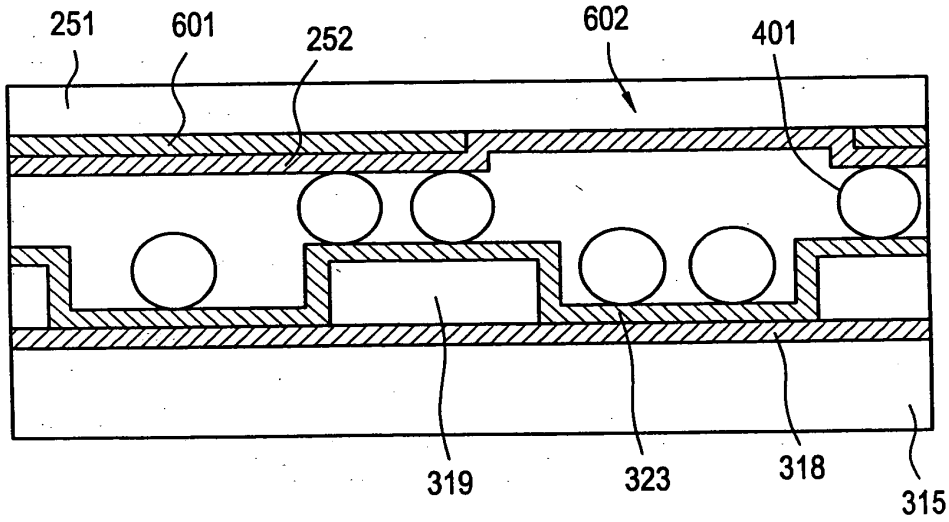


FIG.11

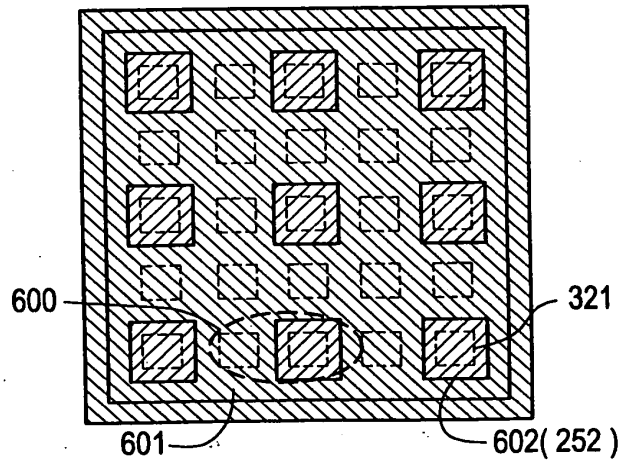


FIG.12
PRIOR ART

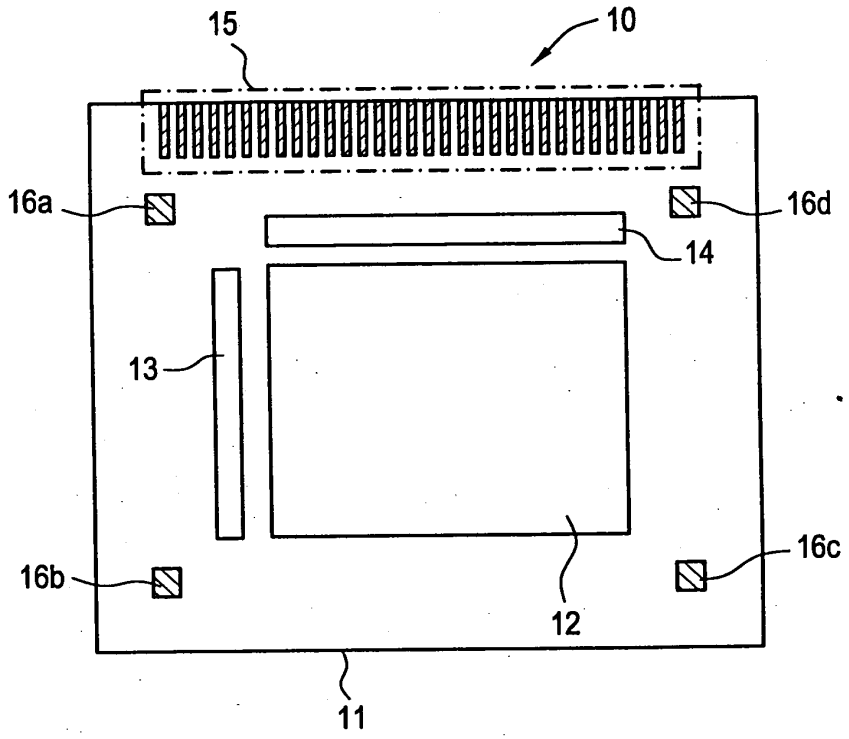


FIG.13
PRIOR ART

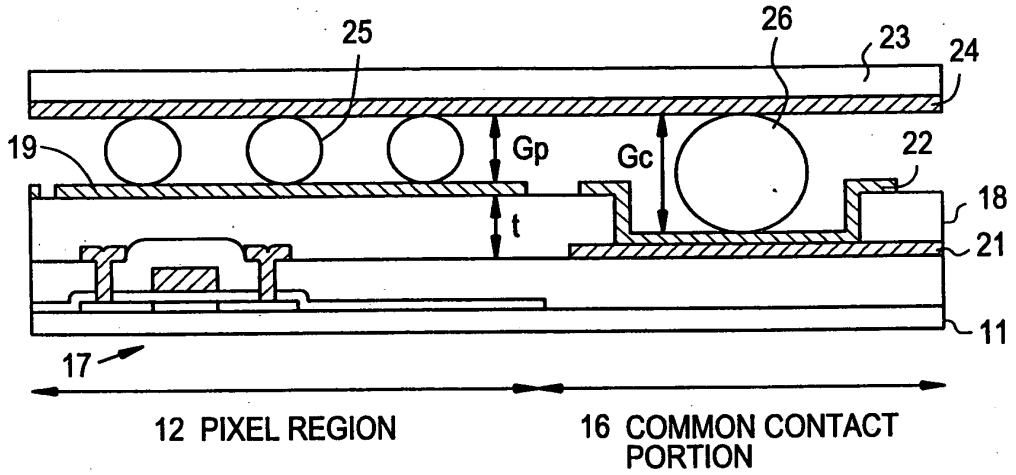
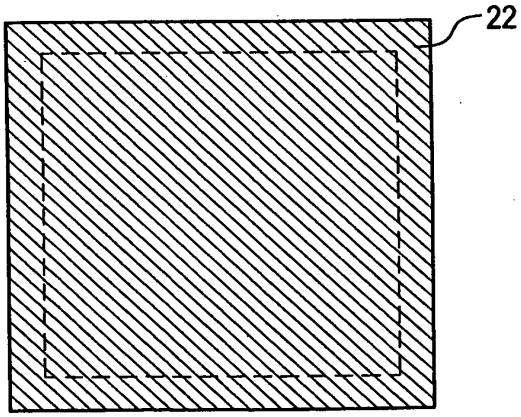


FIG.14
PRIOR ART



CONTACT STRUCTURE

Insert A1

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a contact structure for electrically connecting together conducting lines formed on two opposite substrates, respectively, via conducting spacers and, more particularly, to a contact structure used in common contacts of an electrooptical device such as a liquid crystal display.

Description of the Related Art

In recent years, liquid crystal displays have been extensively used in the display portions of mobile intelligent terminals such as mobile computers and portable telephones including PHS (personal handyphone system). Also, active-matrix liquid crystal displays using TFTs as switching elements are well known.

A liquid crystal display comprises two substrates and a liquid crystal material sealed between them. Electrodes are formed on these two substrates to set up electric fields. A desired image or pattern is displayed by controlling the magnitudes of these electric fields. In the active-matrix liquid crystal display, TFTs (thin-film transistors) are formed on one substrate to control the supply of voltage to each pixel electrode. Therefore, this substrate is referred to as the TFT substrate. A counter electrode placed opposite to the pixel electrodes is formed on the other substrate and so it is referred to as the counter substrate.

In the active matrix display, an electric field is produced between each pixel electrode on the TFT substrate and the counter electrode on the counter substrate, thus

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providing a display. The potential at each pixel electrode on the TFT substrate is controlled by the TFT and thus is varied. On the other hand, the counter electrode on the counter substrate is clamped at a common potential. For this purpose, the counter electrode is connected with an extractor terminal via a common contact formed on the TFT substrate. This extractor terminal is connected with an external power supply. This connection structure clamps the counter electrode at the common potential.

The structure of the common contact of the prior art active-matrix liquid crystal display is next described briefly by referring to Figs. 12 - 14.

Fig. 12 is a top plan view of a TFT substrate 10. This TFT substrate comprises a substrate 11 having a pixel region 12, a scanning line driver circuit 13, and a signal line driver circuit 14. In the pixel region 12, pixel electrodes and TFTs connected with the pixel electrodes are arranged in rows and columns. The scanning line driver circuit 13 controls the timing at which each TFT is turned on and off. The signal line driver circuit 14 supplies image data to the pixel electrodes. Furthermore, there are extractor terminals 15 to supply electric power and control signals from the outside. The substrate 11 makes connection with the counter electrode at common contact portions 16a - 16d.

Fig. 13 is a cross-sectional view of the pixel region 12 and a common contact portion 16 representing the common contact portions 16a - 16d. A TFT 17 and many other TFTs (not shown) are fabricated in the pixel region 12 on the substrate 11. An interlayer dielectric film 18 is deposited on the TFT 17. A pixel electrode 19 connected with the drain electrode of the TFT 17 is formed on the interlayer dielectric film 18.

A precursor for the source and drain electrodes of the TFT 17 is patterned into internal conducting lines 21 at the common contact portion 16. The interlayer dielectric film 18 is provided with a rectangular opening. A conducting pad 22 is formed in this opening and connected with the internal conducting lines 21. The pixel electrode 19 and the conducting pad 22 are patterned from the same starting film.

Fig. 14 is a top plan view of the known common contact portion 16. A region located inside the conducting pad 22 and indicated by the broken line corresponds to the opening formed in the interlayer dielectric film 18.

As shown in Fig. 13, a counter electrode 24 consisting of a transparent conducting film is formed on the surface of a counter substrate 23. This counter electrode 24 is opposite to the pixel electrodes 19 in the pixel region 12 and to the conducting pad 22 at the common contact portion 16.

Spherical insulating spacers 25 are located in the pixel region 12 to maintain the spacing between the substrates 11 and 23. A spherical conducting spacer 26 is positioned at the common contact portion 16 and electrically connects the counter electrode 24 with the conducting pad 22. The pad 22 is electrically connected with the internal conducting lines 21, which in turn are electrically connected with an extractor terminal 15. This connection structure connects the counter electrode 24 on the counter substrate 23 with the extractor terminal 15 on the substrate 11.

In the prior art liquid crystal display, the interlayer dielectric film 18 is provided with the opening at the common contact portion 16, as shown in Fig. 13. Therefore, the cell gap G_c in the common contact portion is almost equal

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to the sum of the cell gap G_p in the pixel region + the film thickness t of the interlayer dielectric film 18.

The cell gap G_p (also known as the cell spacing) in the pixel region 12 is determined by the insulating spacers 25. It is common practice to use standardized spacers as the insulating spacers 25 and so if the spacers 25 have a uniform diameter, the cell gap G_p in the pixel region 12 is substantially uniform among liquid-crystal cells. However, it is difficult to avoid nonuniformity of the cell gap G_c in the common contact portion among liquid-crystal cells.

The cell gap G_c in the common contact portion is constant since the cell gap G_p is constant because of the relation described above. Therefore, the cell gap G_c in the common contact portion depends only on the film thickness t of the interlayer dielectric film 18. Consequently, to make the cell gap G_c uniform among liquid-crystal cells, it is necessary that the film thickness t of this interlayer dielectric film 18 be uniform among cells. However, this is impossible to circumvent.

Normally, the common contact portions of the liquid crystal display are 2 to 4 in number. The film thickness t of the interlayer dielectric film 18 may differ from location to location on the same substrate. In this case, the film thickness t may differ among different common contacts even on the same substrate.

Because of the aforementioned nonuniformity of the thickness t of the interlayer dielectric film 18, the cell gap G_c in the common contact portion differs among different cells or different common contacts. Furthermore, the nonuniformity of the cell gap G_c results in the cell gap G_p in the pixel region to be nonuniform.

The cell gap G_p in the pixel region is affected more by the nonuniformity of the cell gap G_c in the common contact portion as the area of the pixel region 12 becomes narrower than the area of the common contact portion. Especially, in the case of a projection display as used in a projector, the problem of above-described nonuniformity of the cell gap G_p in the pixel region becomes conspicuous, because it is a quite accurate small-sized display of about 1 to 2 inches.

A standardized spacer is also used as the conducting spacer 26. The diameter of this conducting spacer 26 is determined by the diameter of the insulating spacers 25 in the pixel region 12 and by the design thickness of the interlayer dielectric film 18. Where the thickness of the interlayer dielectric film 18 is much larger than the designed value, the cell gap G_c in the common contact portion becomes very large. This makes it impossible to connect the counter electrode with the conducting pad well by the conducting spacer 26. In consequence, the counter electrode cannot be clamped at the common potential. As a result, a display cannot be provided.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a contact structure which is free of the foregoing problems, provides less nonuniform cell gap among different cells if the thickness of the interlayer dielectric film is nonuniform across the cell or among different cells, and reduces poor electrical contacts which would normally be caused by conducting spacers.

This object is achieved in accordance with the teachings of the invention by a contact structure for connecting a conducting film formed on a first substrate

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with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film by selectively leaving the dielectric film; a second conducting film covering the dielectric film left and the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the dielectric film left. The conducting spacers maintain the cell gap between the first and second substrates.

One embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film; an insulator deposited on only portions of the first conducting film exposed through the openings; a second conducting film covering the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates and connecting the second and

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third conducting films. The second conducting film is connected with the first conducting film through the openings extending through the insulator. The second conducting film, the conducting spacers, and the third conducting film are connected in turn through the openings extending through the insulator. The conducting spacers maintain the cell gap between the first and second substrates.

Another embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate of an electrooptical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereover, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film by selectively leaving the interlayer dielectric film;a second conducting film defining the counter electrode formed on the second substrate; a third conducting film covering the interlayer dielectric film left and the openings; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings. The third conducting film and the pixel electrodes are formed from a common starting film. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the dielectric film left. The conducting spacers maintain the spacing between the first and second

8

substrates.

A further embodiment of the invention resides in a contact structure for connecting a first conducting film formed over a first substrate of an electrooptical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereon, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film; an insulator formed on selected portions of the surface of the first conducting film extending through the openings; a second conducting film covering the openings; a third conducting film defining the counter electrode formed on the second substrate; conducting spacers held between the first and second substrates and connecting the second and third conducting films. The pixel electrodes and the second conducting film are formed from a common starting film. The second conducting film is connected with the first conducting film through the openings extending through the insulator. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the insulator formed in the openings. The conducting spacers maintain the cell gap between the first and second substrates.

A still other embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first

and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film and exposing parts of the first conducting film; a second conducting film covering the openings;a third conducting film formed over the second substrate;a fourth conducting film formed between the second substrate and the third conducting film and in contact with the third conducting film; and conducting spacers held between the first and second substrates. The first conducting film, the second conducting film, the conducting spacers, the third conducting film, and the fourth conducting films are connected in turn through the openings. The spacers maintain the cell gap between the first and second substrates.

Other objects and features of the invention will appear in the course of the description thereof, which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a fragmentary cross-sectional view of a common contact portion in accordance with the present invention;

Figs. 2A and 2B are top plan views of the common contact portion shown in Fig. 1;

Fig. 3 is a top plan view of the TFT substrate of a liquid crystal display in accordance with Example 1 of the invention;

Fig. 4 is a top plan view of the counter substrate of the liquid crystal display in accordance with Example 1;

Figs. 5A - 5G are cross-sectional views illustrating a process sequence for fabricating the TFT substrate shown in Fig. 3;

Fig. 6 is a fragmentary cross-sectional view of a pixel region and a common contact portion of the liquid crystal display in accordance with Example 1;

Fig. 7 is a cross-sectional view similar to Fig. 6, but illustrating Example 2 of the invention;

Fig. 8 is a cross-sectional view similar to Fig. 6, but illustrating Example 3 of the invention;

Fig. 9 is an enlarged cross-sectional view of the common contact portion shown in Fig. 7;

Fig. 10 is an enlarged cross-sectional view of the common contact portion shown in Fig. 8;

Fig. 11 is a top plan view of the common contact portion shown in Fig. 8;

Fig. 12 is a top plan view of the TFT substrate of the prior art liquid crystal display;

Fig. 13 is a cross-sectional view of a pixel region and a common contact portion on the TFT substrate shown in Fig. 12; and

Fig. 14 is a top plan view of the common contact portion shown in Fig. 13.

DETAILED DESCRIPTION OF THE INVENTION

EMBODIMENT 1

The present embodiment of this invention is described by referring to Figs. 1, 2A and 2B. Fig. 1 is a fragmentary cross-sectional view of a common contact portion of a liquid crystal display in accordance with the present embodiment. Figs. 2A and 2B are top plan views of the TFT substrate of the liquid crystal display. The structure of a region 120 shown in Fig. 2A is depicted in the enlarged cross section of Fig. 1.

As shown in Fig. 13, in the prior art structure, the

spacers in the pixel region 12 are located over the interlayer insulating film 18 via the pixel electrode 19. However, the interlayer dielectric film 18 does not exist under the conducting pad 22 at the common contact portion 16. Hence, the cell gap G_c in the common contact portion depends on the thickness of the interlayer dielectric film 18.

Accordingly, in the present embodiment, an insulator, or a dielectric, is inserted under the conducting pad in the common contact portion. Conducting spacers are placed on top of the dielectric, so that the cell gap G_c in the contact portion does not depend on the thickness of the interlayer dielectric film 18. In the present embodiment, openings are formed, selectively leaving the interlayer dielectric film 18.

In the present embodiment, as shown in Fig. 1, a first conducting film 103 is formed on a first substrate 101. A dielectric film 104 is deposited on the first conducting film 103. The dielectric film 104 is selectively left to form openings 111 that expose parts of the first conducting film 103. A second conducting film 105 is formed so as to cover the left parts of the dielectric film, 104a, and the openings 111.

A third conducting film 106 is formed on the second substrate 102. Conducting spacers 107 are sandwiched between the first substrate 101 and the second substrate 102.

In the prior art opening 110 shown in Fig. 2A, the dielectric film 104 has been fully removed. In the present embodiment, the dielectric film 104 is selectively left to form the dielectric film portions 104a and the openings 111. The openings 111 expose parts of the first conducting film

103. The first conducting film 103 is connected with the second conducting film 105 at these openings 111.

On the first substrate 101, the left dielectric film 104a is closest to the second substrate 102; therefore, on the left dielectric film 104a, the second conducting film 105 formed on the first substrate electrically connects with the third conducting film 106 formed on the second conducting film 102 through the conducting spacer 107, as shown in Fig. 1.

In region 110, the left dielectric film 104a is closest to the second substrate; therefore, the conducting spacers 107 electrically connecting the second conducting film 105 with the third conducting film 106 maintain the gap G between the substrates. Consequently, this gap G is dependent only on the size of the conducting spacers 107. Therefore, where the conducting spacers 107 are uniform among liquid-crystal cells, the gap G can be made uniform among cells, even if the thickness t of the dielectric film 104 differs among cells.

In the present embodiment, it is desired that the area of each opening 111 be sufficiently larger than the area occupied by each conducting spacer and offer space so that the conducting spacers can move freely, because the spacers 107 existing in the openings 111 do not contribute toward maintaining the gap. Otherwise, plural conducting spacers 107 would be stacked on top of each other, making it impossible to maintain the cell gap G uniform across the cell.

Also in the present embodiment, it is desirable that the area of the surface of each left dielectric film portion 104a be sufficiently larger than the area occupied by each conducting spacer 107, assuring arrangement of the

conducting spacers 107. If the spacers 107 are not positioned over the dielectric film 104a with certainty, it will not be possible to make electrical connections between the first and second substrates. Furthermore, the gap will not be maintained.

The openings 111 are formed as shown in Fig. 2A in the present embodiment. The relation between the left dielectric film 104a and each opening 111 may be reversed as shown in Fig. 2B. It is that noted Fig. 1 is an enlarged view of the region 120 indicated by the broken line in Fig. 2B.

EMBODIMENT 2

The present embodiment is described by referring to Figs. 1 and 2A. Fig. 1 is a cross-sectional view of a common contact portion of the liquid crystal display in accordance with the present embodiment. Fig. 2A is a top plan view of the TFT substrate of the liquid crystal display. Fig. 1 is an enlarged cross-sectional view of the region 120 indicated by the broken line in Fig. 2A.

A dielectric is inserted under a conducting pad in the common contact portion, in the same manner as in Embodiment 1. Conducting spacers are positioned on the dielectric. Thus, the cell gap G_c in the common contact portion does not depend on the thickness of the interlayer dielectric film 18. The present embodiment is characterized in that the dielectric film 18 is selectively left to form openings.

In particular, in the present embodiment, the dielectric layer is formed underneath the conducting pad 22. The conducting spacers are positioned on the dielectric. Consequently, the cell gap G_c in the common contact portion is not dependent on the thickness of the interlayer

dielectric film 18.

Referring to Fig. 1, a first conducting film 103 is formed on top of a first substrate 101. A dielectric film 104 covers the first conducting film 103. The dielectric film 104 is provided with openings 111 to selectively expose the surface of the first conducting film 103. The exposed portions of the dielectric 104 are indicated by 104a. A second conducting film 105 is formed to cover the openings 111.

A third conducting film 106 is formed on the second substrate 102. Conducting spacers 107 are located between the first substrate 101 and the second substrate 102.

Fig. 2A is a top plan view of the TFT substrate, and in which the second conducting film 105 is not yet deposited. In Fig. 2A, the region 110 indicated by the broken line corresponds to the opening for the common contact formed in the interlayer dielectric film 18 of the prior art structure. A dielectric 104a is selectively deposited to leave portions of the first conducting film 103 to be exposed.

The first conducting film 103 is exposed at locations where the dielectric 104a is not deposited. The exposed portions of the first conducting film 103 are connected with the overlying second conducting film 105.

On the first substrate 101, the dielectric 104a is closest to the second substrate. As shown in Fig. 1, on the dielectric 104a, conducting spacers 107 electrically connect the second conducting film 105 on the first substrate 101 with the third conducting film 106 on the second substrate 102.

The dielectric 104a is closest to the second substrate 102. Therefore, the conducting spacers 107 electrically

connecting the second conducting film 105 with the third conducting film 106 hold the cell gap G. In consequence, the gap G is dependent only on the size of the conducting spacers 107. Where the spacers 107 are uniform in size, the cell gap G can be rendered uniform among liquid-crystal cells even if the thickness t of the dielectric film 104 differs among cells.

In the present embodiment, the area of each portion not covered with the dielectric 104a is preferably sufficiently wider than the area occupied by one conducting spacer 107 and permits the conducting spacers 107 to move freely, because the spacers 107 existing in the regions where the dielectric 104a is not present do not contribute toward maintaining the gap. Otherwise, plural conducting spacers 107 would be stacked on top of each other, making it impossible to maintain the cell gap G uniform across the cell.

Also in the present embodiment, it is desirable that the area of each portion of the dielectric film 104a be sufficiently larger than the area occupied by one conducting spacer 107 and that the conducting spacers 107 be arranged with certainty. If the spacers 107 are not positioned on the dielectric film 104a with certainty, it will not be possible to make electrical connections between the first and second substrates. Furthermore, the cell spacing will not be maintained.

In this embodiment, the dielectric 104a is deposited as shown in Fig. 2A. The relation between the regions where the dielectric 104a is deposited and each region where the first conducting film 103 is exposed may be reversed as shown in Fig. 2B.

EXAMPLE 1

In this example, the present invention is applied to a common contact portion of a reflection-type liquid crystal display. Fig. 3 is a top plan view of the TFT substrate of this liquid crystal display. Fig. 4 is a top plan view of the counter substrate of the liquid crystal display.

Referring to Fig. 3, the TFT substrate 200 comprises a substrate 201 having a pixel region 202, a scanning line driver circuit 203, and a signal line driver circuit 204. Pixel electrodes and TFTs connected with the pixel electrodes are arranged in rows and columns in the pixel region 202. The scanning line driver circuit 203 controls the timing at which each TFT is turned on and off. The signal line driver circuit 204 supplies image data to the pixel electrodes. Extractor terminals 205 are also provided to supply electric power and control signals from the outside. Common contact portions 206a - 206d form junctions with the counter electrode.

As shown in Fig. 4, the counter substrate 250 comprises a substrate on which a counter electrode 252 consisting of a transparent conducting film is deposited. A central rectangular region 253 is opposite to the pixel region 202 of the TFT substrate 200. Four corner regions 254a - 254d are electrically connected with the contact portions 206a - 206d, respectively, of the TFT substrate 200.

As shown in Fig. 3, conducting pads are formed in the common contact portions 206a - 206d, respectively, of the TFT substrate 200. These conducting pads are electrically connected together by internal conducting lines 207a - 207c. The internal lines 207a and 207b extend to the extractor terminals 205 and are electrically connected with common terminals 205a and 205b, respectively.

A process sequence for manufacturing the pixel region 202 and the common contact portion 206a - 206d on the TFT substrate is next described by referring to Figs. 5A - 5G.

First, the substrate 201 having an insulating surface was prepared. In the present example, a silicon oxide film was formed as a buffer film on the glass substrate. An active layer 302 consisting of a crystalline silicon film was formed over the substrate 201. Although only one TFT is shown, millions of TFTs are built in the pixel region 202 in practice.

In the present example, an amorphous silicon film was thermally crystallized to obtain the crystalline silicon film. This crystalline silicon film was patterned by an ordinary photolithographic step to obtain the active layer 302. In this example, a catalytic element such as nickel for promoting the crystallization was added during the crystallization. This technology is described in detail in Japanese Unexamined Patent Publication No.7-130652.

Then, a silicon oxide film 303 having a thickness of 150 nm was formed. An aluminum film (not shown) containing 0.2% by weight of scandium was deposited on the silicon oxide film 303. The aluminum film was patterned, using a resist mask 304, into an island pattern 305 from which gate electrodes will be formed (Fig. 5A).

The present example made use of the anodization technique described in Japanese Unexamined Patent Publication No. 7-135318. For further information, refer to this publication.

First, the island pattern 305 was anodized within a 3% aqueous solution of oxalic acid while leaving the resist mask 304 on the island pattern 305, the mask 304 having been used for the patterning step. At this time, an electrical

current of 2 to 3 mV was passed, using a platinum electrode as a cathode. The voltage was increased up to 8 V. Since the resist mask 304 was left on the top surface, porous anodic oxide film 306 was formed on the side surfaces of the island pattern 305 (Fig. 5B).

After removing the resist mask 304, anodization was carried out within a solution prepared by neutralizing a 3% aqueous solution of tartaric acid with aqueous ammonia. At this time, the electrical current was set to 5 - 6 mV. The voltage was increased up to 100 V. In this way, a dense anodic oxide film 307 was formed.

The above-described anodic oxidation step defined the unoxidized island pattern 305 into gate electrodes 308. Internal connecting lines 207c interconnecting the common contact portions 206c and 206d were created from the aluminum film described above simultaneously with the gate electrodes 308.

Then, using the gate electrodes 308 and surrounding anodic oxide film 306, 307 as a mask, the silicon oxide film 303 was etched into a gate insulating film 309. This etching step relied on dry etching using CF_4 gas (Fig. 5C).

After the formation of the gate insulating film 309, the porous anodic oxide film 307 was removed by wet etching using Al mixed acid.

Thereafter, impurity ions for imparting one conductivity type were implanted by ion implantation or plasma doping. Where N-type TFTs are placed in the pixel region, P (phosphorus) ions may be implanted. Where P-type TFTs are placed, B (boron) ions may be implanted.

In the present example, the above-described process for implanting the impurity ions was carried out twice by ion implantation. The first step was performed under a high

accelerating voltage of 80 keV. The system was so adjusted that the peak of the impurity ions was brought under the ends (protruding portions) of the gate insulating film 309. The second step was effected under a low accelerating voltage of 5 keV. The accelerating voltage was adjusted so that the impurity ions were not implanted under the ends (protruding portions) of the gate insulating film 309.

In this way, a source region 310, a drain region 311, lightly doped regions 312, 313, and a channel region 314 for the TFT were formed. The lightly doped region 313 on the side of the drain region 311 is also referred to as the LDD region (Fig. 5D).

At this time, it is preferable to implant the impurity ions to such a dosage that the source and drain regions 310 and 311, respectively, exhibit a sheet resistance of 300 to 500 Ω/□. In addition, it is necessary to optimize the lightly doped regions 312 and 313 according to the performance of the TFT. After the impurity ion implantation step, a thermal treatment was carried out to activate the impurity ions.

Then, a 1 μm-thick-silicon oxide film was formed as a first interlayer dielectric film 315. The thickness of the interlayer dielectric film 315 was set to 1 μm to flatten the surface of the first interlayer dielectric film 315 as much as possible. This could mitigate the protrusions due to the gate electrodes 308.

The first interlayer dielectric film 315 may be made of silicon nitride or silicon oxynitride, as well as silicon oxide. Alternatively, the first interlayer dielectric film 315 may be a multilayer film of these materials.

Contact holes for gaining access to the source and drain regions 310 and 311, respectively, were created in the

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first interlayer dielectric film 315. Contact holes for allowing access to the internal conducting lines 207c were formed in the common contact portions 206c and 206d. Then, a conducting film forming a precursor for source and drain electrodes 316 and 317, respectively, and for internal conducting lines 318 was deposited.

In this example, the conducting film was created from a multilayer film of titanium (Ti), aluminum (Al), and titanium (Ti) by sputtering. Each of the titanium layers was 100 nm thick, while the aluminum layer was 300 nm thick. This multilayer film was patterned to form a source electrode 316, a drain electrode 317, and internal conducting lines 318 (Fig. 5E).

The internal conducting lines 318 shown Fig. 5E correspond to the internal conducting lines 207a and 207b shown in Fig. 3. These conducting lines 207a and 207b were connected with internal conducting lines 207c at the common contact portions 206c and 206d. The internal conducting lines 207c and the gate electrode 308 were created by the same processing steps.

Subsequently, an organic resinous film was formed as a second interlayer dielectric film 319 to a thickness of 1 to 2 μm. Polyimide, polyamide, polyimidamide, acrylic resin, or other material may be used as the material of the organic resinous film. The organic resinous material acts to planarize the surface of the second interlayer dielectric film 319. This is important to make the cell gap uniform. In the present example, polyimide was deposited as the second interlayer dielectric film 319 to a thickness of 1 μm.

Then, contact holes 320 and 321 were formed in the second interlayer dielectric film 319 to have access to the

drain electrode 317 and to the internal conducting lines 318, respectively. The contact holes 321 for the internal conducting lines 318 were formed in the openings 111 shown in Fig. 2A. That is, rectangular holes measuring 100 μm x 100 μm were arranged in 5 rows and 5 columns within the rectangular region 110 measuring 1.1 mm x 1.1 mm. These holes were spaced 100 μm from each other. Moreover, contact holes for connecting the internal conducting lines 318 (207a and 207b) with the common terminals 205a and 205b at the extractor terminals 205 were formed.

As described later, the size of each hole was set to 100 μm x 100 μm to set the diameter of the conducting spacers to 3.5 μm in this example. This provides sufficient space so that the conductive spacer located at this position can move. Hence, the conducting spacers are prevented from being stacked on top of each other.

The area of the left portions of the interlayer dielectric film 319 in the common contact portions is large enough to permit the conducting spacers to move. This assures that the conducting spacers are arranged in these regions. Consequently, the conducting spacers positioned in these regions can maintain the cell gap and make electrical connections reliably.

A thin metal film which would later be made into pixel electrodes 322 and a conducting pad 323 were formed to a thickness of 100 to 400 nm. In the present example, the thin metal film was made of an aluminum film containing 1 wt % titanium and deposited to a thickness of 300 nm by sputtering. Then, the thin metal film was patterned to form the pixel electrodes 322 and the conducting pad 323. This pad 323 measured 1.1 mm x 1.1 mm, was rectangular, and covered the contact holes 321. The extractor terminals 205

were also patterned. Thus, the TFT substrate was completed (Fig. 5G).

Referring to Fig. 6, the counter substrate 250 comprised a transparent plate 251 on which the counter electrode 252 was formed from an ITO film. A glass or quartz substrate can be used as the substrate 251.

Then, the TFT substrate 200 and the counter substrate 250 were bonded together. This bonding step may be a well-known cell assembly method.

First, a sealing material was applied to one of the TFT substrate 200 and the counter substrate 250. In this example, the sealing material was applied to the counter substrate 250. A UV-curable and thermosetting resin was used as the sealing material. This sealing material was applied around the substrate along straight lines except for the liquid crystal injection port by a sealant dispenser. A sealing material to which 3.0 wt % spherical conducting spacers 401 were added was applied to regions 254a - 254d shown in Fig. 4. The sealing material to which the conducting spacers were added functioned as an anisotropic conducting film.

Generally, the conducting spacers 401 consist of resinous spheres coated with a conducting film. In the present example, the conducting spacers 401 were coated with gold (Au). The diameter of the conducting spacers 401 may be larger than the cell gap by about 0.2 to 1 μm. In this example, the conducting spacers 401 had a diameter of 3.5 μm to set the cell gap to 3 μm. After applying the sealing material, it was temporarily baked.

Thereafter, spacers 402 were dispersed onto one of the TFT substrate 200 and the counter substrate 250 to maintain the cell gap. In this example, the spacers 402 were applied

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to the counter substrate 250. To set the cell gap to 3 μm, spherical spacers of a polymeric material were used as the spacers 402.

Then, the TFT substrate 200 and the counter substrate 250 were held opposite to each other, and they were pressed against each other until the cell gap in the pixel region was decreased to the diameter of the spacers 402. Under the pressed state, UV light was directed at this assembly for more than 10 seconds to cure the sealing material. The cell gap was fixed. Then, the assembly was heated under pressure, thus enhancing the adhesive strength.

Subsequently, a liquid crystal material was injected, and the entrance hole was sealed off, thus completing the cell assembly process. As shown in Fig. 6, the counter electrode 252 on the counter substrate 250 was electrically connected with the conducting pad 323 on the TFT substrate 200 by the conducting spacer 401. On the TFT substrate, the conducting pad 323 connected the internal conducting lines 318 with the common terminals. This connection structure permitted the counter electrode 252 on the counter substrate 250 to be connected with an external power supply via the conducting lines on the TFT substrate. Fig. 1 is an enlarged view of the common contact portion of Fig. 6.

In the present example, to set the cell gap to 3 μm, the spacers 402 applied to the pixel region had a diameter of 3 μm. The diameter of the conducting spacers 401 was 3.5 μm. Setting the diameter of the conducting spacers greater than the diameter of the spacers 402 (i.e., the cell gap) made reliable the connection between the counter electrode 252 and the conducting pad 318. When the two plates were being clamped together to bond them together, the conducting spacers 401 were crushed because they were larger in

diameter than the cell gap. This increased the areas of the portions in contact with the counter electrode 252 and with the conducting pad 318, respectively. Hence, the electrical connection was rendered more reliable. Furthermore, the cell gap could be maintained at the same dimension as in the pixel region.

In this example, the internal conducting lines 318 were made of the precursor for the source and drain electrodes 316 and 317, respectively. It is only necessary for the internal conducting lines 318 to be under the pixel electrodes 322. For instance, where a black matrix consisting of a conducting film of titanium or the like is formed inside the second interlayer dielectric film 315, the internal conducting lines 318 can be formed from this conducting film.

In the present example, it is important to flatten the surface of the second interlayer dielectric film 319 on which the pixel electrodes 322 are formed in order to make uniform the cell gap. Also, the flatness of the surface of the first interlayer dielectric film 315 where the internal conducting lines 318 are formed is important.

Methods of obtaining an interlayer dielectric film having a flat surface include a method of increasing the thickness of the interlayer dielectric film, a leveling method using an organic resinous film, a mechanical polishing method, and etch-back techniques. The present example made use of the method of increasing the film thickness to planarize the first interlayer dielectric film 315. Also, the method of relying on leveling using an organic resinous film was used to flatten the first interlayer dielectric film 315. Other methods may also be employed for the same purpose.

In a liquid crystal display in accordance with the present example, a dichroic dye may be dispersed in the liquid crystal layer. Orientation films may be deposited on the TFT substrate and on the counter substrate. Color filters may be formed on the counter substrate. The practitioner may appropriately determine the kind of the liquid crystal layer, the presence or absence of the orientation films and the color filters according to the driving method, the kind of the liquid crystal, and other factors.

For instance, where the color filters are mounted on the counter substrate 250, the color filters are not formed at the common contact portions and so steps are formed between the pixel region and the common contact portions on the counter substrate. To compensate for these steps, it is necessary to make the diameter of the conducting spacers larger by an amount almost equal to the thickness of the color filter.

In the present example, the liquid crystal display is of the reflection type. A transmissive liquid crystal display may also be fabricated. In this case, the precursor for the pixel electrode and for the conducting pad may be made of a transparent ITO film or the like.

In the example described above, the transistor is a coplanar TFT that is a typical top-gate TFT. It may also be a bottom-gate TFT. In addition, thin-film diodes, metal-insulator-metal (MIM) devices, metal-oxide varistors, and other devices can be used, as well as the TFTs.

EXAMPLE 2

The present example is a modification of the common contact portions of Example 1. Fig. 7 is a fragmentary

cross-sectional view of an active-matrix display in accordance with the present example. The configuration of a TFT substrate shown in Fig. 7 is the same as the configuration shown in Fig. 6, and some reference numerals are omitted. Like components are indicated by like reference numerals in both Figs. 6 and 7. Fig. 9 is an enlarged view of the common contact portion shown in Fig. 7.

In Example 1 shown in Fig. 6, the counter electrode 252 consists of an ITO film that is a transparent conducting film. Therefore, the counter electrode 252 and the conducting spacers 401 are larger in electrical resistance than metal films. The present example is intended to reduce this electrical resistance.

Accordingly, the resistance value between the counter electrode 252 and the conducting spacers 401 can be lowered by forming a metallization layer on the counter substrate 250 and patterning the metallization layer into conducting pads, or conducting film, 501 at the common contact portions 254a - 254d. Importantly, the conducting film forming the conducting pads 501 is lower in electrical resistance than the conducting film forming the counter electrode 252.

Where the black matrix on the counter substrate is formed from a conducting film as consisting of chromium, the connecting pads 501 can be formed from this conducting film. When the conducting film is patterned to form the black matrix, the connecting pad 501 may be created.

EXAMPLE 3

The present example is a modification of Example 2. Fig. 8 is a fragmentary cross-sectional view of an active-matrix display in accordance with the present example. The TFT substrate shown in Fig. 8 is identical in structure with

that shown in Fig. 6, and some reference numerals are omitted in Fig. 8. It is noted like components are denoted by like reference numerals in both Figs. 6 and 8. Fig. 10 is an enlarged view of the common contact portion of Fig. 8.

In Example 1, both counter substrate 251 and counter electrode 252 are transparent to light and so the distribution of the conducting spacers 401 on the common contact portions can be visually observed from the side of the counter substrate 250 after both substrates have been bonded together. In Example 2, however, the connecting pad 501 consisting of metallization layer is formed and, therefore, the distribution of the conducting spacers 401 cannot be visually checked.

The present example is intended to permit one to visually observe the distribution of the conducting spacers 401 while a connecting pad is provided to lower the resistance value. For this purpose, the connecting pad, 601, is provided with openings formed at selected locations. One can observe the conducting spacers 401 through these openings.

Fig. 11 is a top plan view of the contact portions according to the present example, taken from the side of the counter substrate. Fig. 10 is a cross-sectional view of the common contact portion in a region 600 surrounded by the broken line. As shown in Fig. 11, the conducting pad 601 is formed with openings 602. In each opening 602, there exist only the counter substrate 251 and the counter electrode 252, both of which have transparency. Hence, the distribution of the conducting spacers 401 can be observed through the openings 602.

To maintain the cell gap, the openings 602 should be formed opposite to the contact holes 321 formed in the

second interlayer dielectric film of the TFT substrate. At these locations, the conducting spacers 401 are not in contact with the counter electrode. The area of each opening 602 should be slightly larger than the area of each contact holes 321 formed in the second interlayer dielectric film, i.e., about several to thirty percent greater. The number of the openings 602, their arrangement, and their shape are not limited to the example of Fig. 11. Rather, one can arbitrarily set these geometrical factors.

Setting each opening 602 in the connecting pad 601 slightly larger than each contact holes 321 makes it possible to visually check the conducting pad 602 on the second interlayer dielectric film 319, which contributes to electrical connection.

In Examples 2 and 3, the cell gap in the common contact portions is made uniform. At the same time, the contact resistances of the conducting spacers 401 and of the counter electrode 252 are decreased. If the main purpose is to lower these resistance values, the common contact portions on the TFT substrate may have the prior art structure as shown in Fig. 13. In this case, any of the connecting pads 501 and 601 described in Examples 2 and 3, respectively, may be formed between the substrate 23 and the counter electrode 24 at the common contact portions 16 shown in Fig. 13.

In Examples 1 - 3 described above, the present invention is applied to active-matrix liquid crystal displays. The contact structure in accordance with the present invention is applicable to any apparatus having a contact structure for electrically connecting conductors formed on one substrate with conducting conductors formed on the other opposite substrate via conducting spacers. For example, the novel contact structure can connect ICs built

on different silicon wafers.

The common contact structure in accordance with the present invention can eliminate variations of the cell gap among liquid-crystal cells even if the film thickness varies among interlayer dielectric films. Also, poor contacts due to conducting spacers can be reduced.

In particular, in accordance with the present invention, the cell gap depends only on the size of conducting spacers. Therefore, where the conducting spacers are uniform in size, the cell gap between opposite substrates or plates can be made uniform among different liquid-crystal cells, if the thickness of a dielectric film electrically insulating the first and second conducting films is different among different liquid-crystal cells.

IN THE CLAIMS:

1. An active matrix display device comprising:

a first substrate:

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having at least two openings;

a second conductive film provide on said second interlayer insulating film and in said openings;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said openings;

wherein at least one of said conductive spacers is held over said second interlayer insulating film and in contact with both said second conductive film and said third conductive film.

2. An active matrix display device according to claim 1, wherein each of said conductive spacers is a sphere coated with gold.

3. An active matrix display device according to claim 1, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

4. An active matrix display device according to claim 1, wherein siad active matrix display device further comprises a fourth conductive film between said third conductive film and second conductive film.

5. An active matrix display device according to claim 1, wherein said active matrix display device is a liquid crystal display device.

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6. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having at least two openings;

a second conductive film provided on said second interlayer insulating film and in said openings;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said openings,

wherein said conductive spacers are dispersed into a sealing material,

wherein at least one of said conductive spacers is held over said second interlayer insulating film and in contact with both said second conductive film and said third conductive film.

7. An active matrix display device according to claim 6, wherein each of said conductive spacers is a sphere coated with gold.

8. An active matrix display device according to claim 6, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

9. An active matrix display device according to claim 6, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

10. An active matrix display device according to claim 6, wherein said active matrix display device is a liquid crystal display device.

11. An active matrix display device comrpising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having at least two openings;

a second conductive film provided on said second interlayer insulating film and in said openings;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said openings;

wherein at least one of said conductive spacers is held over said second interlayer insulating film and in contact with both said second conductive film and said third conductive film,

wherein each of said openings occupies an area larger than an area occupied by each of said conductive spacers.

12. An active matrix display device according to claim 11, wherein each of said conductive spacers is a sphere coated with gold.

13. An active matrix display device according to claim 11, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

14. An active matrix display device according to claim 11, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

15. An active matrix display device according to claim 11, wherein said active matrix display device is a liquid crystal display device.

16. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate:

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having an opening with a part of said second interlayer insulating film remaining in said opening;

a second conductive film provided on said second interlayer insulating film and in said opening;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said opening,

wherein at least one of said conductive spacers is held over said part of said second interlayer insulating film and in contact with both said second conductive film and conductive film.

17. An active matrix display device according to claim 16, wherein each of said conductive spacers is a sphere coated with gold.

18. An active matrix display device according to claim 16, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

19. An active matrix display device according to claim 16, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

20. An active matrix display device according to claim 16, wherein said active matrix display device is a liquid crystal display device.

21. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said conductive film, said second interlayer insulating film having an opening with a part of said second interlayer insulating film remaining in said opening;

a second conductive film provided on said second interlayer insulating film and in said opening;

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between said first substrate and said second substrate;

wherein said first conductive film is connected with said second conductive film in said opening,

wherein said conductive spacers are dispersed into a sealing material,

wherein at least one of said conductive spacers is held over said part of said second interlayer insulating film and in contact with both said second conductive film and said third conductive film.

22. An active matrix display device according to claim 21, wherein each of said conductive spaces is a sphere coated with gold.

23. An active matrix display device according to claim 21, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

24. An active matrix display device according to claim 21, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

25. An active matrix display device according to claim 21, wherein said active matrix display is a liquid crystal display device.

26. An active matrix display device comprising:

a first substrate;

a first interlayer insulating film provided over said first substrate;

a first conductive film provided on said first interlayer insulating film;

a second interlayer insulating film provided on said first conductive film, said second interlayer insulating film having an opening with a part of said second interlayer insulating film remaining in said opening;

a second conductive film provided on said second interlayer insulating film and in said opening.

a second substrate opposed to said first substrate;

a third conductive film provided on said second substrate; and

a plurality of conductive spacers held between siad first substrate and said second susbtrate;

wherein said first conductive film is connected with said second conductive film in said opening,

wherein at least one of said conductive spacers is held over said part of said second interlayer insulating film and in conatact with both said second conductive film and said third conductive film,

wherein said opening occupies an area larger than an area occupied by each of said conductive spacers.

27. An active matrix display device according to claim 26, wherein each of said conductive spacers is a sphere coated with gold.

28. An active matrix display device according to claim 26, wherein said second interlayer insulating film comprises an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin.

29. An active matrix display device according to claim 26, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second conductive film.

30. An active matrix display device according to claim 26, wherein said active matrix display device is a liquid crystal display device.

ABSTRACT OF THE DISCLOSURE

There is disclosed a contact structure for electrically connecting conducting lines formed on a first substrate of an electrooptical device such as a liquid crystal display with conducting lines formed on a second substrate via conducting spacers while assuring a uniform cell gap among different cells if the interlayer dielectric film thickness is nonuniform across the cell or among different cells. A first conducting film and a dielectric film are deposited on the first substrate. Openings are formed in the dielectric film. A second conducting film covers the dielectric film left and the openings. The conducting spacers electrically connect the second conducting film over the first substrate with a third conducting film on the second substrate. The cell gap depends only on the size of the spacers, which maintain the cell gap.

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CONTACT STRUCTURE

上記発明の明細書（下記の箇でxまたはがついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ _月_日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____に訂正されました。

☒ was filed on March 24, 1998
as United States Application Number or
PCT International Application Number
09/046,685 and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0022
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
9-094606	Japan	March 27, 1997	☐
			☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は与に許可された特許の有効性が失われることを認識し、よってここに下記のごとく宣言を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
日本語宣言書

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

Daniel W. Sixbey, (Reg. No. 20,930) Stuart J. Friedman (Reg. No. 24,112) Charles M. Leedom, Jr. (Reg. No. 25,477)
Gerald J. Ferguson, Jr. (Reg. No. 23,016) David S. Safran (Reg. No. 27,997) Thomas W. Cole (Reg. No. 28,290)
Joan K. Lawrence (Reg. No. 29,940) Donald R. Studebaker (Reg. No. 32,815) Jeffrey L. Costellia (Reg. No. 35,483)
Evan R. Smith (Reg. No. 35,683) Tim L. Brocker (Reg. No. 36,092) Eric J. Robinson (Reg. No. 38,285)

書類送付先

Send Correspondence to:

SIDLEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102

SIDLEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)

Gerald J. Ferguson, Jr.
(703) 790-9110

Gerald J. Ferguson, Jr.
(703) 790-9110

唯一または第一発明者		Full name of sole or first inventor Yoshiharu HIRAKATA
発明者の署名	日付	Inventor's signature Yoshiharu Hirakata Date June 1, 1998
住所		Residence Kanagawa, Japan
国籍		Citizenship Japanese
私書箱		Post Office Address c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan
第二共同発明者		Full name of second joint inventor, if any Shunpei YAMAZAKI
発明者の署名	日付	Inventor's signature Shunpei Yamazaki Date June 2, 1998
住所		Residence Tokyo, Japan
国籍		Citizenship Japanese
私書箱		Post Office Address c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

☐ Please see attached page 3a for names, addresses and signatures of additional inventors, if any.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

12/13/2000 MABDI1 00000024 09734177

01 FC:101	710.00	OP
02 FC:102	240.00	OP
03 FC:103	180.00	OP
04 FC:104	270.00	OP

PTO-1556
(5/87)

*U.S. GPO: 2000-468-987/39595

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 30	Minus	** 30	=
Independent	* 6	Minus	*** 6	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
***If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2000

Application or Docket Number: 09/734,177

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	30	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	30 minus 20=	* 10
INDEPENDENT CLAIMS	6 minus 3 =	* 3
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	355.00	OR	BASIC FEE	710.00
X$ 9=		OR	X$18=	180.00
X40=		OR	X80=	240.00
+135=		OR	+270=	
TOTAL		OR	TOTAL	1130.00

CLAIMS AS AMENDED - PART II

Pre Amdt

AMENDMENT A	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 30	Minus	** 30	= —
Independent	* 6	Minus	*** 6	= —
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1)		(Column 2)	(Column 3)
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

875

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

CLAIMS ONLY

SERIAL NO. 09/734177 | FILING DATE 12-12-00

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT		*		*		*	
	IND.	DEP.	IND.	DEP.	IND.	DEP.	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	1						51						
2		1					52						
3		1					53						
4		1					54						
5		1					55						
6	1						56						
7		1					57						
8		1					58						
9		1					59						
10		1					60						
11	1						61						
12		1					62						
13		1					63						
14		1					64						
15		1					65						
16	1						66						
17		1					67						
18		1					68						
19		1					69						
20		1					70						
21	1						71						
22		1					72						
23		1					73						
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25		1					75						
26	1						76						
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41							91						
42							92						
43							93						
44							94						
45							95						
46							96						
47							97						
48							98						
49							99						
50							100						
TOTAL IND.	6						TOTAL IND.						
TOTAL DEP.	24						TOTAL DEP.						
TOTAL CLAIMS	30						TOTAL CLAIMS						

* MAY BE USED FOR ADDITIONAL CLAIMS OR AMENDMENTS

PTO-2022 (1-98)

U.S.DEPARTMENT OF COMMERCE
Patent and Trademark Office

*U.S. GPO: 1998-443-593/89152

Docket No.: 0756-2237

#21A 26Jan01 R. Tallo

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **DIVISIONAL** Application of	)	
Yoshiharu HIRAKATA et al	)	
Based On Serial No. 09/361,218	)	Art Unit: 2871
Which was filed: July 27, 1999	)	Examiner: D. Nguyen
For: CONTACT STRUCTURE	)	

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 09/361,218 filed July 27, 1999, now U.S. PAT. No. 6,177,974; which itself is a Divisional of Serial No. 09/046,685 filed March 24, 1998 now U.S Patent 5,982,471.--

A1

REMARKS

This application has been amended to include the continuing application data thereof.

38

A

Examination on the merits is requested.

Respectfully submitted,

Eric J. Robinson
Registration No. 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

EJR/sas

Docket No.: 0756-2237

#3
26 Jan 01
R. Talbert

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **Divisional** Application of	)	
Yoshiharu HIRAKA et al	)	
Based On Serial No.: 09/361,218	)	Art Unit: 2871
Which was filed: July 27, 1999	)	Examiner: D. Nguyen
For: CONTACT STRUCTURE	)	

INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner for Patents

Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, it is requested that the reference listed on the attached Form PTO-1449 be made of record in the above-identified application.

The references listed on the attached Form PTO-1449 were cited in parent application Serial Nos. 09/361,218, 09/046,685.

Respectfully Submittetd,

Eric J. Robinson
Registration No. 38,285

Nixon Peabody LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

ERJ/sas

NVA157161.1

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/734,177	12/12/00	HIRAKATA Y	0756-2237

022204
NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN VA 22102

MMC2/0228

EXAMINER	
NGUYEN, D	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 02/28/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 2000-473-000/44602

1- File Copy

Office Action Summary	Application No. 09/734,177	Applicant(s) Hirakata et al.
	Examiner Dung Nguyen	Group Art Unit 2871

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-30* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-30* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☒ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☒ received in Application No. (Series Code/Serial Number) *09/361,218*.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *3*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-30 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12-22 of U.S. Patent No. 5,982,471. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the application and the patent disclose the same liquid crystal display contact structure.

3. Claims 1-30 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 51-60 of U.S. Patent No. 6,177,974. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the application and the patent disclose the same liquid crystal display contact structure.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dung Nguyen whose telephone number is (703) 305-0423.

DN
02/24/2000

William L. Sikes
Supervisory Patent Examiner
Group 2871

Notice of References Cited

Application No.	Applicant(s)		
09/734,177	Hirakata et al.		
Examiner	Group Art Unit	Page 1 of 1	
Dung Nguyen	2871		

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	6,177,974	1/2001	Hirakata et al.	349	155
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

Please type a plus sign (+) inside this box → ☐

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	~~Not Yet Assigned~~ 09/734,177
Filing Date	December 12, 2000
First Named Inventor	Yoshiharu HIRAKATA et al
Group Art Unit	2871
Examiner Name	D. Nguyen
Attorney Docket Number	0756-2237

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DN		5,619,358		Tanaka et al	04/1997	—
DN		4,231,034		Bechteler	10/1980	—
DN		3,954,325		Borden	05/1976	—
DN		5,742,006		Grupp et al	04/21/1998	—
DN		5,982,471		Hirakata et al	11/09/1999	—
DN		5,966,594		Adachi et al	10/12/1999	—

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
NOT IN FILE	—	~~WO~~	~~97/06458~~			~~02/20/1997~~	—	~~Full~~

Examiner Signature	ONGUYEN	Date Considered	02/23/01

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

NVA29570.1

2871

Docket No. 0756-2237

#5 Response
Marsha
6/4/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	Art Unit: 2871
Yoshiharu HIRAKATA et al.	)	Examiner: D. Nguyen
Serial No. 09/734,177	)	
Filed: December 12, 2000	)	
For: CONTACT STRUCTURE	)	
	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with The United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on May 29, 2001

Lisa M. D...

RESPONSE

Honorable Commissioner of Patents
Washington, D.C. 20231

Sir:

The Official Action mailed February 28, 2001 has been received and its contents carefully noted. Claims 1-30 are pending in the present application.

With respect to the obviousness-type double patenting rejection as being unpatentable over U.S. Patents 5,982,471 and 6,177,974, Applicant is preparing and will file a Terminal Disclaimer in order to overcome this rejection. Applicant's undersigned attorney will forward the Terminal Disclaimer to the Examiner's attention upon receipt from Japan.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

N183399.1

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/734,177	12/12/00	HIRAKATA Y	0756-2237

EXAMINER	
NGUYEN, D	
ART UNIT	**PAPER NUMBER**
2871	10

022204
NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN VA 22102

MM92/0705

DATE MAILED: 07/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 2000-473-000/44602

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/734,177	Hirakata et al.
Examiner	**Art Unit**
Dung Nguyen	2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 31, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-30* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

Applicant's response dated 05/31/2001 has been received and entered.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

In view of the newly discovered, rejections based on the newly cited reference follow:

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4,9,14,19,24 and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding the above claims, it is confusing and unclear how a fourth conductive film can be formed between a third conductive film and a second conductive film. According to the specification and drawings, the fourth conductive film (i.e., a black matrix) is formed on a second substrate and the third conductive film (i.e., the common electrode) is formed over the

fourth conductive film. Therefore, it is assumed for the purpose of the examination the fourth conductive film forming between the third conductive film and the second substrate.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

5. Claims 1, 4-6, 9-11, 14-16, 19-21, 24-26 and 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al., US Patent No. 6,219,124.

The above claims are anticipate by Lee et al. figure 1 which discloses a liquid crystal display device comprising:

- a first substrate (1);
- a first interlayer insulating film (3);
- a first conductive film (5);
- a second interlayer insulating film (7) having at least two openings (A and B), wherein the first conductive film is connected with the second conductive film in the openings;
- a second conductive film (9);
- a second substrate (19);

• a third conductive film (17);

• a fourth conductive film (13) forming between the third conductive film and the second substrate;

• a plurality of conductive spacers (11), wherein the conductive spacers contacted with both the second conductive film and the third conductive film.

It should be noted that of the filling date of the US Patent No. 6,219,124 (04/10/1997) is after the foreign priority date of the instant application. If Applicants wish to overcome such prior art, then sworn translation of the foreign priority documents will need to filed with the response to this Office Action.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3, 7-8, 12-13, 17-18, 22-23 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al., US Patent No. 6,219,124.

Regarding claims 2, 7, 12, 17, 22 and 27, Lee et al. disclose the claimed invention as described above except for the gold based material for spacers. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a gold based

material as a conductive material for a conductive spacer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Regarding claims 3, 8, 13, 18, 23 and 28, Lee et al. disclose the claimed invention as described above except for the second interlayer insulating comprising an organic resin selected from the group consisting of polyimide, polyamide, polyimidamide and acrylic resin. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an organic material (e.g., acrylic resin, polyimide, polyamide) for an interlayer insulating film, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

Double Patenting

8. Claims 1-30 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12-22 of U.S. Patent No. 5,982,471 , as stated in the previous office action.

9. Claims 1-30 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 51-60 of U.S. Patent No. 6,177,974 , as stated in the previous office action.

Applicants' response to the double patenting rejection (response dated 05/31/2001) is acknowledged.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dung Nguyen whose telephone number is (703) 305-0423. The fax phone number for this Group is (703) 308-7722.

Any information of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 308-0956.

DN
07/02/2001

William L. Sikes
Supervisory Patent Examiner
Group 2871

Notice of References Cited

Applicant/Patent	Application/Control No.	
Hirakata et al.	09/734,177	
Examiner	Art Unit	Page 1 of 1
Dung Nguyen	2871	

U.S. PATENT DOCUMENTS

		Document Number Country Code-Number-Kind Code	Date MM-YYYY[1]	Name	Classification[2]	
	A	6,219,124	4/2001	Lee et al.	349	147
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

		Document Number Country Code-Number-Kind Code	Date MM-YYYY[1]	Country	Name	Classification[2]	
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

		Include, as applicable: Author, Title, Date, Publisher, Edition or Volume, Pertinent Pages
	U	
	V	
	W	
	X	

* A copy of this reference is not being furnished with this Office action. See MPEP § 707.05(a). [1] Dates in MM-YYYY format are publication dates. [2] Classifications may be U.S. or foreign.

GAU 2871

Please type a plus sign (+) inside this box → [+]

PTO/SB/21 (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

OIPE 2177 OCT 05 2001 PATENT & TRADEMARK OFFICE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/734,177
Filing Date	December 12, 2000
First Named Inventor	Yoshiharu HIRAKATA et al.
Group Art Unit	2871
Examiner Name	D. Nguyen
Total Number of Pages in This Submission	
Attorney Docket Number	740756-2237

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [x] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [x] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance Communication to Group
- [ ] Other

RECEIVED OCT 11 2001 TC 2800 MAIL ROOM

Remarks

[x] The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 19-2380 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Luan C. Do, Reg. No. 38,434 Nixon Peabody LLP 8180 Greensboro Drive Suite 800 McLean, VA 22012
Signature	
Date	October 5, 2001

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date:

Type or printed name	
Signature	Date October 5, 2001

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

NVA199621.1

PTO/SB/17 (11-00)
Approved for use through 10/31/2002. OMB 0651-0032

FEE TRANSMITTAL FOR FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 110.00

Complete if Known	
Application Number	09/734,177
Filing Date	December 12, 2000
First Named Inventor	Yoshiharu HIRAKATA et al.
Examiner Name	D. Nguyen
Group Art Unit	2871
Attorney Docket No.	740756-2237

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 19-2380

Deposit Account Name: Nixon Peabody LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☒ **Payment Enclosed:**

☒ Check ☐ Credit Card ☐ Money Order ☐ Other

OIPE OCT 05 2001 PATENT & TRADEMARK OFFICE

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($)00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Independent Claims		-3** =		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

RECEIVED OCT 11 2001 TO 2800 MAIL ROOM

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge – late filing fee or oath	
127	50	227	25	Surcharge – late provisional filing fee or cover sheet	
139	130	139	130	Non-English transaction	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	200	200	Extension for reply within second month	
117	920	460	460	Extension for reply within third month	
118	1,440	720	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,280	241	640	Petition to revive – unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.29(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) Terminal Disclaimer $110.00

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)110.00

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on October 5, 2001.

Name:

SUBMITTED BY				Complete *(if applicable)*	
Name *(Print/Type)*	Luan C. Do	Registration No. *(Attorney/Agent)*	38,434	Telephone	703-790-9110
Signature				Date	October 5, 2001

NVA199620.1

Docket No. 0756-2237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
Yoshiharu HIRAKATA et al.) Art Unit: 2871
Serial No. 09/734,177) Examiner: D. Nguyen
Filed: December 12, 2000)
For: CONTACT STRUCTURE)

#7/B
Amdt
J. McMillan
10/15/01

AMENDMENT

Honorable Commissioner of Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated July 5, 2001 please consider the following amendments and remarks in connection with the above-identified application.

IN THE CLAIMS:

Please amend claims 4, 9, 14, 19, 24 and 29 as follows:

B1 4. (Amended) An active matrix display device according to claim 1, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second substrate.

B2 9. (Amended) An active matrix display device according to claim 6, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second substrate.

B3 14. (Amended) An active matrix display device according to claim 11, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second substrate.

B4 19. (Amended) An active matrix display device according to claim 16, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second substrate.

24. (Amended) An active matrix display device according to claim 21, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second substrate.

29. (Amended) An active matrix display device according to claim 26, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second substrate.

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application.

The Official Action mailed July 5, 2001 has been received and its contents carefully noted. Claims 1-30 are pending in the present application, of which claims 1, 6, 11, 16, 21, and 26 are independent.

Referring now to the Office Action, claims 4, 9, 14, 19, 24, and 29 are rejected under 35 U.S.C. § 112, second paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. More particularly, the Office is unclear how a fourth conductive film can be formed between a third conductive film and a second conductive film. In response, Applicants have amended claims 4, 9, 14, 19, 24, and 29, as shown above, to recite that the fourth conductive film is formed between the third conductive film and the second substrate.

Claims 1, 4-6, 9-11, 14-16, 19-21, 24-26, and 29-30 are rejected under 35 U.S.C. § 102(e) as allegedly anticipated by Lee et al. (U.S. Patent No. 6,219,124). In response, Applicants are in the process of preparing a verified full English translation of priority document of JP 9-094606 having a priority date of March 27, 1997, which predates the issue date of April 17, 2001 of Lee et al. As soon as the verified English translation is available, Applicants will forward the same to the Office.

Claims 1-30 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 12-22 of U.S. Patent No. 5,982,471 and claims 51-60 of U.S. Patent No. 6,177,974. In response, Applicants are submitting herewith a terminal disclaimer.

In view of the submission of the amendments, the terminal disclaimer, and the the pending submission of the verified English translation, as stated above, Applicants respectfully request reconsideration and withdrawal of the § 112, second paragraph, rejection, the § 102(e) rejection, and the double patenting rejections.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

Luan C. Do
Reg. No. 38,434

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
(703) 790-9110

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 4, 9, 14, 19, 24 and 29 as follows:

4. (Amended) An active matrix display device according to claim 1, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second [conductive film] substrate.

9. (Amended) An active matrix display device according to claim 6, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second [conductive film] substrate.

14. (Amended) An active matrix display device according to claim 11, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second [conductive film] substrate.

19. (Amended) An active matrix display device according to claim 16, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second [conductive film] substrate.

24. (Amended) An active matrix display device according to claim 21, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second [conductive film] substrate.

29. (Amended) An active matrix display device according to claim 26, wherein said active matrix display device further comprises a fourth conductive film between said third conductive film and said second [conductive film] substrate.

OShapple 10-18-01 8/Terminal Disclaimer

Docket No. 0756-2237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
Yoshiharu HIRAKATA et al.	)	
Serial No. 09/734,177	)	Art Unit: 2871
Filed: December 12, 2000	)	Examiner: D. Nguyen
For: CONTACT STRUCTURE	)	

TERMINAL DISCLAIMER

CERTIFICATE OF MAILING

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Honorable Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

I, Dr. Shunpei Yamazaki, having a place of business at Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, state that I am authorized to sign on behalf of the assignee of this invention and that the Assignment referred to below has been reviewed and certify that, to the best of my knowledge and belief, the entire right, title and interest in the above-identified application is in the name of Semiconductor Energy Laboratory Co., Ltd. by virtue of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 9256, Frame 0091.

Semiconductor Energy Laboratory Co., Ltd. hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 to 156 and 173, as presently shortened by any terminal disclaimer, of prior Patent Nos. 5,982,471 and 6,177,974.

10/09/2001 EABUBAK1 00000069 09734177
01 FC:148 110.00 OP

Docket No. 0756-2237

Semiconductor Energy Laboratory Co., Ltd. hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and prior Patent Nos. 5,982,471 and 6,177,974 are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, Semiconductor Energy Laboratory Co., Ltd. does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 to 156 and 173 of the prior patent, as presently shortened by any terminal disclaimer, in the event that it later expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 35 CFR 1.321, has all claims cancelled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

07/19/2001

Date

Shunpei Yamazaki

Name: Shunpei Yamazaki

Title: President

Company Name: Semiconductor Energy Laboratory Co., Ltd

TERMINAL DISCLAIMER APPROVED

OCT 18 2001

TECHNOLOGY CENTER 2800
SPECIAL PROGRAM CENTER

Sharon S. Hoppe

Sharon Hoppe
Supervisory Legal Instrumental Examiner
Technology Center 2800
Paralegal Specialist

2871

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/734,177
Filing Date	December 12, 2000
First Named Inventor	Yoshiharu HIRAKATA et al.
Group Art Unit	2871
Examiner Name	D. Nguyen
Total Number of Pages in This Submission	
Attorney Docket Number	740756-2237

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer (original w/ Cover)
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☒ Submission of Verified Translation

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Luan C. Do Nixon Peabody LLP 8180 Greensboro Drive Suite 800 McLean, VA 22102
Signature	
Date	October 11, 2001

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NVA200378.1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	) Group Art Unit: 2871
Yoshiharu HIRAKATA et al.	) Examiner: D. Nguyen
Serial No.: 09/734,177	)
Filed: December 12, 2000	)
For: CONTACT STRUCTURE	)

SUBMISSION OF VERIFIED TRANSLATION

Assistant Commissioner of Patent
Washington, D.C. 20231

October 11, 2001

Dear Sir:

Further to the Amendment filed on October 5, 2001, in order to perfect Applicants' claim for priority pursuant to 35 U.S.C. §119, submitted herewith is a verified translation of Japanese Patent Application No. 9-094606 filed March 27, 1997.

If the Examiner has any further questions concerning this matter, he is invited to contact the undersigned.

Respectfully submitted,

NIXON PEABODY LLP

Luan C. Do
Registration No. 38,434

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Telephone (703) 790-9110

EJR/LCD:sbs

NVA200366.1

Docket No.: 0756-2237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Divisional Application of :	)
Yoshiharu HIRAKATA et al	)
Application No.: 09/734,177	) Group Art Unit: 2871
Filed: December 12, 2000	) Examiner: D. Nguyen
For : CONTACT STRUCTURE	)

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Noriko Inage, 116-2, Kamiohi, Ohi-machi, Ashigarakami-gun, Kanagawa-ken 258-0016 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 9-094606 filed on March 27, 1997; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 9-094606 filed on March 27, 1997.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that theses statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 4th day of October, 2001

Noriko Inage

Name: Noriko Inage

[Name of Document]	Patent Application
[Reference Number]	P003585-02
[Filing Date]	March 27, 1997
[Attention]	Commissioner, Patent Office
[International Patent Classification]	H01L 21/00
[Title of Invention]	Contact Structure
[Number of Claims]	20
[Inventor]	
[Address]	398, Hase, Atsugi-shi, Kanagawa-ken c/o Semiconductor Energy Laboratory Co., Ltd.
[Name]	Yoshiharu HIRAKATA
[Inventor]	
[Address]	398, Hase, Atsugi-shi, Kanagawa-ken c/o Semiconductor Energy Laboratory Co., Ltd
[Name]	Shunpei YAMAZAKI
[Applicant]	
[Identification Number]	000153878
[Name]	Semiconductor Energy Laboratory Co., Ltd.
[Representative]	Shunpei YAMAZAKI
[Indication of Handlings]	
[Payment Method]	Prepayment
[Number of Prepayment Note]	002543
[Payment Amount]	21000
[List of Attachment]	
[Attachment]	Specification 1
[Attachment]	Drawing 1
[Attachment]	Abstract 1

[Name of Document] Specification

[Title of the Invention]

CONTACT STRUCTURE

[Scope of Claim]

[Claim 1]

A contact structure of an electro-optical device comprising:

a first conducting film formed over a first substrate;

a dielectric film covering at least a portion of said first conducting film;

a opening portion formed in the dielectric film to expose parts of the first conducting film by selectively leaving the dielectric film;

a second conducting film covering said dielectric film and said opening portion,

a third conducting film formed over said second substrate;

and a plurality of conducting spacers held between said first and second substrates and maintaining a gap between said first and second substrate;

wherein said opening portion,

said second conducting film, said conducting spacers and third conducting film are connected in turn on said second dielectric film, wherein said conducting spacers maintain a gap between said first and second substrates.

[Claim 2]

The contact structure of claim 1 wherein each of said openings occupies an area larger than an area occupied by each of said conducting spacers.

[Claim 3]

The contact structure of claim 1 or 2 wherein said dielectric film has a surface larger than an area occupied by each of said conducting spacers.

[Claim 4]

A contact structure of an electro-optical device comprising:

a first conducting film formed over a first substrate;

a first dielectric film covering at least a portion of said first conducting film;

having an opening portion to expose a portion of said first conducting film;

a opening portion formed in the dielectric film to expose parts of the first

conducting film by selectively leaving the dielectric film;

a second conducting film covering said opening portion;

a third conducting film formed over a second substrate;

and a plurality of conducting spacers held between said first and second substrates and maintaining a gap between first and second substrates;

wherein said opening portion, said first conducting film and said second conducting film are connected;

and wherein said insulator on the said opening portion, said conducting spacers and said third conducting film are connected in turn on said second dielectric film, wherein said conducting spacers maintain a gap between said first and second substrates.

[Claim 5]

The contact structure of claim 4 wherein said dielectric film and said insulator are substantially identical in thickness.

[Claim 6]

The contact structure of claim 4 or 5 wherein each of said parts of said opening portion has an area larger than an area occupied by each of said conducting spacers.

[Claim 7]

The contact structure of claim 4 or 6 wherein said insulator has a surface larger than an area occupied by each of said conducting spacers.

[Claim 8]

The contact structure of claim 1 or 7 further comprising a fourth conducting film placed between said second substrate and said third conducting film and being in contact with said third conducting film.

[Claim 9]

The contact structure of claim 8 wherein said second substrate and said third conducting film are transparent to light, and wherein said fourth conducting film has at least one opening.

[Claim 10]

A contact structure of an electro-optical device comprising:

a second substrate opposite to said first substrate;

a pixel electrode formed over said first substrate;

a counter electrode formed over said second substrate;

a first conducting film formed over said first substrate and under said pixel electrode;

a interlayer dielectric film covering at least a portion of said first conducting film and having at least one opening portion formed in the dielectric film to expose parts of said first conducting film by selectively leaving the dielectric film;

a third conducting film covering said interlayer dielectric film and said opening portion, said third conducting film and said pixel electrode comprising same material;

a plurality of conducting spacers held between said first and second substrates and maintaining a gap between said first and second substrates;

and wherein said first and second conducting films are contacted at said opening portion, wherein said dielectric film, said conducting spacers and said third conducting film are connected in turn on said second conducting film, wherein said conducting spacers maintain a gap between said first and second substrates.

[Claim 11]

The contact structure of claim 10 wherein said opening portion occupies an area larger than an area occupied by each of said conducting spacers.

[Claim 12]

The contact structure of claim 10 or 11 said interlayer dielectric film a surface larger than an area occupied by each of said conducting spacers.

[Claim 13]

A contact structure of an electro-optical device comprising:

a second substrate opposite to said first substrate;

a pixel electrode formed on said first substrate;

a counter electrode formed over said second substrate;

a first conducting film formed over said first substrate and under said pixel electrode;

a interlayer dielectric film covering at least a portion of said first conducting film and having an opening portion to expose a portion of said first conducting film,

and said opening portion formed in the dielectric film to expose parts of the

first conducting film by selectively leaving the dielectric film;

a second conducting film covering said first and second dielectric film and said opening portion, said second conducting films and said pixel electrode comprising same material;

a plurality of conducting spacers held between said first and second substrates and maintaining a gap between said first and second substrates;

wherein said first and second conducting films are contacted at said parts of said opening portion,

and wherein said insulator, said conducting spacers and said third conducting film are contacted at said parts of said second dielectric film, wherein said second conducting film, said conducting spacers and said counter electrode are connected in turn on said second dielectric film, wherein said conducting spacers maintain a gap between said first and second substrates.

[Claim 14]

The contact structure of claim 13 wherein said interlayer dielectric film and said insulator are substantially identical in thickness.

[Claim 15]

The contact structure of claim 13 or 14 wherein each of said parts of said opening portion has an area larger than an area occupied by each of said conducting spacers.

[Claim 16]

The contact structure of claim 13 or 15 wherein said insulator has a surface larger than an area occupied by each of said conducting spacers.

[Claim 17]

The contact structure of claim 13 or 16 further comprising a forth conducting film placed between said second substrate and said third conduction film and being in contact with said third conducting film.

[Claim 18]

The contact structure of claim 17 further comprising a black matrix, wherein said third conducting film and said black matrix comprise same material.

[Claim 19]

The contact structure of claim 17 or 18 wherein said second substrate and said third conducting film are transparent to light, and wherein said forth conducting film has at least one opening.

[Claim 20]

A contact structure of an electro-optical device comprising:

a first conducting film formed over a first substrate;

a dielectric film covering at least a portion of said first conducting film and having at least one opening portion to expose parts of said first conducting film;

a second conducting film covering said opening portion;

a third conducting film formed over a second substrate;

a fourth conducting film formed between said second substrate and said third conducting film and being in contact with said third conducting film;

and a plurality of conducting spacers held between said first and second substrates, wherein said conducting spacers maintain a gap between said first and second substrates;

wherein said opening portion, said second conducting film, said conducting spacers, said third conducting film and said forth conducting film are connected in turn on the first conducting film.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to a contact structure for electrically connecting together conducting lines formed on two opposite substrates, respectively, via conducting spacers and, more particularly, to a contact structure used in common contacts of an electro-optic device such as a liquid crystal display.

[0002]

[Prior Art]

In recent years, liquid crystal displays have been extensively used in the display portions of mobile intelligent terminals such as mobile computers and portable telephones including PHS (personal handyphone system). Also, active-matrix liquid crystal displays using TFTs as switching elements are well known.

[0003]

A liquid crystal display comprises two substrates and a liquid crystal material sealed between them. Electrodes are formed on these two substrates to set up electric fields. A desired image or pattern is displayed by controlling the magnitudes of these electric fields. In the active-matrix liquid crystal display, TFTs (thin-film transistors) are formed on one substrate to control the supply of voltage to each pixel electrode. Therefore, this substrate is referred to as the TFT substrate. A counter electrode placed opposite to the pixel electrodes is formed on the other substrate and so it is referred to as the counter substrate.

[0004]

In the active matrix display, an electric field is produced between each pixel electrode on the TFT substrate and the counter electrode on the counter substrate, thus providing a display. The potential at each pixel electrode on the TFT substrate is controlled by the TFT and thus is varied. On the other hand, the counter electrode on the counter substrate is clamped at a common potential. For this purpose, the counter electrode is connected with an extractor terminal via a common contact formed on the TFT substrate. This extractor terminal is connected with an external power supply. This connection structure clamps the counter electrode at the common potential.

[0005]

The structure of the common contact of the prior art active-matrix liquid crystal display is next described briefly by referring to FIGS. 12-14.

[0006]

FIG. 12 is a top plan view of a TFT substrate 10. This TFT substrate comprises a substrate 11 having a pixel region 12, a scanning line driver circuit 13, and a signal line driver circuit 14. In the pixel region 12, pixel electrodes and TFTs connected with the pixel electrodes are arranged in rows and columns. The scanning line driver circuit 13 controls the timing at which each TFT is turned on and off. The signal line driver circuit 14 supplies image data to the pixel electrodes. Furthermore, there are extractor terminals 15 to supply electric power and control signals from the outside. The substrate 11 makes connection with the counter electrode at common contact portions 16a-16d.

[0007]

FIG. 13 is a cross-sectional view of the pixel region 11 and a common contact portion 15. A TFT 17 and many other TFTs (not shown) are fabricated in the pixel region 12 on the substrate 10. An interlayer dielectric film 18 is deposited on the TFT 17. A pixel electrode 19 connected with the drain electrode of the TFT 17 is formed on the interlayer dielectric film 18.

[0008]

A precursor for the source and drain electrodes of the TFT 17 is patterned into internal conducting lines 21 at the common contact portion 16. The interlayer dielectric film 18 is provided with a rectangular opening. A conducting pad 22 is formed in this opening and connected with the internal conducting lines 21. The pixel electrode 19 and the conducting pad 22 are patterned from the same starting film.

[0009]

FIG. 14 is a top plan view of the known common contact portion 16. A region located inside the conducting pad 22 and indicated by the broken line corresponds to the opening formed in the interlayer dielectric film 18.

[0010]

As shown in FIG. 13, a counter electrode 24 consisting of a transparent conducting film is formed on the surface of a counter substrate 23. This counter electrode 24 is opposite to the pixel electrodes 19 in the pixel region 12 and to the conducting pad 22 at the common contact portion 16.

[0011]

Spherical insulating spacers 25 are located in the pixel region 12 to maintain the spacing between the substrates 11 and 23. A spherical conducting spacer 26 is positioned at the common contact portion 16 and electrically connects the counter electrode 24 with the conducting pad 22. The pad 22 is electrically connected with the internal conducting lines 21, which in turn are electrically connected with an extractor terminal 14. This connection structure connects the counter electrode 24 on the counter substrate 23 with the extractor terminal 14 on the substrate 10.

[0012]

[Problem to be Solved by the Invention]

In the prior art liquid crystal display, the interlayer dielectric film 18 is provided with the opening at the common contact portion 16, as shown in FIG. 13. Therefore, the cell gap Gc in the common contact portion is almost equal to the sum of the cell gap Gp in the pixel region + the film thickness t of the interlayer dielectric film 18.

[0013]

The cell gap Gp (also known as the cell spacing) in the pixel region 12 is determined by the insulating spacers 25. It is common practice to use standardized spacers as the insulating spacers 25 and so if the spacers 25 have a uniform diameter, the cell gap Gp in the pixel region 12 is substantially uniform among liquid-crystal cells. However, it is difficult to avoid nonuniformity of the cell gap Gc in the common contact portion among liquid-crystal cells.

[0014]

The cell gap Gc in the common contact portion is constant since the cell gap Gp is constant because of the relation described above. Therefore, the cell gap Gc in the common contact portion depends only on the film thickness t of the interlayer dielectric film 18. Consequently, to make the cell gap Gc uniform among liquid-crystal cells, it is necessary that the film thickness t of this interlayer dielectric film 18 be uniform among cells. However, this is impossible to circumvent.

[0015]

Normally, the common contact portions of the liquid crystal display are 2 to 4 in number. The film thickness t of the interlayer dielectric film 18 may differ from location to location on the same substrate. In this case, the film thickness t may differ among different common contacts even on the same substrate.

[0016]

Because of the aforementioned nonuniformity of the thickness t of the interlayer dielectric film 18, the cell gap Gc in the common contact portion differs among different cells or different common contacts. Furthermore, the nonuniformity of the cell gap Gc results in the cell gap Gp in the pixel region to be nonuniform.

[0017]

The cell gap Gp in the pixel region is affected more by the nonuniformity of

the cell gap Gc in the common contact portion as the area of the pixel region 12 becomes narrower than the area of the common contact portion. Especially, in the case of a projection display as used in a projector, the problem of above-described nonuniformity of the cell gap Gp in the pixel region becomes conspicuous, because it is a quite accurate small-sized display of about 1 to 2 inches.

[0018]

A standardized spacer is also used as the conducting spacer 26. The diameter of this conducting spacer 26 is determined by the diameter of the insulating spacers 25 in the pixel region 12 and by the design thickness of the interlayer dielectric film 18. Where the thickness of the interlayer dielectric film 18 is much larger than the designed value, the cell gap Gc in the common contact portion becomes very large. This makes it impossible to connect the counter electrode with the conducting pad well by the conducting spacer 26. In consequence, the counter electrode cannot be clamped at the common potential. As a result, a display cannot be provided.

[0019]

It is an object of the present invention to provide a contact structure which is free of the foregoing problems, provides less nonuniform cell gap among different cells if the thickness of the interlayer dielectric film is nonuniform across the cell or among different cells, and reduces poor electrical contacts which would normally be caused by conducting spacers.

[0020]

[Means for Solving the Problem]

This object is achieved in accordance with the teachings of the invention by a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film by selectively leaving the dielectric film; a second conducting film covering the dielectric film left and the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates

and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the dielectric film left. The conducting spacers maintain the cell gap between the first and second substrates.

[0021]

One embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film to expose parts of the first conducting film; an insulator deposited on only portions of the first conducting film exposed through the openings; a second conducting film covering the openings; a third conducting film formed on the second substrate; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings extending through the insulator. The second conducting film, the conducting spacers, and the third conducting film are connected in turn through the openings extending through the insulator. The conducting spacers maintain the cell gap between the first and second substrates.

[0022]

Another embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate of an electro-optical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereover, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film by selectively leaving the interlayer dielectric film; a second conducting film defining the counter electrode formed on the second substrate; a third

conducting film covering the interlayer dielectric film left and the openings; and conducting spacers held between the first and second substrates and connecting the second and third conducting films. The second conducting film is connected with the first conducting film through the openings. The third conducting film and the pixel electrodes are formed from a common starting film. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the dielectric film left. The conducting spacers maintain the spacing between the first and second substrates.

[0023]

A further embodiment of the invention resides in a contact structure for connecting a first conducting film formed over a first substrate of an electro-optical device with a counter electrode formed on a second substrate opposite to the first substrate, which has pixel electrodes formed thereon, the contact structure comprising: a cell gap defined between the first and second substrates; a first conducting film formed on the first substrate and under the pixel electrodes; an interlayer dielectric film covering the first conducting film; openings formed in the interlayer dielectric film to expose parts of the first conducting film; an insulator formed on selected portions of the surface of the first conducting film extending through the openings; a second conducting film covering the openings; a third conducting film defining the counter electrode formed on the second substrate; conducting spacers held between the first and second substrates and connecting the second and third conducting films. The pixel electrodes and the second conducting film are formed from a common starting film. The second conducting film is connected with the first conducting film through the openings extending through the insulator. The second conducting film, the conducting spacers, and the third conducting film are connected in turn on the insulator formed in the openings. The conducting spacers maintain the cell gap between the first and second substrates.

[0024]

A still other embodiment of the invention resides in a contact structure for connecting a conducting film formed on a first substrate with a conducting film formed on a second substrate opposite to the first substrate, the contact structure comprising: a

cell gap defined between the first and second substrates; a first conducting film formed on the first substrate; a dielectric film covering the first conducting film; openings formed in the dielectric film and exposing parts of the first conducting film; a second conducting film covering the openings; a third conducting film formed over the second substrate; a fourth conducting film formed between the second substrate and the third conducting film and in contact with the third conducting film; and conducting spacers held between the first and second substrates. The first conducting film, the second conducting film, the conducting spacers, the third conducting film, and the fourth conducting films are connected in turn through the openings. The spacers maintain the cell gap between the first and second substrates.

[0025]

[Embodiment Modes of the Invention]

The present embodiment of this invention is described by referring to FIGS. 1, 2A and 2B.

[0026]

[Embodiments of the Invention]

[Embodiment 1]

FIG. 1 is a fragmentary cross-sectional view of a common contact portion of a liquid crystal display in accordance with the present embodiment. FIGS. 2 are top plan views of the TFT substrate of the liquid crystal display. The structure of a region 120 shown in FIG. 2 is depicted in the enlarged cross section of FIG. 1.

[0027]

As shown in FIG. 13, in the prior art structure, the spacers in the pixel region 12 are located over the interlayer insulating film 18 via the pixel electrode 19. However, the interlayer dielectric film 18 does not exist under the conducting pad 22 at the common contact portion 16. Hence, the cell gap Gc in the common contact portion depends on the thickness of the interlayer dielectric film 18.

[0028]

Accordingly, in the present embodiment, an insulator, or a dielectric, is inserted under the conducting pad in the common contact portion. Conducting spacers are placed on top of the dielectric, so that the cell gap Gc in the contact portion does not depend on

the thickness of the interlayer dielectric film 18. In the present embodiment, openings are formed, selectively leaving the interlayer dielectric film 18.

[0029]

In the present embodiment, as shown in FIG. 1, a first conducting film 103 is formed on a first substrate 101. A dielectric film 104 is deposited on the first conducting film 103. The dielectric film 104 is selectively left to form openings 111 that expose parts of the first conducting film 103. A second conducting film 105 is formed so as to cover the left parts of the dielectric film, 104a, and the openings 111.

[0030]

A third conducting film 106 is formed on the second substrate 102. Conducting spacers 107 are sandwiched between the first substrate 101 and the second substrate 102.

[0031]

In the prior art opening 110 shown in FIG. 2A, the dielectric film 104 has been fully removed. In the present embodiment, the dielectric film 104 is selectively left to form the dielectric film portions 104a and the openings 111. The openings 111 expose parts of the first conducting film 103. The first conducting film 103 is connected with the second conducting film 105 at these openings 111.

[0032]

On the first substrate 101, the left dielectric film 104a is closest to the second substrate 102; therefore, on the left dielectric film 104a, the second conducting film 105 formed on the first substrate electrically connects with the third conducting film 106 formed on the second conducting film 102 through the conducting spacer 107, as shown in FIG. 1.

[0033]

In region 110, the left dielectric film 104a is closest to the second substrate; therefore, the conducting spacers 107 electrically connecting the second conducting film 105 with the third conducting film 106 maintain the gap G between the substrates. Consequently, this gap G is dependent only on the size of the conducting spacers 107. Therefore, where the conducting spacers 107 are uniform among liquid-crystal cells, the gap G can be made uniform among cells, even if the thickness t of the dielectric film

104 differs among cells.

[0034]

In the present embodiment, it is desired that the area of each opening 111 be sufficiently larger than the area occupied by each conducting spacer and offer space so that the conducting spacers can move freely, because the spacers 107 existing in the openings 111 do not contribute toward maintaining the gap. Otherwise, plural conducting spacers 107 would be stacked on top of each other, making it impossible to maintain the cell gap G uniform across the cell.

[0035]

Also in the present embodiment, it is desirable that the area of the surface of each left dielectric film portion 104a be sufficiently larger than the area occupied by each conducting spacer 107, assuring arrangement of the conducting spacers 107. If the spacers 107 are not positioned over the dielectric film 104a with certainty, it will not be possible to make electrical connections between the first and second substrates. Furthermore, the gap will not be maintained.

[0036]

The openings 111 are formed as shown in FIG. 2A in the present embodiment. The relation between the left dielectric film 104a and each opening 111 may be reversed as shown in FIG. 2B. It is that noted FIG. 1 is an enlarged view of the region 120 indicated by the broken line in FIG. 2B.

[0037]

[Embodiment 2]

The present embodiment is described by referring to FIGS. 1 and 2A. FIG. 1 is a cross-sectional view of a common contact portion of the liquid crystal display in accordance with the present embodiment. FIG. 2A is a top plan view of the TFT substrate of the liquid crystal display. FIG. 1 is an enlarged cross-sectional view of the region 120 indicated by the broken line in FIG. 2A.

[0038]

A dielectric is inserted under a conducting pad in the common contact portion, in the same manner as in Embodiment 1. Conducting spacers are positioned on the dielectric. Thus, the cell gap Gc in the common contact portion does not depend on

the thickness of the interlayer dielectric film 18. The present embodiment is characterized in that the dielectric film 18 is selectively left to form openings.

[0039]

In particular, in the present embodiment, the dielectric layer is formed underneath the conducting pad 22. The conducting spacers are positioned on the dielectric. Consequently, the cell gap Gc in the common contact portion is not dependent on the thickness of the interlayer dielectric film 18.

[0040]

Referring to FIG. 1, a first conducting film 103 is formed on top of a first substrate 101. A dielectric film 104 covers the first conducting film 103. The dielectric film 104 is provided with openings 110 to selectively expose the surface of the first conducting film 103. The exposed portions of the dielectric 104 are indicated by 104a. A second conducting film 105 is formed to cover the openings 110.

[0041]

A third conducting film 106 is formed on the second substrate 102. Conducting spacers 107 are located between the first substrate 101 and the second substrate 102.

[0042]

FIG. 2A is a top plan view of the TFT substrate, and in which the second conducting film 105 is not yet deposited. In FIG. 2A, the region 110 indicated by the broken line corresponds to the opening for the common contact formed in the interlayer dielectric film 18 of the prior art structure. A dielectric 104a is selectively deposited to leave portions of the first conducting film 103 to be exposed.

[0043]

The first conducting film 103 is exposed at locations where the dielectric 104a is not deposited. The exposed portions of the first conducting film 103 are connected with the overlying second conducting film 105.

[0044]

On the first substrate 101, the dielectric 104a is closest to the second substrate. As shown in FIG. 1, on the dielectric 104a, conducting spacers 107 electrically connect the second conducting film 105 on the first substrate 101 with the third conducting film 106 on the second substrate 102.

[0045]

The dielectric 104a is closest to the second substrate 102. Therefore, the conducting spacers 107 electrically connecting the second conducting film 105 with the third conducting film 106 hold the cell gap G. In consequence, the gap G is dependent only on the size of the conducting spacers 107. Where the spacers 107 are uniform in size, the cell gap G can be rendered uniform among liquid-crystal cells even if the thickness t of the dielectric film 104 differs among cells.

[0046]

In the present embodiment, the area of each portion not covered with the dielectric 104a is preferably sufficiently wider than the area occupied by one conducting spacer 107 and permits the conducting spacers 107 to move freely, because the spacers 107 existing in the regions where the dielectric 104a is not present do not contribute toward maintaining the gap. Otherwise, plural conducting spacers 107 would be stacked on top of each other, making it impossible to maintain the cell gap G uniform across the cell.

[0047]

Also in the present embodiment, it is desirable that the area of each portion of the dielectric film 104a be sufficiently larger than the area occupied by one conducting spacer 107 and that the conducting spacers 107 be arranged with certainty. If the spacers 107 are not positioned on the dielectric film 104a with certainty, it will not be possible to make electrical connections between the first and second substrates. Furthermore, the cell spacing will not be maintained.

[0048]

In this embodiment, the dielectric 104a is deposited as shown in FIG. 2A. The relation between the regions where the dielectric 104a is deposited and each region where the first conducting film 103 is exposed may be reversed as shown in FIG. 2B.

[0049]

[Examples]

[Example 1]

In this example, the present invention is applied to a common contact portion of a reflection-type liquid crystal display. FIG. 3 is a top plan view of the TFT

substrate of this liquid crystal display. FIG. 4 is a top plan view of the counter substrate of the liquid crystal display.

[0050]

Referring to FIG. 3, the TFT substrate 200 comprises a substrate 201 having a pixel region 202, a scanning line driver circuit 203, and a signal line driver circuit 204. Pixel electrodes and TFTs connected with the pixel electrodes are arranged in rows and columns in the pixel region 202. The scanning line driver circuit 203 controls the timing at which each TFT is turned on and off. The signal line driver circuit 204 supplies image data to the pixel electrodes. Extractor terminals 205 are also provided to supply electric power and control signals from the outside. Common contact portions 206a-206d form junctions with the counter electrode.

[0051]

As shown in FIG. 4, the counter substrate 250 comprises a substrate on which a counter electrode 252 consisting of a transparent conducting film is deposited. A central rectangular region 253 is opposite to the pixel region 202 of the TFT substrate 200. Four corner regions 254a-254d are electrically connected with the contact portions 206a-206d, respectively, of the TFT substrate 200.

[0052]

As shown in FIG. 3, conducting pads are formed in the common contact portions 206a-206d, respectively, of the TFT substrate 200. These conducting pads are electrically connected together by internal conducting lines 207a-207c. The internal lines 207a and 207b extend to the extractor terminals 205 and are electrically connected with common terminals 205a and 205b, respectively.

[0053]

A process sequence for manufacturing the pixel region 202 and the common contact portion 206a-206d on the TFT substrate is next described by referring to Figs. 5.

[0054]

First, the substrate 201 having an insulating surface was prepared. In the present example, a silicon oxide film was formed as a buffer film on the glass substrate. An active layer 302 consisting of a crystalline silicon film was formed over the substrate 201. Although only one TFT is shown, millions of TFTs are built in the pixel

region 202 in practice.

[0055]

In the present example, an amorphous silicon film was thermally crystallized to obtain the crystalline silicon film. This crystalline silicon film was patterned by an ordinary photolithographic step to obtain the active layer 302. In this example, a catalytic element such as nickel for promoting the crystallization was added during the crystallization. This technology is described in detail in Japanese Unexamined Patent Publication No. 7-130652.

[0056]

Then, a silicon oxide film 303 having a thickness of 150 nm was formed. An aluminum film (not shown) containing 0.2wt% by weight of scandium was deposited on the

silicon oxide film 303. The aluminum film was patterned, using a resist mask 304, into an island pattern 305 from which gate electrodes will be formed (Fig. 5A).

[0057]

The present example made use of the anodization technique described in Japanese Unexamined Patent Publication No. 7-135318. For further information, refer to this publication.

[0058]

First, the island pattern 305 was anodized within a 3% aqueous solution of oxalic acid while leaving the resist mask 304 on the island pattern 305, the mask 304 having been used for the patterning step. At this time, an electrical current of 2 to 3 mV was passed, using a platinum electrode as a cathode. The voltage was increased up to 8 V. Since the resist mask 304 was left on the top surface, porous anodic oxide film 306 was formed on the side surfaces of the island pattern 305 (Fig. 5B).

[0059]

After removing the resist mask 304, anodization was carried out within a solution prepared by neutralizing a 3% aqueous solution of tartaric acid with aqueous ammonia. At this time, the electrical current was set to 5 to 6 mV. The voltage was increased up to 100 V. In this way, a dense anodic oxide film 307 was formed.

[0060]

The above-described anodic oxidation step defined the unoxidized island pattern 305 into gate electrodes 308. Internal connecting lines 207c interconnecting the common contact portions 206c and 206d were created from the aluminum film described above simultaneously with the gate electrodes 308.

[0061]

Then, using the gate electrodes 308 and surrounding anodic oxide film 306, 307 as a mask, the silicon oxide film 303 was etched into a gate insulating film 309. This etching step relied on dry etching using CF_4 gas (Fig. 5C).

[0062]

After the formation of the gate insulating film 309, the porous anodic oxide film 307 was removed by wet etching using Al mixed acid.

[0063]

Thereafter, impurity ions for imparting one conductivity type were implanted by ion implantation or plasma doping. Where N-type TFTs are placed in the pixel region, P (phosphorus) ions may be implanted. Where P-type TFTs are placed, B (boron) ions may be implanted.

[0064]

In the present example, the above-described process for implanting the impurity ions was carried out twice by ion implantation. The first step was performed under a high accelerating voltage of 80 keV. The system was so adjusted that the peak of the impurity ions was brought under the ends (protruding portions) of the gate insulating film 309. The second step was effected under a low accelerating voltage of 5 keV. The accelerating voltage was adjusted so that the impurity ions were not implanted under the ends (protruding portions) of the gate insulating film 309.

[0065]

In this way, a source region 310, a drain region 311, lightly doped regions 312, 313, and a channel region 314 for the TFT were formed. The lightly doped region 313 on the side of the drain region 311 is also referred to as the LDD region (Fig. 5D).

[0066]

At this time, it is preferable to implant the impurity ions to such a dosage that the source and drain regions 310 and 311, respectively, exhibit a sheet resistance of 300

to 500 Ω／□. In addition, it is necessary to optimize the lightly doped regions 312 and 313 according to the performance of the TFT. After the impurity ion implantation step, a thermal treatment was carried out to activate the impurity ions.

[0067]

Then, a 1 μm-thick-silicon oxide film was formed as a first interlayer dielectric film 315. The thickness of the interlayer dielectric film 315 was set to 1 μm to flatten the surface of the first interlayer dielectric film 315 as much as possible. This could mitigate the protrusions due to the gate electrodes 308.

[0068]

The first interlayer dielectric film 315 may be made of silicon nitride or silicon oxynitride, as well as silicon oxide. Alternatively, the first interlayer dielectric film 315 may be a multilayer film of these materials.

[0069]

Contact holes for gaining access to the source and drain regions 310 and 311, respectively, were created in the first interlayer dielectric film 315. Contact holes for allowing access to the internal conducting lines 207c were formed in the common contact portions 206c and 206d. Then, a conducting film forming a precursor for source and drain electrodes 316 and 317, respectively, and for internal conducting lines 318 was deposited.

[0070]

In this example, the conducting film was created from a multilayer film of titanium (Ti), aluminum (Al), and titanium (Ti) by sputtering. Each of the titanium layers was 100 nm thick, while the aluminum layer was 300 nm thick. This multilayer film was patterned to form a source electrode 316, a drain electrode 317, and internal conducting lines 318 (Fig. 5E).

[0071]

The internal conducting lines 318 shown FIG. 5 correspond to the internal conducting lines 207a and 207b shown in FIG. 3. These conducting lines 207a and 207b were connected with internal conducting lines 207c at the common contact portions 206c and 206d. The internal conducting lines 207c and the gate electrode 308 were created by the same processing steps.

[0072]

Subsequently, an organic resinous film was formed as a second interlayer dielectric film 319 to a thickness of 1 to 2 μm. Polyimide, polyamide, polyimidamide, acrylic resin, or other material may be used as the material of the organic resinous film. The organic resinous material acts to planarize the surface of the second interlayer dielectric film 319. This is important to make the cell gap uniform. In the present example, polyimide was deposited as the second interlayer dielectric film 319 to a thickness of 1 μm.

[0073]

Then, contact holes 320 and 321 were formed in the second interlayer dielectric film 319 to have access to the drain electrode 317 and to the internal conducting lines 318, respectively. The contact holes 321 for the internal conducting lines 318 were formed in the openings 111 shown in Fig. 2A. That is, rectangular holes measuring 100 μm times 100 μm were arranged in 5 rows and 5 columns within the rectangular region 110 measuring 1.1 mm.times.1.1 mm. These holes were spaced 100 μm from each other. Moreover, contact holes for connecting the internal conducting lines 318 (207a and 207b) with the common terminals 205a and 205b at the extractor terminals 205 were formed.

[0074]

As described later, the size of each hole was set to 100 μm times.100 μm to set the diameter of the conducting spacers to 3.5 μm in this example. This provides sufficient space so that the conductive spacer located at this position can move. Hence, the conducting spacers are prevented from being stacked on top of each other.

[0075]

The area of the left portions of the interlayer dielectric film 319 in the common contact portions is large enough to permit the conducting spacers to move. This assures that the conducting spacers are arranged in these regions. Consequently, the conducting spacers positioned in these regions can maintain the cell gap and make electrical connections reliably.

[0076]

A thin metal film which would later be made into pixel electrodes 322 and a

conducting pad 323 were formed to a thickness of 100 to 400 nm. In the present example, the thin metal film was made of an aluminum film containing 1 wt % titanium and deposited to a thickness of 300 nm by sputtering. Then, the thin metal film was patterned to form the pixel electrodes 322 and the conducting pad 323. This pad 323 measured 1.1 mm.times.1.1 mm, was rectangular, and covered the contact holes 321. The extractor terminals 205 were also patterned. Thus, the TFT substrate was completed (Fig. 5G).

[0077]

Referring to Fig. 6, the counter substrate 250 comprised a transparent plate 251 on which the counter electrode 252 was formed from an ITO film. A glass or quartz substrate can be used as the substrate 251.

[0078]

Then, the TFT substrate 200 and the counter substrate 250 were bonded together. This bonding step may be a well-known cell assembly method.

[0079]

First, a sealing material was applied to one of the TFT substrate 200 and the counter substrate 250. In this example, the sealing material was applied to the counter substrate 250. A UV-curable and thermosetting resin was used as the sealing material. This sealing material was applied around the substrate along straight lines except for the liquid crystal injection port by a sealant dispenser. A sealing material to which 3.0 wt % spherical conducting spacers 401 were added was applied to regions 254a-254d shown in Fig. 4. The sealing material to which the conducting spacers were added functioned as an anisotropic conducting film.

[0080]

Generally, the conducting spacers 401 consist of resinous spheres coated with a conducting film. In the present example, the conducting spacers 401 were coated with gold (Au). The diameter of the conducting spacers 401 may be larger than the cell gap by about 0.2 to 1 μm. In this example, the conducting spacers 401 had a diameter of 3.5 μm to set the cell gap to 3 μm. After applying the sealing material, it was temporarily baked.

[0081]

Thereafter, spacers 402 were dispersed onto one of the TFT substrate 200 and the counter substrate 250 to maintain the cell gap. In this example, the spacers 402 were applied to the counter substrate 250. To set the cell gap to 3 μm, spherical spacers of a polymeric material were used as the spacers 402.

[0082]

Then, the TFT substrate 200 and the counter substrate 250 were held opposite to each other, and they were pressed against each other until the cell gap in the pixel region was decreased to the diameter of the spacers 402. Under the pressed state, UV light was directed at this assembly for more than 10 seconds to cure the sealing material. The cell gap was fixed. Then, the assembly was heated under pressure, thus enhancing the adhesive strength.

[0083]

Subsequently, a liquid crystal material was injected, and the entrance hole was sealed off, thus completing the cell assembly process. As shown in Fig. 6, the counter electrode 252 on the counter substrate 250 was electrically connected with the conducting pad 323 on the TFT substrate 200 by the conducting spacer 401. On the TFT substrate, the conducting pad 323 connected the internal conducting lines 318 with the common terminals. This connection structure permitted the counter electrode 252 on the counter substrate 250 to be connected with an external power supply via the conducting lines on the TFT substrate. FIG. 1 is an enlarged view of the common contact portion of FIG. 6.

[0084]

In the present example, to set the cell gap to 3 μm, the spacers 402 applied to the pixel region had a diameter of 3 μm. The diameter of the conducting spacers 401 was 3.5 μm. Setting the diameter of the conducting spacers greater than the diameter of the spacers 402 (i.e., the cell gap) made reliable the connection between the counter electrode 252 and the conducting pad 318. When the two plates were being clamped together to bond them together, the conducting spacers 401 were crushed because they were larger in diameter than the cell gap. This increased the areas of the portions in contact with the counter electrode 252 and with the conducting pad 318, respectively. Hence, the electrical connection was rendered more reliable. Furthermore, the cell gap

could be maintained at the same dimension as in the pixel region.

[0085]

In this example, the internal conducting lines 318 were made of the precursor for the source and drain electrodes 316 and 317, respectively. It is only necessary for the internal conducting lines 318 to be under the pixel electrodes 322. For instance, where a black matrix consisting of a conducting film of titanium or the like is formed inside the second interlayer dielectric film 315, the internal conducting lines 318 can be formed from this conducting film.

[0086]

In the present example, it is important to flatten the surface of the second interlayer dielectric film 319 on which the pixel electrodes 322 are formed in order to make uniform the cell gap. Also, the flatness of the surface of the first interlayer dielectric film 315 where the internal conducting lines 318 are formed is important.

[0087]

Methods of obtaining an interlayer dielectric film having a flat surface include a method of increasing the thickness of the interlayer dielectric film, a leveling method using an organic resinous film, a mechanical polishing method, and etch-back techniques. The present example made use of the method of increasing the film thickness to planarize the first interlayer dielectric film 315. Also, the method of relying on leveling using an organic resinous film was used to flatten the first interlayer dielectric film 315. Other methods may also be employed for the same purpose.

[0088]

In a liquid crystal display in accordance with the present example, a dichroic dye may be dispersed in the liquid crystal layer. Orientation films may be deposited on the TFT substrate and on the counter substrate. Color filters may be formed on the counter substrate. The practitioner may appropriately determine the kind of the liquid crystal layer, the presence or absence of the orientation films and the color filters according to the driving method, the kind of the liquid crystal, and other factors.

[0089]

For instance, where the color filters are mounted on the counter substrate 250, the color filters are not formed at the common contact portions and so steps are formed

between the pixel region and the common contact portions on the counter substrate. To compensate for these steps, it is necessary to make the diameter of the conducting spacers larger by an amount almost equal to the thickness of the color filter.

[0090]

In the present example, the liquid crystal display is of the reflection type. A transmissive liquid crystal display may also be fabricated. In this case, the precursor for the pixel electrode and for the conducting pad may be made of a transparent ITO film or the like.

[0091]

In the example described above, the transistor is a coplanar TFT that is a typical top-gate TFT. It may also be a bottom-gate TFT. In addition, thin-film diodes, metal-insulator-metal (MIM) devices, metal-oxide varistors, and other devices can be used, as well as the TFTs.

[0092]

[Example 2]

The present example is a modification of the common contact portions of Example 1. Fig. 7 is a fragmentary cross-sectional view of an active-matrix display in accordance with the present example. The configuration of a TFT substrate shown in Fig. 7 is the same as the configuration shown in Fig. 6, and some reference numerals are omitted. Like components are indicated by like reference numerals in both Figs. 6 and 7. FIG. 9 is an enlarged view of the common contact portion shown in Fig. 7.

[0093]

In Example 1 shown in Fig. 6, the counter electrode 252 consists of an ITO film that is a transparent conducting film. Therefore, the counter electrode 252 and the conducting spacers 401 are larger in electrical resistance than metal films. The present example is intended to reduce this electrical resistance.

[0094]

Accordingly, the resistance value between the counter electrode 252 and the conducting spacers 401 can be lowered by forming a metallization layer on the counter substrate 250 and patterning the metallization layer into conducting pads, or conducting film, 501 at the common contact portions 254a to 254d. Importantly, the conducting

film forming the conducting pads 501 is lower in electrical resistance than the conducting film forming the counter electrode 252.

[0095]

Where the black matrix on the counter substrate is formed from a conducting film as consisting of chromium, the connecting pads 501 can be formed from this conducting film. When the conducting film is patterned to form the black matrix, the connecting pad 501 may be created.

[0096]

[Example 3]

The present example is a modification of Example 2. FIG. 8 is a fragmentary cross-sectional view of an active-matrix display in accordance with the present example. The TFT substrate shown in Fig. 8 is identical in structure with that shown in Fig. 6, and some reference numerals are omitted in Fig. 8. It is noted like components are denoted by like reference numerals in both Figs. 6 and 8. Fig. 10 is an enlarged view of the common contact portion of Fig. 8.

[0097]

In Example 1, both counter substrate 251 and counter electrode 252 are transparent to light and so the distribution of the conducting spacers 401 on the common contact portions can be visually observed from the side of the counter substrate 250 after both substrates have been bonded together. In Example 2, however, the connecting pad 501 consisting of metallization layer is formed and, therefore, the distribution of the conducting spacers 401 cannot be visually checked.

[0098]

The present example is intended to permit one to visually observe the distribution of the conducting spacers 401 while a connecting pad is provided to lower the resistance value. For this purpose, the connecting pad, 601, is provided with openings formed at selected locations. One can observe the conducting spacers 401 through these openings.

[0099]

FIG. 11 is a top plan view of the contact portions according to the present example, taken from the side of the counter substrate. Fig. 10 is a cross-sectional view

of the common contact portion in a region 600 surrounded by the broken line. As shown in Fig. 11, the conducting pad 601 is formed with openings 602. In each opening 602, there exist only the counter substrate 251 and the counter electrode 252, both of which have transparency. Hence, the distribution of the conducting spacers 401 can be observed through the openings 602.

[0100]

To maintain the cell gap, the openings 602 should be formed opposite to the contact holes 321 formed in the second interlayer dielectric film of the TFT substrate. At these locations, the conducting spacers 401 are not in contact with the counter electrode. The area of each opening 602 should be slightly larger than the area of each contact holes 321 formed in the second interlayer dielectric film, i.e., about several to thirty percent greater. The number of the openings 602, their arrangement, and their shape are not limited to the example of Fig. 11. Rather, one can arbitrarily set these geometrical factors.

[0101]

Setting each opening 602 in the connecting pad 601 slightly larger than each contact holes makes it possible to visually check the conducting pad 602 on the second interlayer dielectric film 319, which contributes to electrical connection.

[0102]

In Examples 2 and 3, the cell gap in the common contact portions is made uniform. At the same time, the contact resistances of the conducting spacers 401 and of the counter electrode 252 are decreased. If the main purpose is to lower these resistance values, the common contact portions on the TFT substrate may have the prior art structure as shown in Fig. 13. In this case, any of the connecting pads 501 and 601 described in Examples 2 and 3, respectively, may be formed between the substrate 23 and the counter electrode 24 at the common contact portions 16 shown in Fig. 13.

[0103]

In Examples 1-3 described above, the present invention is applied to active-matrix liquid crystal displays. The contact structure in accordance with the present invention is applicable to any apparatus having a contact structure for electrically connecting conductors formed on one substrate with conducting conductors

formed on the other opposite substrate via conducting spacers. For example, the novel contact structure can connect ICs built on different silicon wafers.

[0104]

[Effect of the Invention]

The common contact structure in accordance with the present invention can eliminate variations of the cell gap among liquid-crystal cells even if the film thickness varies among interlayer dielectric films. Also, poor contacts due to conducting spacers can be reduced.

[0105]

In particular, in accordance with the present invention, the cell gap depends only on the size of conducting spacers. Therefore, where the conducting spacers are uniform in size, the cell gap between opposite substrates or plates can be made uniform among different liquid-crystal cells, if the thickness of a dielectric film electrically insulating the first and second conducting films is different among different liquid-crystal cells.

[Brief Description of the Drawings]

[Fig. 1] A fragmentary cross-sectional view of a common contact portion in accordance with the present invention.

[Fig. 2] Top plan views of the common contact portion in accordance with the present invention.

[Fig. 3] A top plan view of the TFT substrate of a liquid crystal display in accordance with Example 1 of the invention.

[Fig. 4] A top plan view of the counter substrate of the liquid crystal display in accordance with Example 1.

[Fig. 5] A drawing illustrating a process sequence for fabricating the TFT substrate in accordance with Example 1.

[Fig. 6] A fragmentary cross-sectional view of a pixel region and a common contact portion of the liquid crystal display in accordance with Example 1.

[Fig. 7] A fragmentary cross-sectional view of a pixel region and a common contact portion of the liquid crystal display in accordance with Example 2.

[Fig. 8] A fragmentary cross-sectional view of a pixel region and a common contact

portion of the liquid crystal display in accordance with Example 3.

[Fig. 9] An enlarged cross-sectional view of the common contact portion in accordance with Example 2.

[Fig. 10] An enlarged cross-sectional view of the common contact portion in accordance with Example 3.

[Fig. 11] A top plan view of the common contact portion in accordance with Example 3.

[Fig. 12] A top plan view of the TFT substrate of the prior art liquid crystal display.

[Fig. 13] A cross-sectional view of a pixel region and a common contact portion on the TFT substrate.

[Fig. 14] A top plan view of the common contact portion of prior art.

[Description of Reference Numerals]

101 first substrate
102 second substrate
103 first conducting film
104 dielectric film
105 second conducting film
106 third conducting film
107 conducting spacers
200 TFT substrate
205 extractor terminal
206 common contact portion
207 internal conducting line
250 counter substrate
252 counter electrode
315 first interlayer dielectric film
318 internal conducting line
319 second interlayer dielectric film
322 pixel electrode
323 conducting pad
401 conducting spacers

402 spacers

501, 601 connecting pad

[Document Name] Abstract

[Summary]

[Problem]

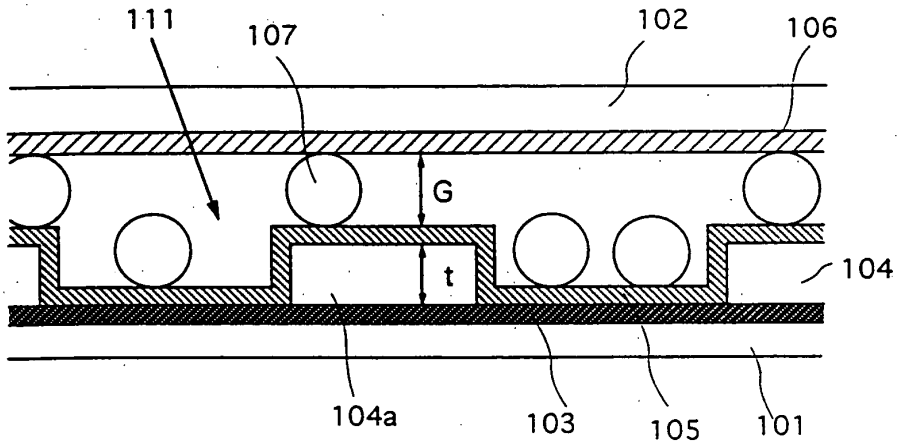
A common contact structure in accordance with the present invention can eliminate variations of the cell gap among liquid-crystal cells even if the film thickness varies among interlayer dielectric films. Also, poor contacts due to conducting spacers can be reduced.

[Solving Means]

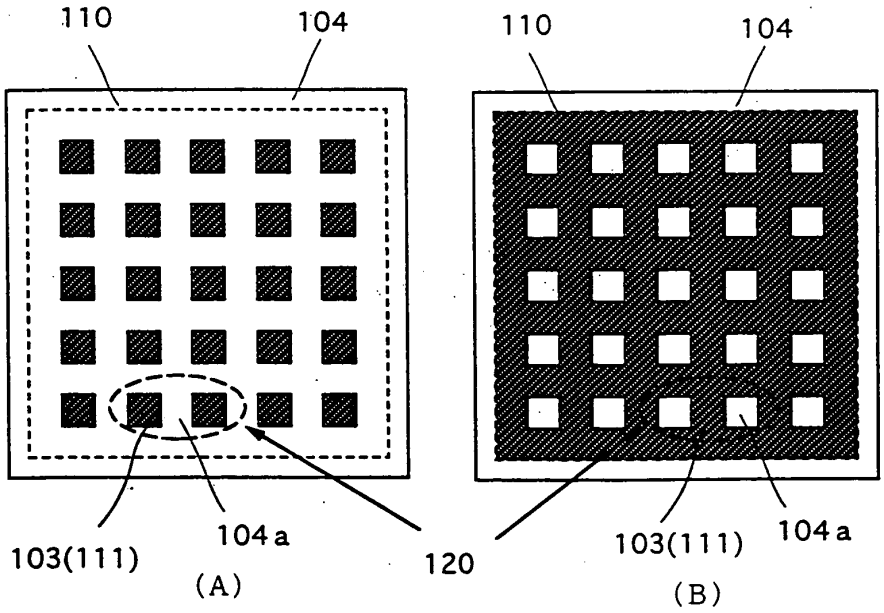
A first conducting film 103, a dielectric film 104, a opening portion 111 formed on the conducting film 104, leaving dielectric film 104a and a second dielectric film 105 covering the opening portion 111 are formed on top of a first substrate 101. The conducting spacers 107 electrically connecting the second conducting film 105 with the third conducting film 106 hold the cell gap G. In consequence, the gap G is dependent only on the size of the conducting spacers 107. Where the spacers 107 are uniform in size, the cell gap G can be rendered uniform among liquid-crystal cells even if the thickness t of the dielectric film 104 differs among cells.

[Selected Drawing] Fig. 1

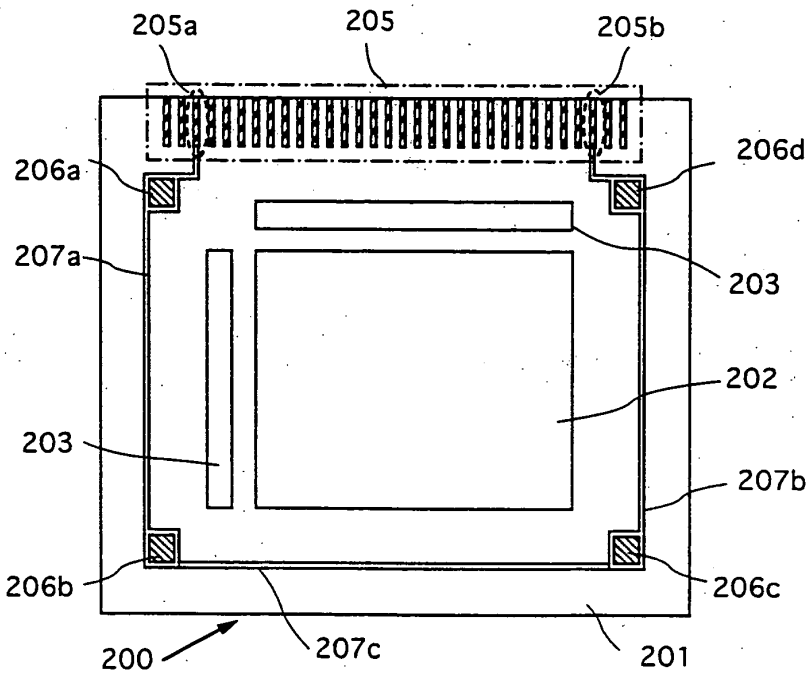
[Reference Number] P003585-02
[Document Name] Drawing
[Fig. 1]



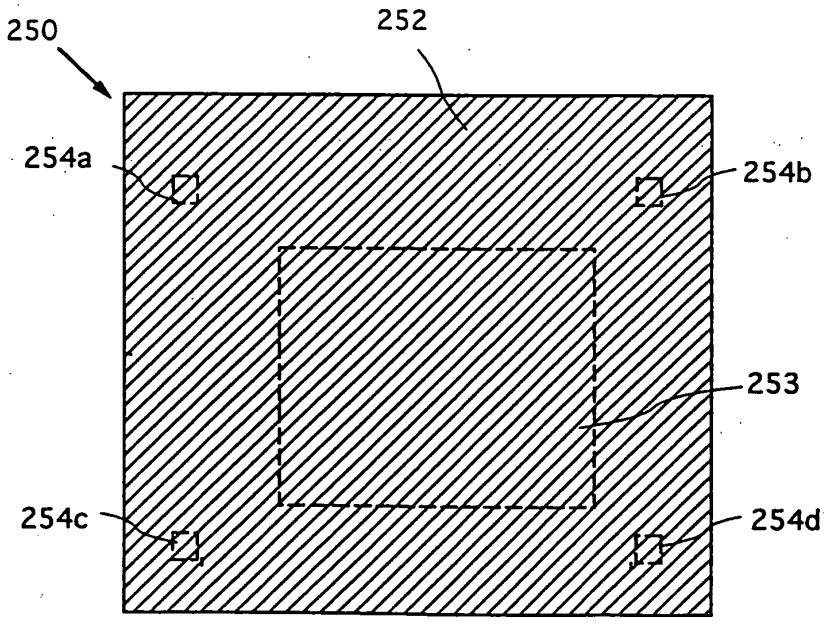
[Fig. 2]



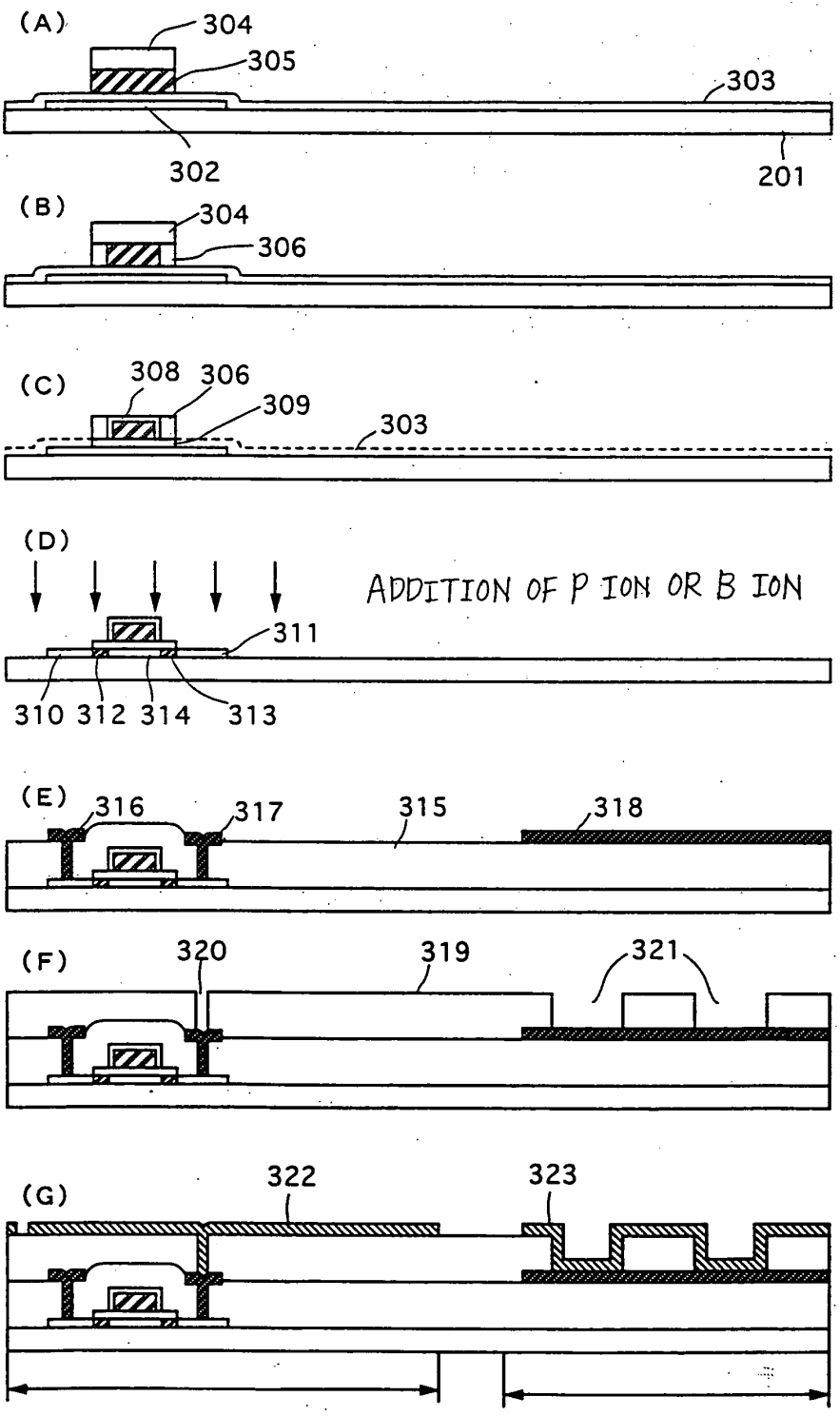
[Fig. 3]


205a
205
205b
206a
206d
207a
203
202
203
207b
206b
206c
200
207c
201

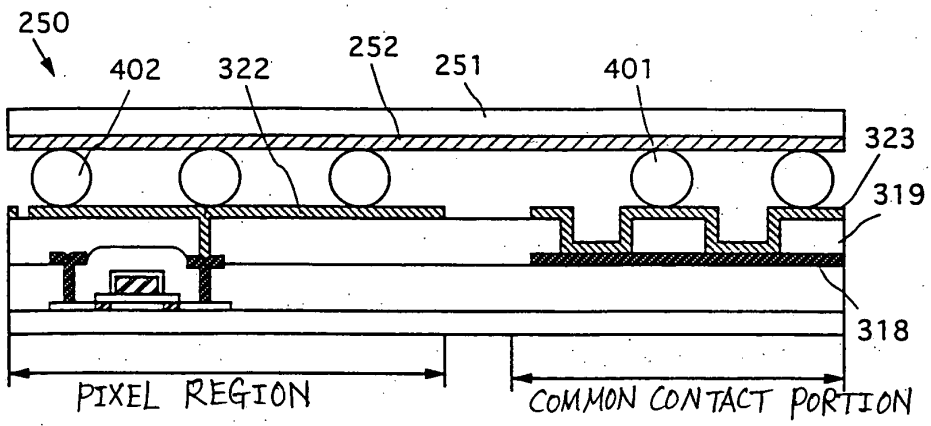
[Fig. 4]


250
252
254a
254b
253
254c
254d

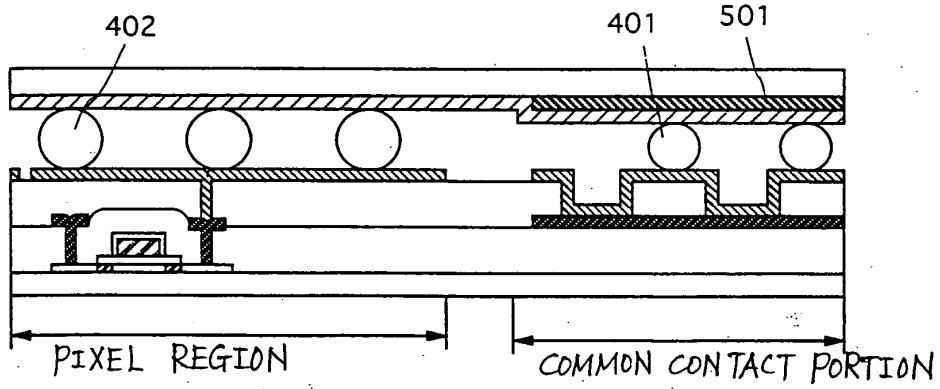
[Fig. 5]


(A)
304
305
303
302
201
(B)
304
306
(C)
308
306
309
303
(D)
ADDITION OF P ION OR B ION
311
310
312
314
313
(E)
316
317
315
318
(F)
320
319
321
(G)
322
323

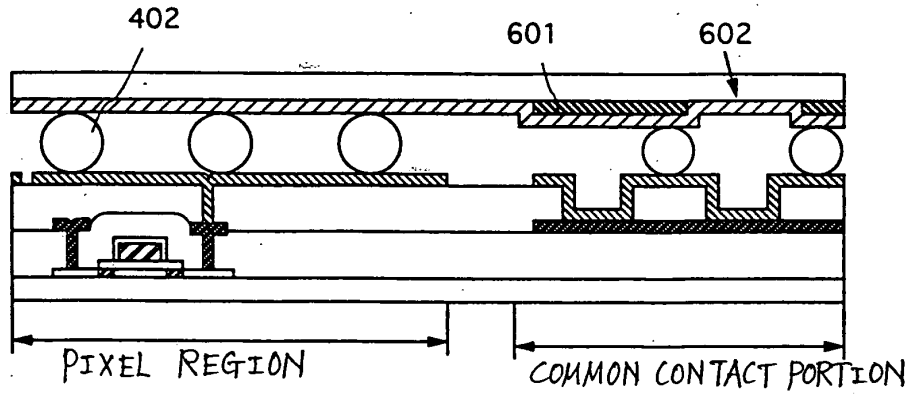
[Fig. 6]



[Fig. 7]

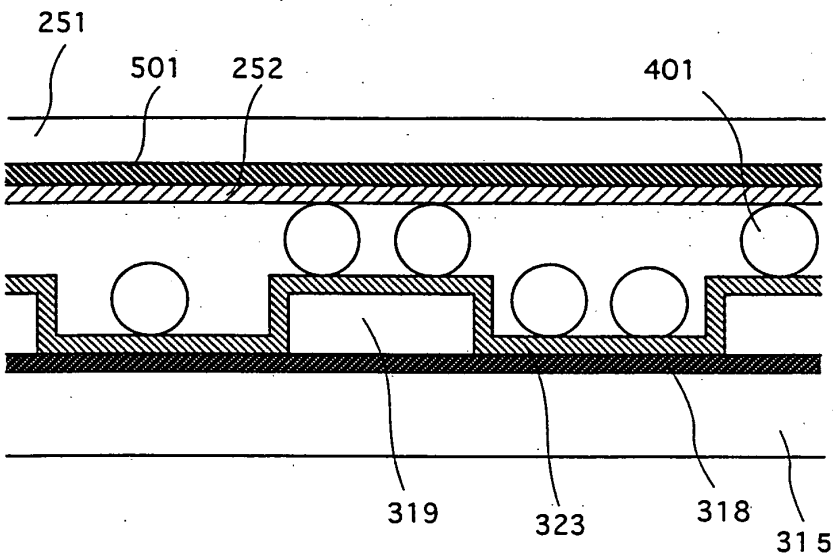


[Fig. 8]

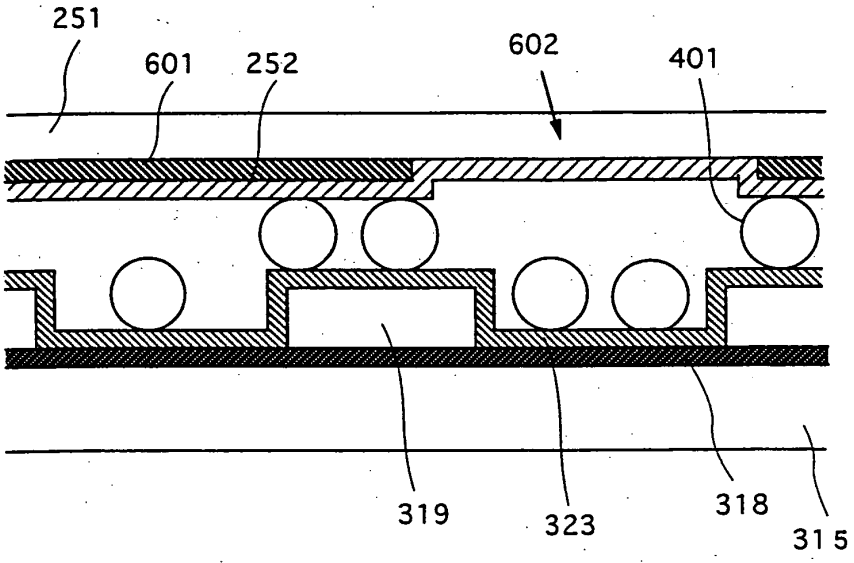


[Reference Number] 003858-02

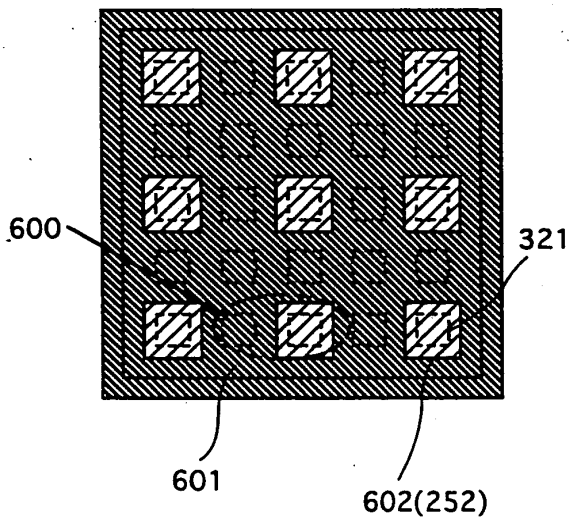
[Fig. 9]



[Fig. 10]

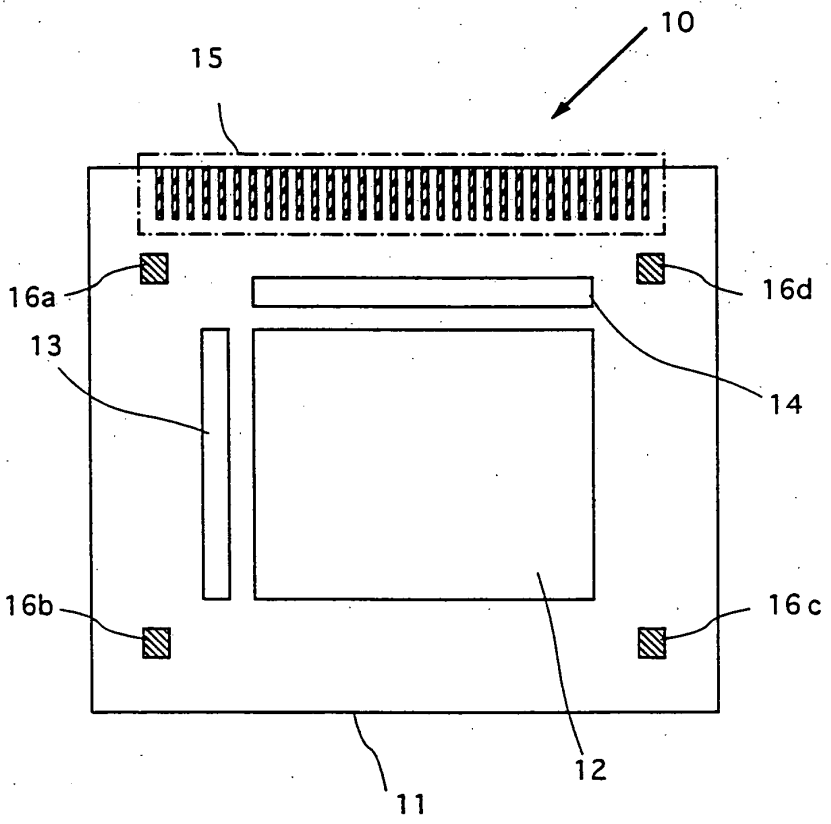


[Fig. 11]

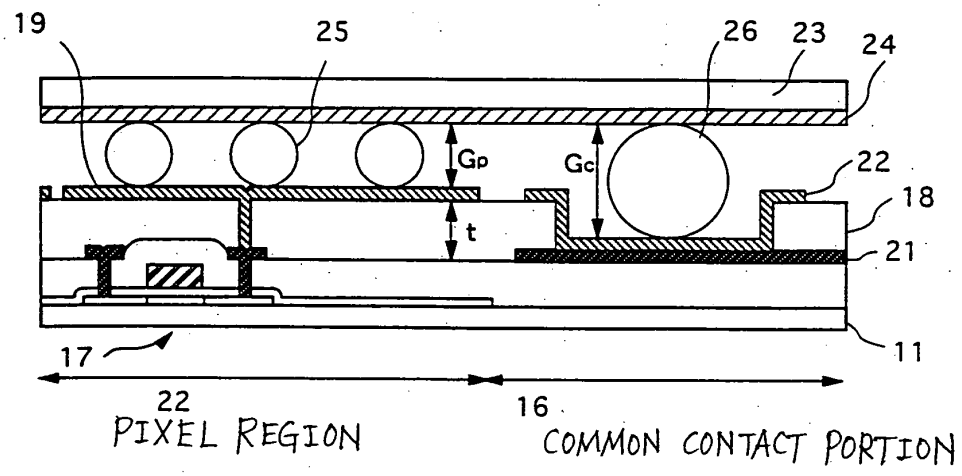


[Reference Number] 003585-02

[Fig. 12]



[Fig. 13]


19
25
26
23
24
Gp
Gc
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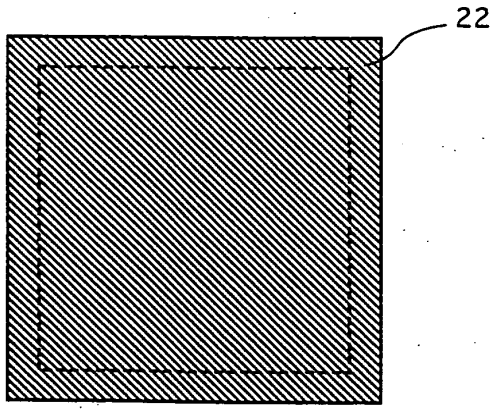
16
PIXEL REGION
COMMON CONTACT PORTION

[Fig. 14]


22

Nixon Peabody LLP
Attorneys at Law

8180 Greensboro Drive
Suite 800
McLean, Virginia 22102-3823
(703) 790-9110

Fax: (703) 883-0370

FAX

#19/Translation

Date: December 6, 2001 **Pages (including cover):** 45

To: Examiner Dung Nguyen **Fax:** 703-746-7730 **Ph:** 703-305-0423

From: Luan Do

Message: Dear Examiner Nguyen:

Pursuant to our telephone conversation this morning, attached herewith is a copy of the verified English Translation of Japanese Application No. 9-0946606 that you requested. Please note that the verified English Translation was submitted on October 11, 2001, and we have received a stamped post card with the same date from the PTO.

If we could be of further assistance in this matter, please let us know.

Regards,

Luan C. Do

Reg. No. 38,434

Date: December 6, 2001 **Pages (including cover):** 45

To: Examiner Dung Nguyen **Fax:** 703-746-7730 **Ph:** 703-305-0423

From: Luan Do

Client/Matter: 740756-002237 **User No.:** **Disbursement Amount:** S

NVA207289.1

Received from < 703+883+0370 > at 12/6/01 11:15:47 AM [Eastern Standard Time]

This will acknowledge receipt in re filing of:

1. Submission of Verified Translation with Transmittal

J.C.D

In re U.S.Patent Application of:

Inventor(s): Yoshiharu HIRAKATA et al.
Serial No.: 09/734,177
Filed: December 12, 2000
Due date: October 16, 2001
Title: CONTACT STRUCTURE

DOCKET No. 740756-2237
October 11, 2001
EJR/LCD/sbs

*****PLEASE DATE STAMP AND RETURN*****

NVA200376.1

OCT 12 2001

CRDS 10/15/01

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/734,177
Filing Date	December 12, 2000
First Named Inventor	Yoshiharu HIRAKATA et al.
Group Art Unit	2871
Examiner Name	D. Nguyen
Total Number of Pages in This Submission	
Attorney Docket Number	740756-2237

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Changes of Correspondence Address
- ☐ Terminal Disclaimer (original w/ Cover)
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☒ Submission of Verified Translation

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Luan C. Do Nixon Peabody LLP 8180 Greensboro Drive Suite 800 McLean, VA 22102
Signature	
Date	October 11, 2001

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date:

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Signature	Date

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NVA200378.1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	) Group Art Unit: 2871
Yoshiharu HIRAKATA et al.	) Examiner: D. Nguyen
Serial No.: 09/734,177	)
Filed: December 12, 2000	)
For: CONTACT STRUCTURE	)

SUBMISSION OF VERIFIED TRANSLATION

Assistant Commissioner of Patent
Washington, D.C. 20231

October 11, 2001

Dear Sir:

Further to the Amendment filed on October 5, 2001, in order to perfect Applicants' claim for priority pursuant to 35 U.S.C. §119, submitted herewith is a verified translation of Japanese Patent Application No. 9-094606 filed March 27, 1997.

If the Examiner has any further questions concerning this matter, he is invited to contact the undersigned.

Respectfully submitted,

NIXON PEABODY LLP

Luan C. Do
Registration No. 38,434

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, Virginia 22102
Telephone (703) 790-9110

EJR/LCD:sbs

NVA200366.1

Docket No.: 0756-2237

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Divisional Application of :	)
Yoshiharu HIRAKATA et al	)
Application No.: 09/734,177	) Group Art Unit: 2871
Filed: December 12, 2000	) Examiner: D. Nguyen
For : CONTACT STRUCTURE	)

VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Noriko Inage, 116-2, Kamiohi, Ohi-machi, Ashigarakami-gun, Kanagawa-ken 258-0016 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 9-094606 filed on March 27, 1997; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 9-094606 filed on March 27, 1997.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that theses statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 4th day of October, 2001

/Noriko Inage/

Name: Noriko Inage

[Name of Document]	Patent Application
[Reference Number]	P003585-02
[Filing Date]	March 27, 1997
[Attention]	Commissioner, Patent Office
[International Patent Classification]	H01L 21/00
[Title of Invention]	Contact Structure
[Number of Claims]	20
[Inventor]	
[Address]	398, Hase, Atsugi-shi, Kanagawa-ken c/o Semiconductor Energy Laboratory Co., Ltd.
[Name]	Yoshiharu HIRAKATA
[Inventor]	
[Address]	398, Hase, Atsugi-shi, Kanagawa-ken c/o Semiconductor Energy Laboratory Co., Ltd
[Name]	Shunpei YAMAZAKI
[Applicant]	
[Identification Number]	000153878
[Name]	Semiconductor Energy Laboratory Co., Ltd.
[Representative]	Shunpei YAMAZAKI
[Indication of Handlings]	
[Payment Method]	Prepayment
[Number of Prepayment Note]	002543
[Payment Amount]	21000
[List of Attachment]	
[Attachment]	Specification 1
[Attachment]	Drawing 1
[Attachment]	Abstract 1

[Name of Document] Specification

[Title of the Invention]

CONTACT STRUCTURE

[Scope of Claim]

[Claim 1]

A contact structure of an electro-optical device comprising:

a first conducting film formed over a first substrate;

a dielectric film covering at least a portion of said first conducting film;

a opening portion formed in the dielectric film to expose parts of the first conducting film by selectively leaving the dielectric film;

a second conducting film covering said dielectric film and said opening portion,

a third conducting film formed over said second substrate;

and a plurality of conducting spacers held between said first and second substrates and maintaining a gap between said first and second substrate;

wherein said opening portion,

said second conducting film, said conducting spacers and third conducting film are connected in turn on said second dielectric film, wherein said conducting spacers maintain a gap between said first and second substrates.

[Claim 2]

The contact structure of claim 1 wherein each of said openings occupies an area larger than an area occupied by each of said conducting spacers.

[Claim 3]

The contact structure of claim 1 or 2 wherein said dielectric film has a surface larger than an area occupied by each of said conducting spacers.

[Claim 4]

A contact structure of an electro-optical device comprising:

a first conducting film formed over a first substrate;

a first dielectric film covering at least a portion of said first conducting film;

having an opening portion to expose a portion of said first conducting film;

a opening portion formed in the dielectric film to expose parts of the first