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**Estakhri et al.**

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- (54) **PRECISION CLOCK SYNTHESIZER USING RC OSCILLATOR AND CALIBRATION CIRCUIT**
- (75) Inventors: **Petro Estakhri**, Pleasanton; **Mahmud Assar**, Morgan Hill; **Parviz Keshtbod**, Los Altos Hills, all of CA (US)
- (73) Assignee: **Lexa Media, Inc.**, Fremont, CA (US)
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- (58) **Field of Search** ..... **327/147, 148, 327/151, 155, 156, 157, 160, 162, 163; 331/1 R, 11, 3-111; 375/226, 294, 374, 375; 324/521, 617, 622**

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*Primary Examiner*—Terry D. Cunningham  
*Assistant Examiner*—Linh Nguyen  
(74) *Attorney, Agent, or Firm*—Haverstock & Owens LLP

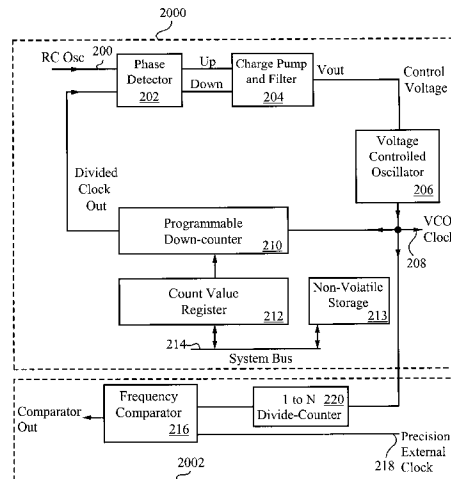
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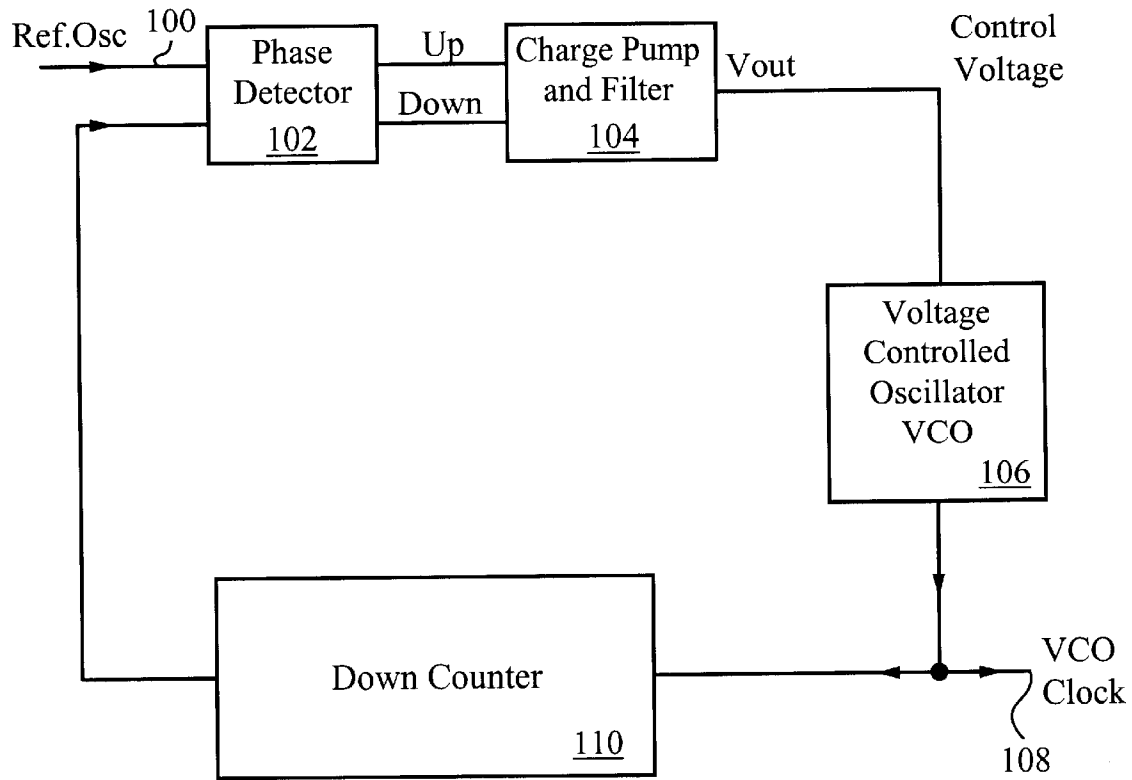
(57) **ABSTRACT**

A system and method of generating an output signal of very precise frequency without the use of a crystal oscillator. An input signal is generated using any convenient such as an RC oscillator. A circuit for producing a frequency-controlled output signal comprises a phase lock loop having a VCO and a down counter. The down counter reduces the frequency of a VCO clock signal in accordance with a down count value. The down count value is loaded in a register and stored in non-volatile memory. The down count value is set during a calibration operation using a precision external clock signal. In this way, a clock signal with a highly precise frequency is generated without using a crystal oscillator.

**11 Claims, 3 Drawing Sheets**



**SCHRADER**  
**EXH. 1004**



Typical Clock Synthesizer

Fig. 1

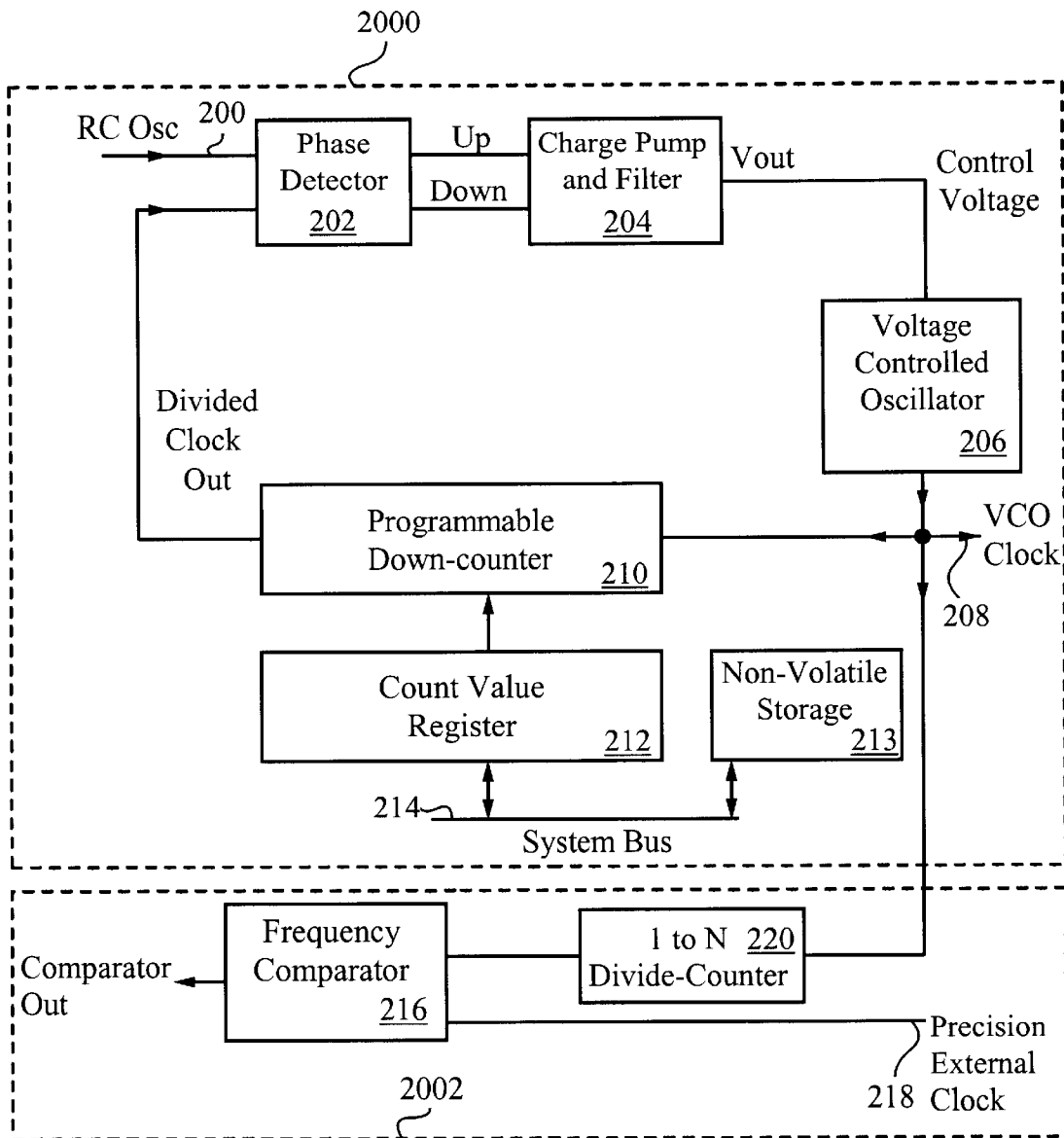


Fig. 2

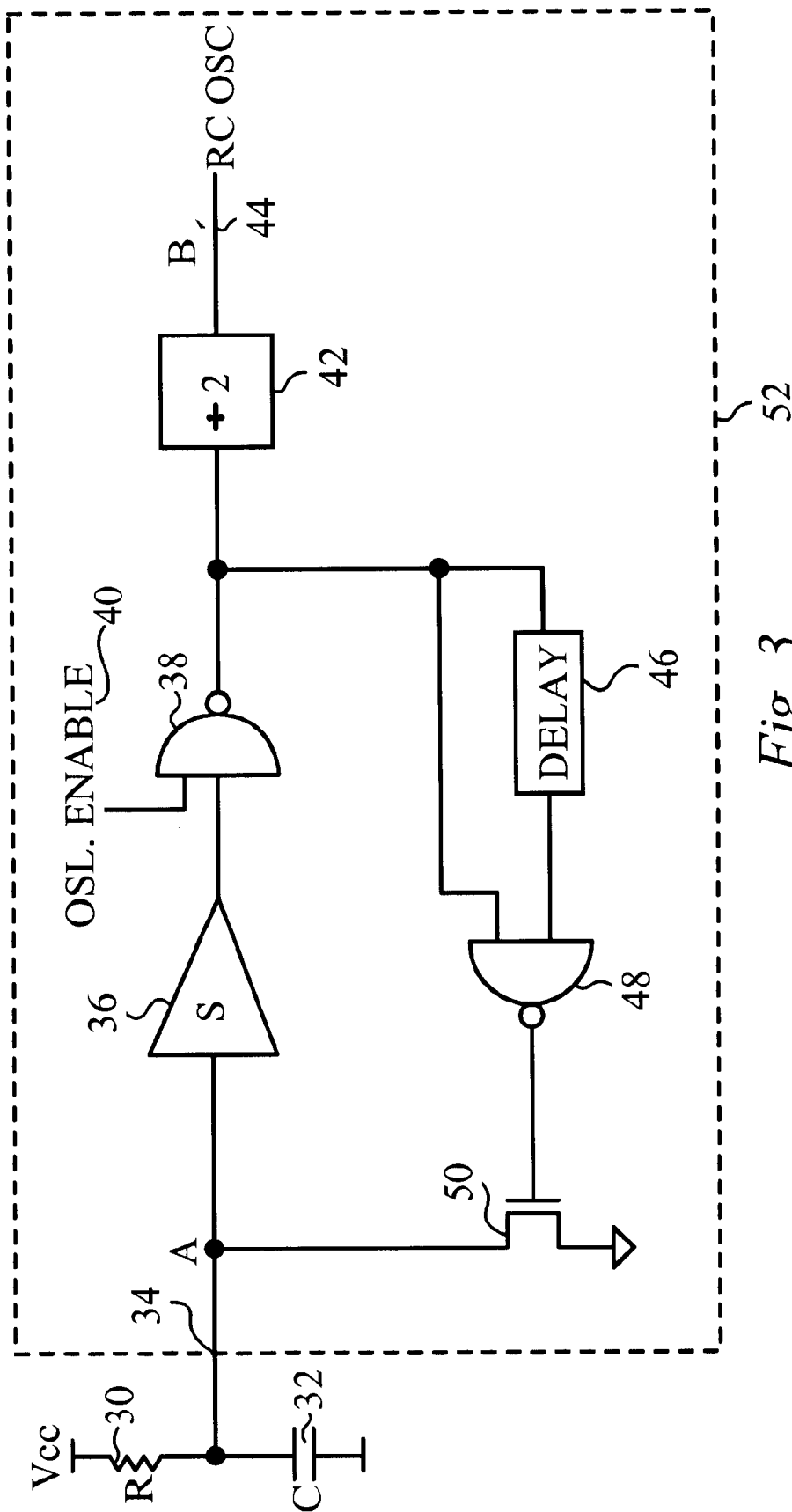


Fig. 3

## PRECISION CLOCK SYNTHESIZER USING RC OSCILLATOR AND CALIBRATION CIRCUIT

### FIELD OF THE INVENTION

This invention relates to a circuit for generating a clock signal and for controlling the frequency of the clock signal. More particularly, it relates to individually calibrating a preset value of a digital counter at the time of manufacture to control the frequency of a clock output.

### BACKGROUND OF THE INVENTION

Many applications require the generation of an accurate clock frequency for internal operations of a synchronous system. FIG. 1 shows a conventional phase lock loop (PLL) clock synthesizer. Conventional PLL design criteria and methods are well known. A reference oscillator signal **100** is coupled as a first input to a phase detector **102**. The phase detector **102** provides up/down signals as inputs to a charge pump and filter **104**. The voltage output from the charge pump and filter **104** is provided as an input to a voltage controlled oscillator VCO **106**. In response to the voltage generated by the charge pump and filter **104**, the VCO **106** generates a VCO Clock signal **108** that is the output of the system of FIG. 1. The VCO clock signal **108** is also coupled as an input to a down counter **110**. The down counter **110** reduces the frequency of the VCO clock signal **108** in accordance with a preset count value. The down counter **110** applies its output as a second input to the phase detector **102**. The phase detector compares the signal from the down counter **110** to the reference oscillator signal **100** and determines which is faster. The phase detector will either provide an up or a down signal to the charge pump and filter depending upon whether the reference oscillator signal **100** or the output of the down counter **110** is slower. In this way the VCO clock **108** is a multiple of the reference oscillator signal **100** by a ratio established by the down counter **110**.

According to conventional practice designers utilize a crystal controlled oscillator to generate the desired reference oscillator. A crystal is an external component to an integrated circuit. Even when mass produced, however, a crystal clock driver can be prohibitively expensive. This means that the use of a crystal adds expense to a system implementation. The cost of a crystal can be significant with respect to the cost of an integrated circuit. In inexpensive digital applications, however, such as digital film for a digital camera, the presence of a crystal oscillator adds to the product costs. Also, the printed circuit board must accommodate the presence of the crystal. This increases the size and the complexity of the printed circuit board, which translates to increased cost. In addition, a crystal oscillator has a relatively slow start time after the application of power to the circuit. Keeping the power applied to the circuit at all times to avoid this slow restart condition can violate the low power condition desired during an idle mode. Another drawback of a crystal oscillator is that the physical size of a crystal is relatively large, in comparison to a resistor and capacitor. In certain applications such as digital film, the size of the crystal can cause the overall size of the product to be undesirably large. In certain of such applications, the crystal height is sufficiently high that the PCB will not fit in the digital film cartridge.

At least these factors all indicate that using a crystal oscillator is disadvantageous. Yet, owing to the need for a high precision clock signal, integrated circuit designers and digital system designers conventionally use crystal oscillators for generating clock signals.

RC circuits have long been used to create an oscillating signal. RC oscillators are far cheaper than crystal oscillators, and can undesirably increase the cost in applications such as digital film. RC oscillators can be designed to track both power supply and temperature variations. Unfortunately, the manufacturing tolerances in RC components typically run in the five to ten percent range. In addition, semiconductor devices that are conventionally used in RC oscillators vary as a result of variations in the manufacturing process used to fabricate such devices. Thus, while RC oscillators can be made to operate at a constant and unvarying frequency, the initial frequency of an RC oscillator may not operate at a desired frequency.

There remains therefore a need for a system and method of developing a clock mechanism for use in digital circuits while avoiding the use of expensive crystal oscillators. There further remains a need for a system and method of using inexpensive RC oscillators in digital applications. There further remains a need to tune or adjust each RC circuit individually to compensate for the component variation inherent within each RC circuit element. There further remains a need for developing an RC oscillator that can reliably generate a signal satisfying the narrow tolerances of the digital applications.

### BRIEF SUMMARY OF THE INVENTION

The present invention provides a system for and method of developing a clock mechanism for use in digital circuits that avoids the use of crystal oscillators in clock signal generation. The present invention further provides a system for and method of using a relatively inexpensive RC oscillator in digital applications. The present invention further provides means for tuning each signal generator individually to compensate for the component variation within each circuit. The present invention further provides means for achieving far greater frequency accuracy than is normally possible through use of RC oscillators, thereby satisfying circumstances requiring narrow tolerances.

According to one embodiment of the present invention, a circuit for producing a frequency-controlled output signal comprises a phase lock loop. A reference clock is coupled as a first input to a phase detector. Preferably, the reference clock is generated by an RC oscillator. The phase detector provides up/down signals as inputs to a charge pump and filter. The voltage output from the charge pump and filter is provided as an input to a voltage controlled oscillator VCO. In response to the voltage generated by the charge pump and filter, the VCO generates a VCO Clock signal. The VCO clock signal is also coupled as an input to a programmable down counter. The down value controls the frequency of the VCO clock signal. The down count value is loaded into a register via an internal bus.

The down counter applies its output as a second input to the phase detector. The phase detector compares the signal from the down counter to the reference oscillator signal and determines which is faster. The phase detector will either provide an up or a down signal to the charge pump and filter depending upon whether the reference oscillator signal or the output of the down counter is slower. In this way the VCO clock is a multiple of the reference oscillator signal by a ratio established by the down counter, which is adjustable.

According to one embodiment of the present invention, the phase lock loop is coupled to a calibration system which measures the frequency of the VCO clock. The calibration system is used to calibrate the oscillator circuit during a manufacturing process. Once the oscillator circuit is

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