# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE PATENT TRIAL AND APPEAL BOARD

In re U.S. Patent No. 6,240,376 Trial No.: IPR 2012-00042

Application No.: 09/127,587

Filed: July 31, 1998 Issued: May 29, 2001

Atty. Dkt. No. 007121.00004

Inventors: Alain Raynaud

Luc M. Burgun

Patent Owner: Mentor Graphics

Corporation

For: METHOD AND

APPARATUS FOR GATE-

LEVEL SIMULATION OF

SYNTHESIZED

REGISTER TRANSFER LEVEL DESIGNS WITH

SOURCE-LEVEL DEBUGGING

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## PRELIMINARY RESPONSE BY PATENT OWNER UNDER 37 C.F.R. § 42.107



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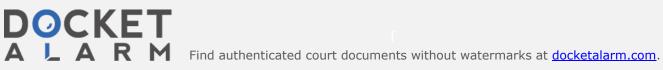


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#### **EXHIBIT LIST**

MG 2001	First Amended Complaint in <i>Mentor Graphics Corp. v. EVE-USA, Inc. and Emulation and Verification Engineering</i> , SA, 6:06-CV-00341-AA (D. OR., filed March 13, 2006)
MG 2002	Defendants' Unopposed Motion By Special Appearance For Extension Of Time To Respond To Plaintiff's First Amended Complaint in <i>Mentor Graphics Corp. v. EVE-USA, Inc. and Emulation and Verification Engineering</i> , SA, 6:06-CV-00341-AA (D. Or., filed May 23, 2006)
MG 2003	Order of Dismissal in <i>Mentor Graphics Corp. v. EVE-USA, Inc. and Emulation and Verification Engineering</i> , SA, 6:06-CV-00341-AA (D. Or., filed November 20, 2006)
MG 2004	Complaint for Declaratory Judgment and Injunctive Relief in Synopsys, Inc., EVE-USA, Inc. and Emulation and Verification Engineering, S.A. v. Mentor Graphics Corp., 3:12-cv-050025-LB (N.D. Cal., filed September 27, 2012)
MG 2005	Banner & Witcoff, Ltd.'s "Messenger Log"
MG 2006	October 4, 2012 Synopsys Press Release "Synopsys Acquires EVE"
MG 2007	EVE-USA's Supplemental Corporate Disclosure Statement, Docket No. 7, <i>Synopsys, Inc. et al. v. Mentor Graphics Corp.</i> , 3:12-CV-05025-MC (N.D. Cal. filed October. 26, 2012)
MG 2008	Jansen, D., <u>The Electronic Design Automation Handbook</u> , Kluwer Academic Publishers, 2003, Chapter 2
MG 2009	Bhatnagar, <u>Advanced ASIC Chip Synthesis: Using Synopsys®</u> <u>Design Compiler<sup>TM</sup> and PrimeTime<sup>®</sup></u> , Kluwer Academic Publishers, 1999
MG 2010	Gregory et al. U.S. Patent No. 5,937,190



MG 2011 HDL Compiler™ for VHDL User Guide, Version F-2011.09-SP4, March 2012, SYNOPSYS, Section 4



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