Paper No.		

UNITED STATES PATENT AND TRADEMARK OFF:	ICE
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BEFORE THE PATENT TRIAL AND APPEAL BOARD

SYNOPSYS, INC. Petitioner

V.

Patent of MENTOR GRAPHICS CORPORATION
Patent Owner

Case IPR2012-00042 (SCM) Patent 6,240,376 B1

Mail Stop *Patent Board, PTAB*United State Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE



TABLE OF CONTENTS

TAB	BLE O	F CO	NTENTS	ii	
EXE	HBIT	LIST	••••••	iii	
I.	. PETITIONER SYNOPSYS' <i>INTER PARTES REVIEW</i> IS NOT BARRED BY § 315(B) OR ASSIGNOR ESTOPPEL				
II.	CLA	AIM C	ONSTRUCTION	2	
	A.	The	Board's Construction Of Instrumentation Signal Is Correct	3	
		1.	The claim language supports the Board's construction	4	
		2.	Mentor's construction conflicts with the specification	5	
		3.	Mentor's extrinsic evidence cannot overcome the intrinsic record.	8	
III.	GRI	EGOR	Y ANTICIPATES THE CHALLENGED CLAIMS		
	A.	Greg	gory Anticipates Claim 1	9	
		1.	Gregory satisfies the "instrumentation signal" limitation	9	
		2.	Gregory satisfies the "execution status" limitation	10	
	B.	Greg	gory Anticipates Dependent Claims 2-4.	12	
	C.	Greg	gory Anticipates Claim 5	14	
	D.	Greg	gory Anticipates Dependent Claims 6-9 And 11	14	
	E.	Greg	gory Anticipates Claims 28-29.	15	
IV.	CON	NCLU	SION	15	
CER	etifi(CATE	OF SERVICE	17	



EXHIBIT LIST

Previously Filed

- 1001 U.S. Patent No. 6,240,376 to Raynaud, et al.
- 1002 Prosecution history of application Serial No. 09/127,584, which matured into the '376 patent.
- 1003 Chen, et al., "A Source-Level Dynamic Analysis Methodology and Tool for High-Level Synthesis," Proceedings of the Tenth International Symposium on System Synthesis, 1997, pp. 134-140, Sep. 1997.
- Koch, et al., "Breakpoints and Breakpoint Detection in Source Level Emulation," ISSS Proceedings of the 9th International Symposium on System Synthesis, pp. 26-31 (1996).
- 1005 Koch Publication information from CiteCeerX and ACM archives.
- Koch, et al., "Debugging of Behavioral VHDL Specifications by Source Level Emulation," Proceedings of the European Design Automation Conference, pp. 256-261, September 1995.
- 1007 U.S. Patent No. 6,132,109 to Gregory, et al.
- HDL-ICETM ASIC Emulation System, Quickturn Design Systems, Inc.
- 1009 Prosecution history for application Serial No. 08/566,401, which matured into U.S. Patent No. 5,838,948.
- 1010 U.S. Patent No. 5,960,191 to Sample, et al.
- 1011 Transcript of Initial Conference Call, Mar. 21, 2013
- U.S. Patent No. 6,363,520 to Boubezari et al.
- Declaration of Dr. Brad Hutchings in support of Petitioner's Opposition to Patent Owner's Substitute Motion to Amend
- Excerpts from Field-Programmable Gate Array Technology, Stephen M. Trimberger, 1994.



EXHIBIT LIST (CONT'D)

- Taking Advantage of Reconfigurable Logic, Bradly K. Fawcett, Seventh Annual IEEE International Proceedings, ASIC Conference, 1994, pgs. 227-230.
- Effects of FPGA Architecture on FPGA Routing, Stephen Trimberger, 32nd ACM/IEEE Design Automation Conference, 1995.
- A Reprogrammable Gate Array and Applications, Stephen Trimberger, Proceedings of the IEEE, Vol. 81, No. 7, July 1993.
- Proper Use of Hierarchy in HDL-Based High Density FGPA Design, Carol A. Fields, published in Lecture Notes in Computer Science, 1995 at pgs. 168-177.
- Deposition Transcript of Dr. Majid Sarrafzadeh dated August, 22, 2013.
- Declaration of Travis Jensen.



I. PETITIONER SYNOPSYS' *INTER PARTES REVIEW* IS NOT BARRED BY § 315(b) OR ASSIGNOR ESTOPPEL.

Section 315(b) does not bar Synopsys' request for inter partes review. Mentor's privity argument fails because Mentor admitted that Synopsys and EVE were not in privity in 2006 when EVE was served with a complaint alleging infringement. See, e.g., Paper 24 at 3; Paper 16 at 16-17; Paper 23 at 4-5; Paper 15 at 2, 7-8. The Board expressly held this was the legal standard for § 315(b) and that "the effective filing date of the petition and the status of EVE as a real partyin-interest to the *inter partes* review" are not relevant to this standard. Paper 24 at 3. In any event, Mentor cannot prove that Synopsys and EVE were in privity prior to, or on, the filing date of the petition. Mentor now argues that privity should be assessed at "any time before the institution of the IPR, including after the filing of the Petition." Response at 7. This argument is foreclosed by the plain language of § 315(b) itself which refers to the date "the petition requesting the proceeding is filed." Mentor's argument that EVE was a real party in interest fails because Mentor cites no evidence to support its assertions.

Neither does assignor estoppel bar Synopsys' request. Mentor cites no law or legislative history suggesting that assignor estoppel is cognizable in an *inter partes* review. *See* Paper 24 at 7-10. Nor does Mentor show that *inter partes* review should be different from *inter partes* reexamination where it was recognized that "[t]he Office, an administrative agency, is bound by the statues and



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